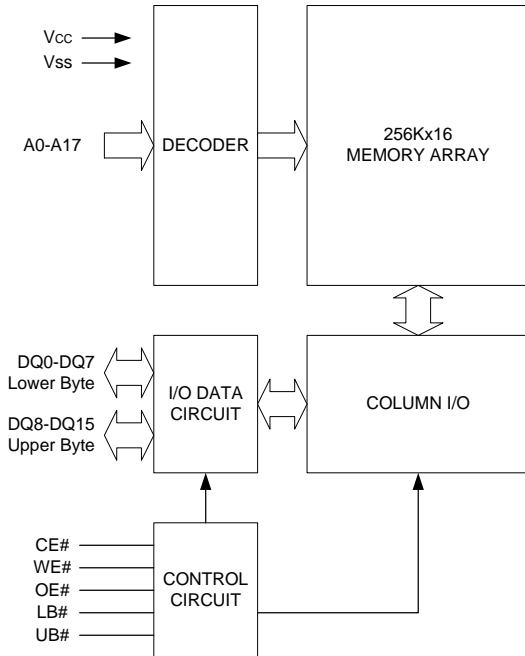




## REVISION HISTORY

<u>Revision</u>	<u>Description</u>	<u>Issue Date</u>
Rev. 1.0	Initial Issue	Mar.23.2006
Rev. 1.1	Revised $V_{IL} = 0.6V \Rightarrow 0.8V$	Jun.09.2006
Rev. 1.2	Revised <b><u>PACKAGE OUTLINE DIMENSION</u></b> (TSOP II)	Apr.12.2007
Rev. 2.0	Added LL Spec. Revised <b>TEST CONDITION</b> of $I_{SB1}/I_{DR}$ Added -12ns Spec. Revised $I_{CC}$ and $I_{SB1}$ Added I grade Revised <b><u>ABSOLUTE MAXIMUM RATINGS</u></b>	Jun.25.2007
Rev. 2.1	Revised <b>TEST CONDITION</b> of $I_{CC}$ Revised <b><u>FEATURES &amp; ORDERING INFORMATION</u></b> <b>Lead free</b> <b>and green package available to Green package available</b> Deleted $T_{SOLDER}$ in <b><u>ABSOLUTE MAXIMUM RATINGS</u></b> Added packing type in <b><u>ORDERING INFORMATION</u></b>	Apr.17.2009
Rev. 2.2	Added package type TFBGA	May.06.2010
Rev. 2.3	Revised <b><u>ORDERING INFORMATION</u></b> in page 12	Aug.30.2010
Rev. 2.4	Revised -12ns spec as -10ns spec and related parameter	July.03.2013
Rev. 2.5	Revised <b><u>ORDERING INFORMATION</u></b> in page 11 Correct <b><u>ORDERING INFORMATION</u></b> Typo. Added power type in <b><u>ORDERING INFORMATION</u></b>	May.20.2016
Rev. 2.6	Added -12ns Spec. Revised $I_{SB1}$ & $I_{CC}$ Revised <b><u>PIN DESCRIPTION</u></b> in page 2 Deleted -25ns Spec. Deleted Package Type: 48-ball 6mm x 8mm TFBGA Deleted <b>WRITE CYCLE</b> Notes : 1. WE#,CE#, LB#, UB# must be high during all address transitions. In page 9	Dec.27.2016

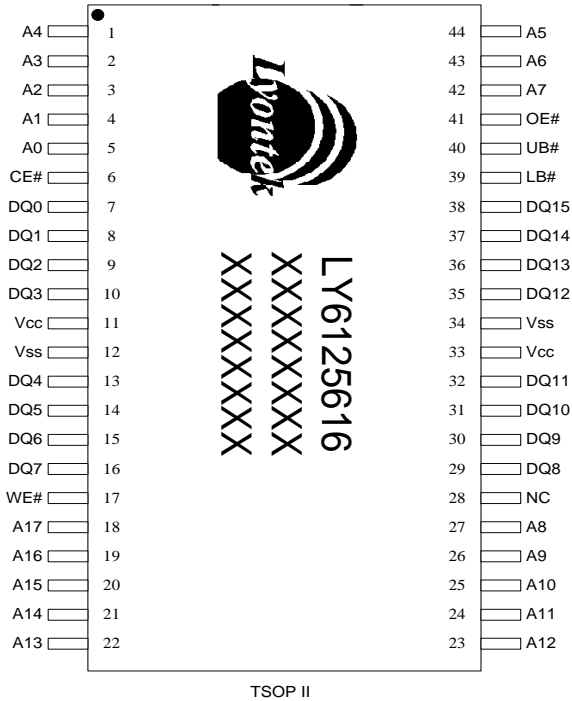


**FUNCTIONAL BLOCK DIAGRAM**

**PIN DESCRIPTION**

SYMBOL	DESCRIPTION
A0 - A17	Address Inputs
DQ0 - DQ15	Data Inputs/Outputs
CE#	Chip Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
LB#	Lower Byte Control
UB#	Upper Byte Control
Vcc	Power Supply
Vss	Ground
NC	No Connection



### PIN CONFIGURATION





### ABSOLUTE MAXIMUM RATINGS\*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on V <sub>CC</sub> relative to V <sub>SS</sub>	V <sub>T1</sub>	-0.5 to 6.5	V
Voltage on any other pin relative to V <sub>SS</sub>	V <sub>T2</sub>	-0.5 to V <sub>CC</sub> +0.5	V
Operating Temperature	T <sub>A</sub>	0 to 70(C grade)	°C
		-20 to 80(E grade)	
		-40 to 85(I grade)	
Storage Temperature	T <sub>STG</sub>	-65 to 150	°C
Power Dissipation	P <sub>D</sub>	1	W
DC Output Current	I <sub>OUT</sub>	50	mA

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

### TRUTH TABLE

MODE	CE#	OE#	WE#	LB#	UB#	I/O OPERATION		SUPPLY CURRENT
						DQ0 - DQ7	DQ8 - DQ15	
Standby	H	X	X	X	X	High-Z	High-Z	I <sub>SB1</sub>
Output Disable	L	H	H	X	X	High-Z	High-Z	I <sub>CC</sub>
	L	X	X	H	H	High-Z	High-Z	
Read	L	L	H	L	H	D <sub>OUT</sub>	High-Z	I <sub>CC</sub>
	L	L	H	H	L	High-Z	D <sub>OUT</sub>	
	L	L	H	L	L	D <sub>OUT</sub>	D <sub>OUT</sub>	
Write	L	X	L	L	H	D <sub>IN</sub>	High-Z	I <sub>CC</sub>
	L	X	L	H	L	High-Z	D <sub>IN</sub>	
	L	X	L	L	L	D <sub>IN</sub>	D <sub>IN</sub>	

Note: H = V<sub>IH</sub>, L = V<sub>IL</sub>, X = Don't care.



## DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP. *4	MAX.	UNIT	
Supply Voltage	V <sub>CC</sub>		4.5	5.0	5.5	V	
Input High Voltage	V <sub>IH</sub> *1		2.2	-	V <sub>CC</sub> +0.3	V	
Input Low Voltage	V <sub>IL</sub> *2		-0.3	-	0.8	V	
Input Leakage Current	I <sub>LI</sub>	V <sub>CC</sub> ≥ V <sub>IN</sub> ≥ V <sub>SS</sub>	-1	-	1	μA	
Output Leakage Current	I <sub>LO</sub>	V <sub>CC</sub> ≥ V <sub>OUT</sub> ≥ V <sub>SS</sub> , Output Disabled	-1	-	1	μA	
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -4mA	2.4	-	-	V	
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 8mA	-	-	0.4	V	
Average Operating Power supply Current	I <sub>CC</sub>	Cycle time = MIN. CE# = V <sub>IL</sub> , I <sub>I/O</sub> = 0mA Others at V <sub>IL</sub> or V <sub>IH</sub>	10	-	120	215	mA
			12	-	80	190	mA
			15	-	100	140	mA
			20	-	80	110	mA
Standby Power Supply Current	I <sub>SB1</sub>	CE# ≥ V <sub>CC</sub> - 0.2V Others at 0.2V / V <sub>CC</sub> -0.2V	10/12	-	3.5	15	mA
			15/20	-	0.1	3*5	mA
			15/20LL	-	20	100*6	μA

Notes:

- V<sub>IH</sub>(max) = V<sub>CC</sub> + 2.0V for pulse width less than 6ns.
- V<sub>IL</sub>(min) = V<sub>SS</sub> - 2.0V for pulse width less than 6ns.
- Over/Undershoot specifications are characterized on engineering evaluation stage, not for mass production test.
- Typical values are included for reference only and are not guaranteed or tested.  
Typical values are measured at V<sub>CC</sub> = V<sub>CC</sub>(TYP.) and T<sub>A</sub> = 25°C
- 1mA for special request
- 50μA for special request

## CAPACITANCE (T<sub>A</sub> = 25°C, f = 1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Input Capacitance	C <sub>IN</sub>	-	8	pF
Input/Output Capacitance	C <sub>I/O</sub>	-	10	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

## AC TEST CONDITIONS

Input Pulse Levels	0.2V to V <sub>CC</sub> - 0.2V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	C <sub>L</sub> = 30pF + 1TTL, I <sub>OH</sub> /I <sub>OL</sub> = -8mA/16mA



## AC ELECTRICAL CHARACTERISTICS

### (1) READ CYCLE

PARAMETER	SYM.	LY6125616-10		LY6125616-12		LY6125616-15		LY6125616-20		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t <sub>RC</sub>	10	-	12	-	15	-	20	-	ns
Address Access Time	t <sub>AA</sub>	-	10	-	12	-	15	-	20	ns
Chip Enable Access Time	t <sub>ACE</sub>	-	10	-	12	-	15	-	20	ns
Output Enable Access Time	t <sub>OE</sub>	-	5	-	6	-	7	-	8	ns
Chip Enable to Output in Low-Z	t <sub>CLZ</sub> *	2	-	3	-	4	-	4	-	ns
Output Enable to Output in Low-Z	t <sub>OLZ</sub> *	0	-	0	-	0	-	0	-	ns
Chip Disable to Output in High-Z	t <sub>CHZ</sub> *	-	5	-	6	-	7	-	8	ns
Output Disable to Output in High-Z	t <sub>OHZ</sub> *	-	5	-	6	-	7	-	8	ns
Output Hold from Address Change	t <sub>OH</sub>	3	-	3	-	3	-	3	-	ns
LB#, UB# Access Time	t <sub>BA</sub>	-	5	-	6	-	7	-	8	ns
LB#, UB# to High-Z Output	t <sub>BHZ</sub> *	-	5	-	6	-	7	-	8	ns
LB#, UB# to Low-Z Output	t <sub>BLZ</sub> *	2	-	3	-	4	-	4	-	ns

### (2) WRITE CYCLE

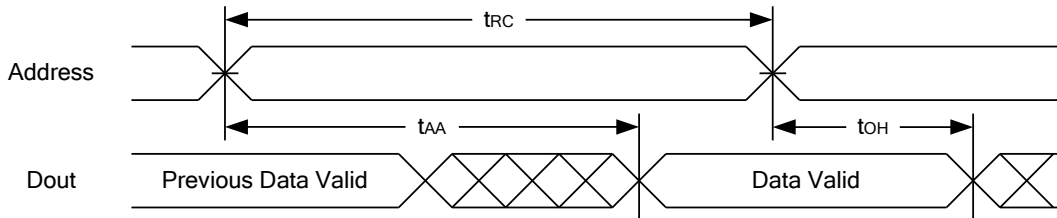
PARAMETER	SYM.	LY6125616-10		LY6125616-12		LY6125616-15		LY6125616-20		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t <sub>WC</sub>	10	-	12	-	15	-	20	-	ns
Address Valid to End of Write	t <sub>AW</sub>	8	-	10	-	12	-	16	-	ns
Chip Enable to End of Write	t <sub>CW</sub>	8	-	10	-	12	-	16	-	ns
Address Set-up Time	t <sub>AS</sub>	0	-	0	-	0	-	0	-	ns
Write Pulse Width	t <sub>WP</sub>	8	-	9	-	10	-	11	-	ns
Write Recovery Time	t <sub>WR</sub>	0	-	0	-	0	-	0	-	ns
Data to Write Time Overlap	t <sub>DW</sub>	6	-	7	-	8	-	9	-	ns
Data Hold from End of Write Time	t <sub>DH</sub>	0	-	0	-	0	-	0	-	ns
Output Active from End of Write	t <sub>OW</sub> *	2	-	3	-	4	-	5	-	ns
Write to Output in High-Z	t <sub>WHZ</sub> *	-	6	-	7	-	8	-	9	ns
LB#, UB# Valid to End of Write	t <sub>BW</sub>	8	-	10	-	12	-	16	-	ns

\*These parameters are guaranteed by device characterization, but not production tested.

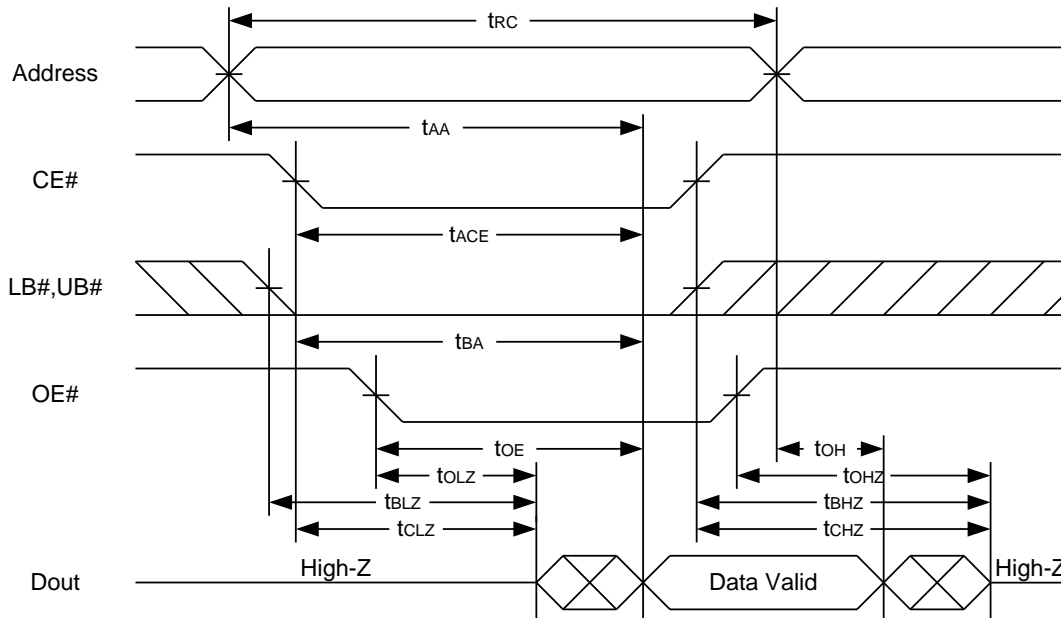


### TIMING WAVEFORMS

#### READ CYCLE 1 (Address Controlled) (1,2)



#### READ CYCLE 2 (CE# and OE# Controlled) (1,3,4,5)



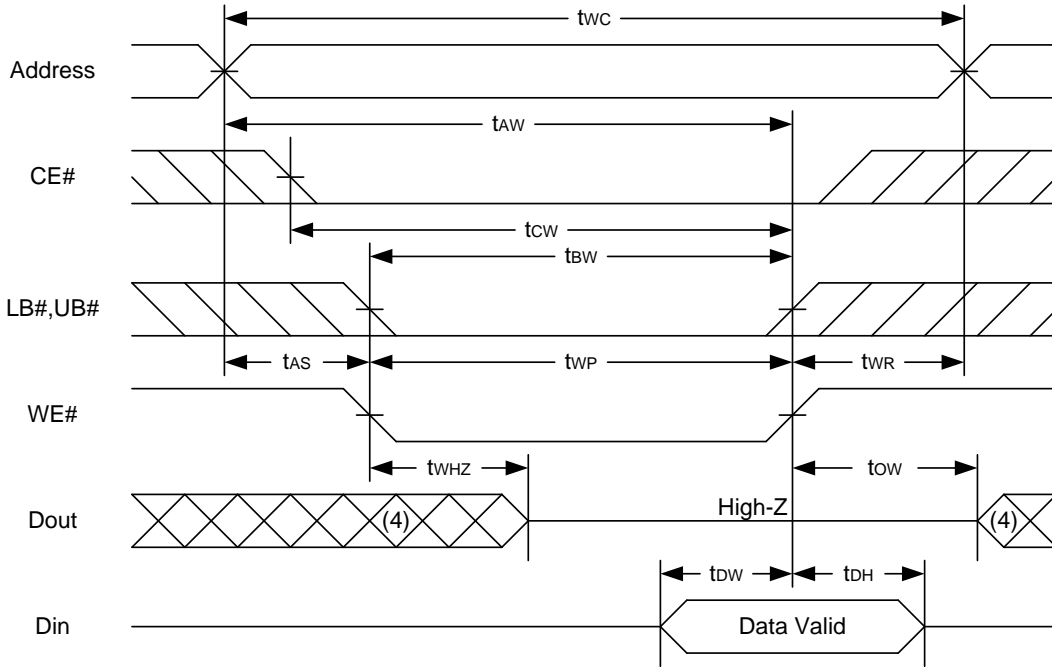
#### Notes :

1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low, LB# or UB# = low.
3. Address must be valid prior to or coincident with CE# = low, LB# or UB# = low transition; otherwise  $t_{AA}$  is the limiting parameter.
4.  $t_{CLZ}$ ,  $t_{BLZ}$ ,  $t_{OLZ}$ ,  $t_{CHZ}$ ,  $t_{BHZ}$  and  $t_{OHZ}$  are specified with  $C_L = 5pF$ . Transition is measured  $\pm 500mV$  from steady state.
5. At any given temperature and voltage condition,  $t_{CHZ}$  is less than  $t_{CLZ}$ ,  $t_{BHZ}$  is less than  $t_{BLZ}$ ,  $t_{OHZ}$  is less than  $t_{OLZ}$ .

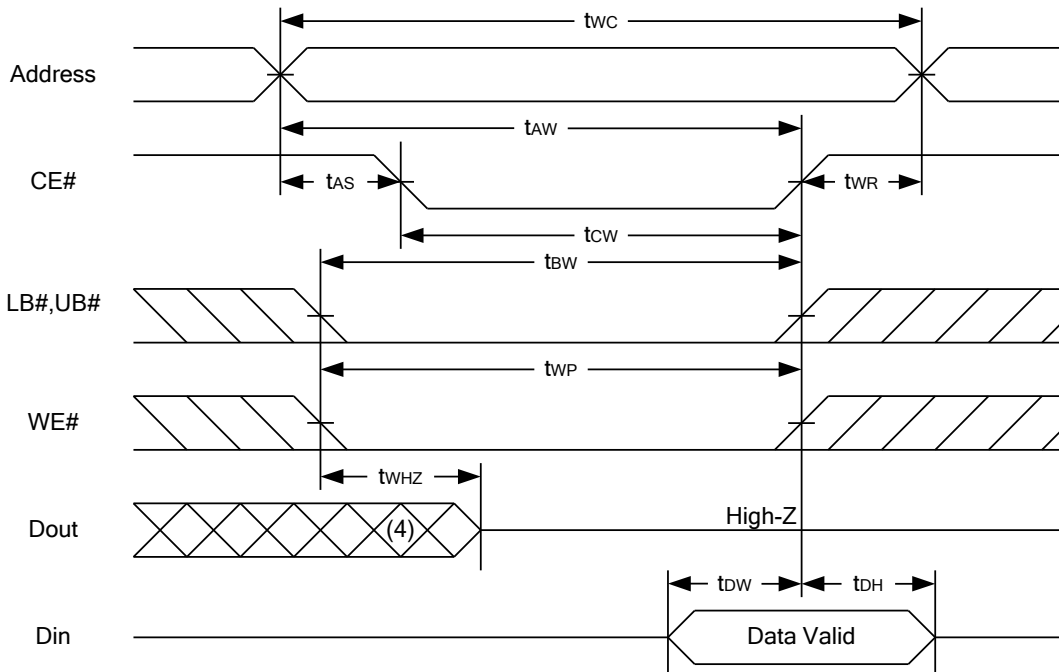




#### WRITE CYCLE 1 (WE# Controlled) (1,2,4,5)

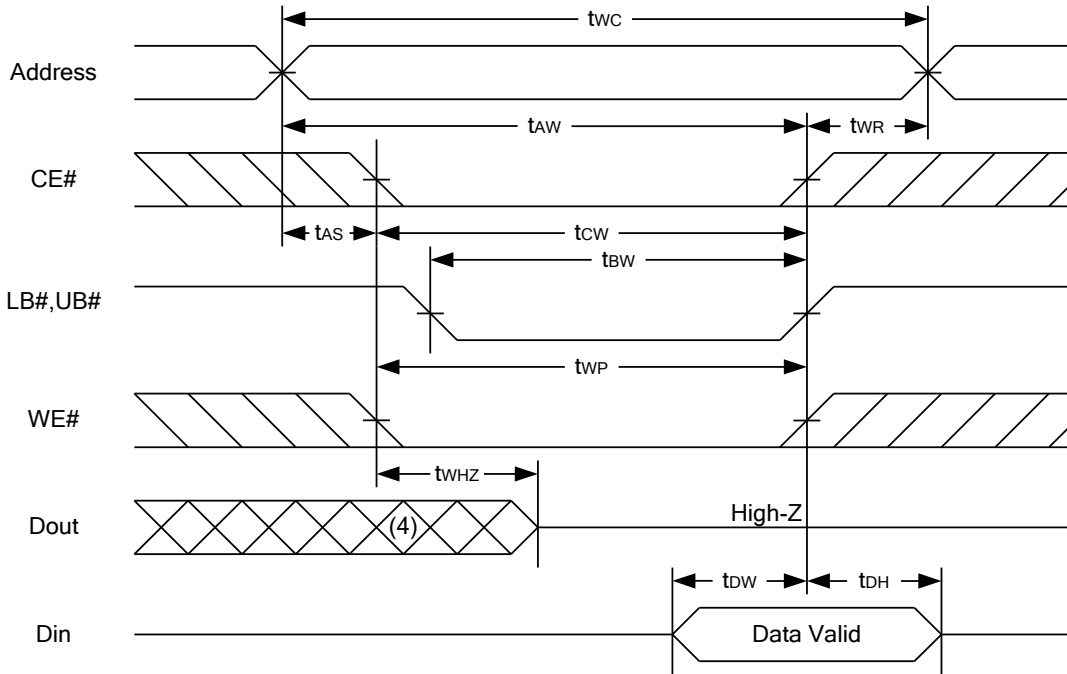


#### WRITE CYCLE 2 (CE# Controlled) (1,4,5)





#### WRITE CYCLE 3 (LB#,UB# Controlled) (1,4,5)



Notes :

1. A write occurs during the overlap of a low CE#, low WE#, LB# or UB# = low.
2. During a WE# controlled write cycle with OE# low,  $t_{WP}$  must be greater than  $t_{WHZ} + t_{DW}$  to allow the drivers to turn off and data to be placed on the bus.
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the CE#, LB#, UB# low transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
5.  $t_{OW}$  and  $t_{WHZ}$  are specified with  $C_L = 5pF$ . Transition is measured  $\pm 500mV$  from steady state.

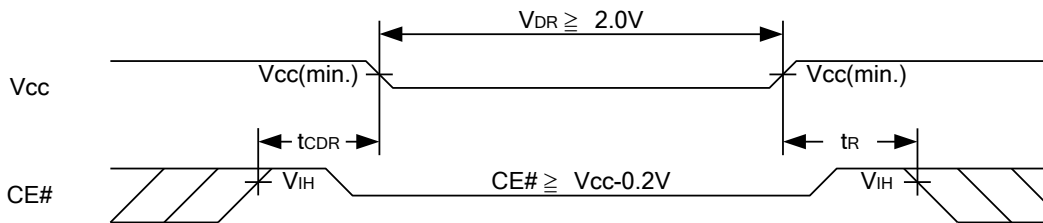


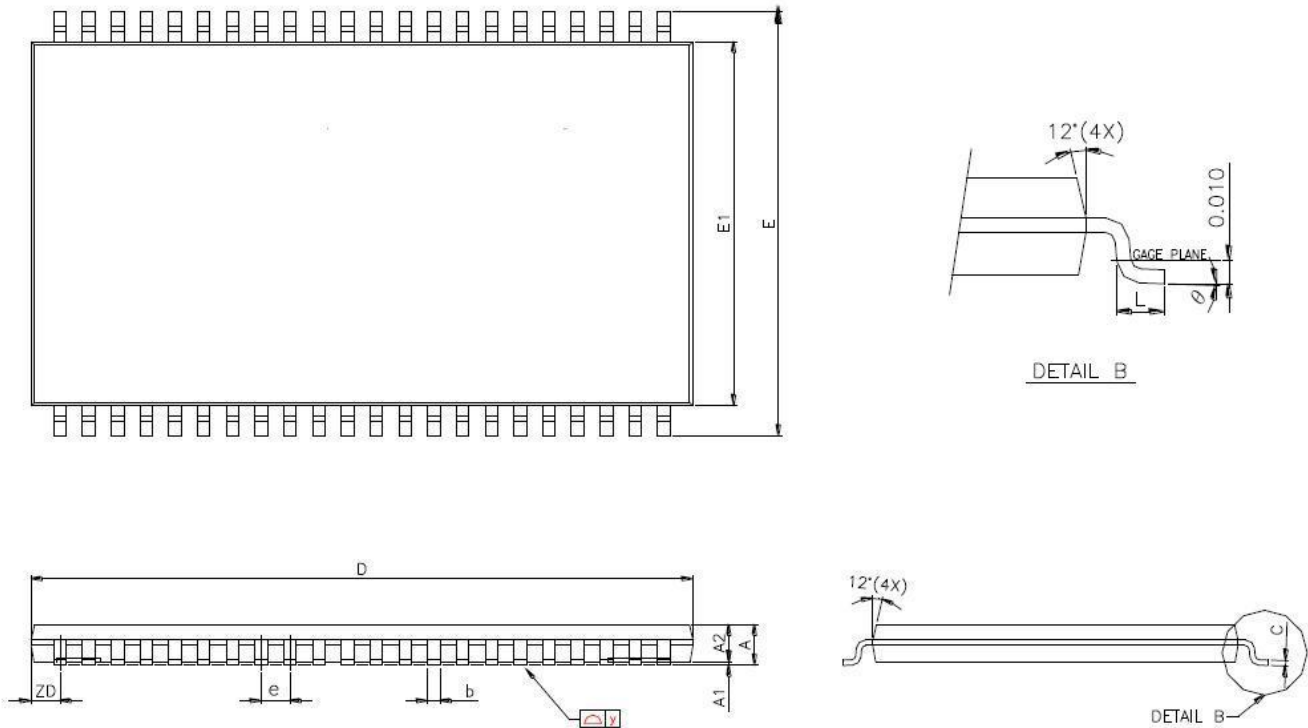
### DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
V <sub>CC</sub> for Data Retention	V <sub>DR</sub>	CE# ≥ V <sub>CC</sub> - 0.2V	2.0	-	5.5	V	
Data Retention Current	I <sub>DR</sub>	V <sub>CC</sub> = 2.0V, CE# ≥ V <sub>CC</sub> - 0.2V Other pins at 0.2V or V <sub>CC</sub> -0.2V	10/12	-	-	10	mA
			15/20	-	0.05	2	mA
			15/20LL	-	10	50	μA
Chip Disable to Data Retention Time	t <sub>CDR</sub>	See Data Retention Waveforms (below)	0	-	-	ns	
Recovery Time	t <sub>R</sub>		t <sub>RC</sub> *	-	-	ns	

t<sub>RC</sub>\* = Read Cycle Time

### DATA RETENTION WAVEFORM



**PACKAGE OUTLINE DIMENSION**
**44-pin 400mil TSOP II Package Outline Dimension**


SYMBOLS	DIMENSIONS IN MILLMETERS			DIMENSIONS IN MILS		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	-	-	1.20	-	-	47.2
A1	0.05	0.10	0.15	2.0	3.9	5.9
A2	0.95	1.00	1.05	37.4	39.4	41.3
b	0.30	-	0.45	11.8	-	17.7
c	0.12	-	0.21	4.7	-	8.3
D	18.212	18.415	18.618	717	725	733
E	11.506	11.760	12.014	453	463	473
E1	9.957	10.160	10.363	392	400	408
e	-	0.800	-	-	31.5	-
L	0.40	0.50	0.60	15.7	19.7	23.6
ZD	-	0.805	-	-	31.7	-
y	-	-	0.076	-	-	3
θ	0°	3°	6°	0°	3°	6°



#### ORDERING INFORMATION

Package Type	Access Time (Speed)(ns)	Power Type	Temperature Range(°C)	Packing Type	Lyontek Item No.		
44-pin (400mil) TSOP II	10	Normal Power	0°C~70°C	Tray	LY6125616ML-10		
				Tape Reel	LY6125616ML-10T		
			-40°C~85°C	Tray	LY6125616ML-10I		
				Tape Reel	LY6125616ML-10IT		
	12	Normal Power	0°C~70°C	Tray	LY6125616ML-12		
				Tape Reel	LY6125616ML-12T		
			-40°C~85°C	Tray	LY6125616ML-12I		
				Tape Reel	LY6125616ML-12IT		
	15	Normal Power	0°C~70°C	Tray	LY6125616ML-15		
				Tape Reel	LY6125616ML-15T		
				-20°C~80°C	Tray	LY6125616ML-15E	
					Tape Reel	LY6125616ML-15ET	
			-40°C~85°C	Tray	LY6125616ML-15I		
				Tape Reel	LY6125616ML-15IT		
				Ultra Low Power	0°C~70°C	Tray	LY6125616ML-15LL
						Tape Reel	LY6125616ML-15LLT
			-40°C~85°C		Tray	LY6125616ML-15LLI	
					Tape Reel	LY6125616ML-15LLIT	
			20	Normal Power	0°C~70°C	Tray	LY6125616ML-20
						Tape Reel	LY6125616ML-20T
	-20°C~80°C	Tray				LY6125616ML-20E	
		Tape Reel				LY6125616ML-20ET	
	-40°C~85°C	Tray			LY6125616ML-20I		
		Tape Reel			LY6125616ML-20IT		
Ultra Low Power		0°C~70°C			Tray	LY6125616ML-20LL	
					Tape Reel	LY6125616ML-20LLT	
	-40°C~85°C	Tray			LY6125616ML-20LLI		
		Tape Reel			LY6125616ML-20LLIT		



**Lyontek Inc.**

**LY6125616**

Rev. 2.6

**5V 256K X 16 BIT HIGH SPEED CMOS SRAM**

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