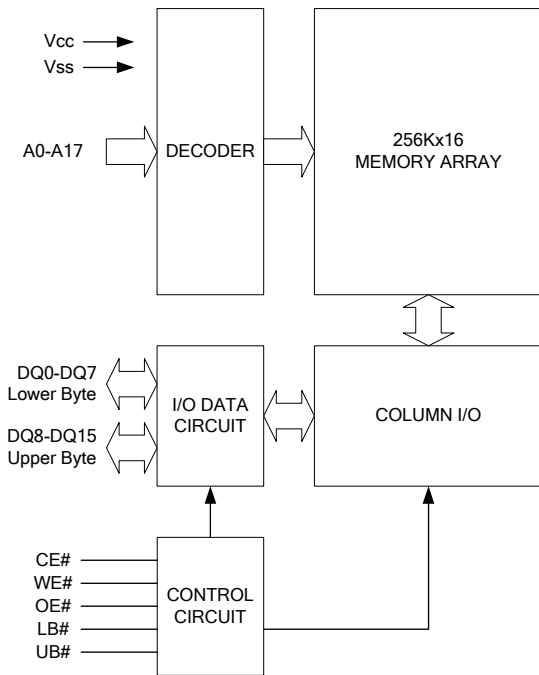




REVISION HISTORY

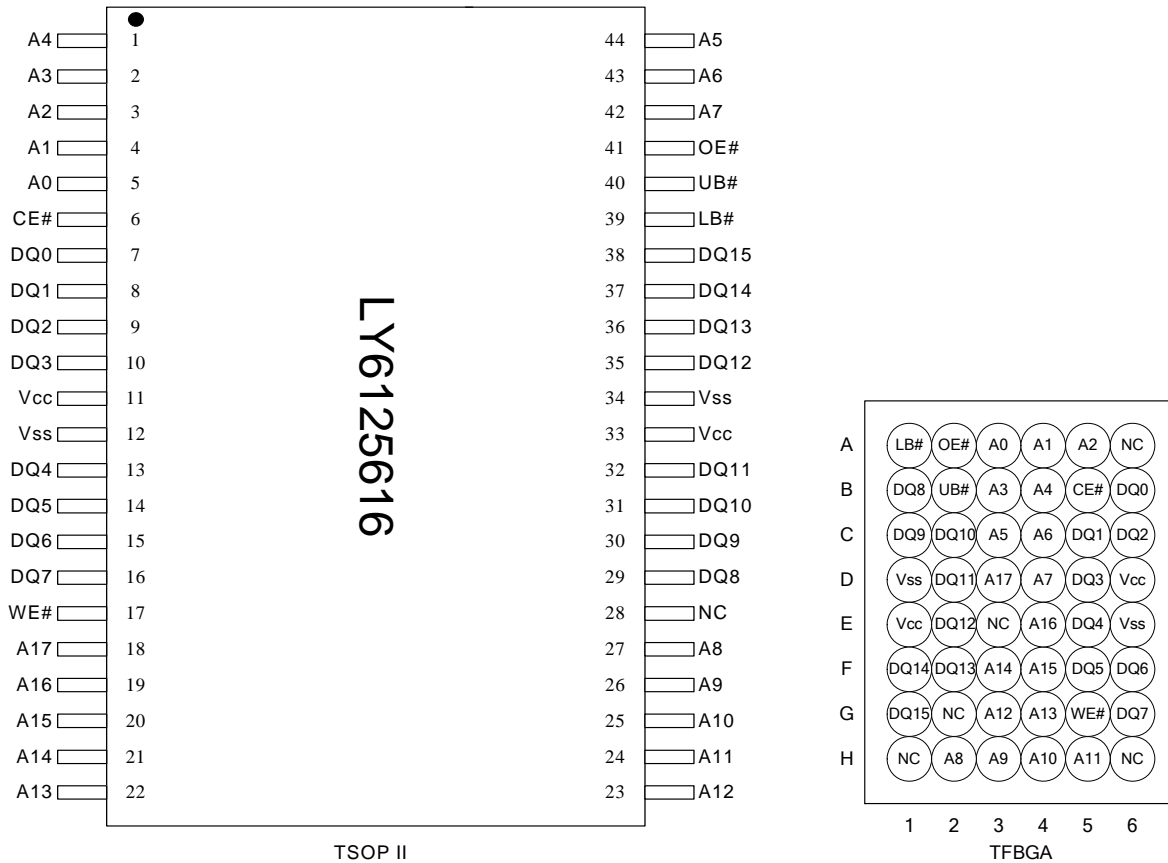
<u>Revision</u>	<u>Description</u>	<u>Issue Date</u>
Rev. 1.0	Initial Issue	Mar.23.2006
Rev. 1.1	Revised $V_{IL} = 0.6V \Rightarrow 0.8V$	Jun.9.2006
Rev. 1.2	Revised Package Outline Dimension(TSOP-II)	Apr.12.2007
Rev. 2.0	Added LL Spec. Revised Test Condition of I_{SB1}/I_{DR} Added -12ns Spec. Revised I_{CC} and I_{SB1} Added I grade	Jun.25.2007
Rev. 2.1	Revised <u>ABSOLUTE MAXIMUM RATINGS</u> Revised Test Condition of I_{CC} Revised <u>FEATURES & ORDERING INFORMATION</u> <u>Lead free and green package available to Green package available</u> Deleted T_{SOLDER} in <u>ABSOLUTE MAXIMUM RATINGS</u> Added packing type in <u>ORDERING INFORMATION</u>	Apr.17.2009
Rev. 2.2	Added package type TFBGA	May.6.2010
Rev. 2.3	Revised <u>ORDERING INFORMATION</u> in page 12	Aug.25.2010

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A17	Address Inputs
DQ0 – DQ15	Data Inputs/Outputs
CE#	Chip Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
LB#	Lower Byte Control
UB#	Upper Byte Control
Vcc	Power Supply
Vss	Ground

PIN CONFIGURATION

ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on Vcc relative to Vss	V_{T1}	-0.5 to 6.5	V
Voltage on any other pin relative to Vss	V_{T2}	-0.5 to $V_{cc}+0.5$	V
Operating Temperature	T_A	0 to 70(C grade)	°C
		-20 to 80(E grade)	
		-40 to 85(I grade)	
Storage Temperature	T_{STG}	-65 to 150	°C
Power Dissipation	P_D	1	W
DC Output Current	I_{OUT}	50	mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.



TRUTH TABLE

MODE	CE#	OE#	WE#	LB#	UB#	I/O OPERATION		SUPPLY CURRENT
						DQ0-DQ7	DQ8-DQ15	
Standby	H	X	X	X	X	High - Z	High - Z	I _{SB1}
Output Disable	L	H	H	X	X	High - Z	High - Z	I _{CC}
	L	X	X	H	H	High - Z	High - Z	
Read	L	L	H	L	H	D _{OUT}	High - Z	I _{CC}
	L	L	H	H	L	High - Z	D _{OUT}	
	L	L	H	L	L	D _{OUT}	D _{OUT}	
Write	L	X	L	L	H	D _{IN}	High - Z	I _{CC}
	L	X	L	H	L	High - Z	D _{IN}	
	L	X	L	L	L	D _{IN}	D _{IN}	

Note: H = V_{IH}, L = V_{IL}, X = Don't care.

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP. ⁴	MAX.	UNIT	
Supply Voltage	V _{CC}		4.5	5.0	5.5	V	
Input High Voltage	V _{IH} ¹		2.2	-	V _{CC} +0.3	V	
Input Low Voltage	V _{IL} ²		- 0.3	-	0.8	V	
Input Leakage Current	I _{LI}	V _{CC} ≥ V _{IN} ≥ V _{SS}	- 1	-	1	μA	
Output Leakage Current	I _{LO}	V _{CC} ≥ V _{OUT} ≥ V _{SS} , Output Disabled	- 1	-	1	μA	
Output High Voltage	V _{OH}	I _{OH} = -4mA	2.4	-	-	V	
Output Low Voltage	V _{OL}	I _{OL} = 8mA	-	-	0.4	V	
Average Operating Power supply Current	I _{CC}	Cycle time = Min. CE# = V _{IL} , I _{I/O} = 0mA Others at V _{IL} or V _{IH}	12	-	-	180	mA
			15	-	100	140	mA
			20	-	80	110	mA
			25	-	75	100	mA
Standby Power Supply Current	I _{SB1}	CE# ≥ V _{CC} - 0.2V Others at 0.2V / V _{CC} -0.2V	12	-	-	15	mA
			15/20/25	-	0.1	3 ^{*5}	mA
			15/20/25LL	-	20	100 ^{*6}	μA

Notes:

- V_{IH}(max) = V_{CC} + 3.0V for pulse width less than 10ns.
- V_{IL}(min) = V_{SS} - 3.0V for pulse width less than 10ns.
- Over/Undershoot specifications are characterized, not 100% tested.
- Typical values are included for reference only and are not guaranteed or tested.
Typical valued are measured at V_{CC} = V_{CC}(TYP.) and T_A = 25°C
- 1mA for special request
- 50μA for special request

CAPACITANCE (T_A = 25°C, f = 1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C _{IN}	-	8	pF
Input/Output Capacitance	C _{I/O}	-	10	pF

Note : These parameters are guaranteed by device characterization, but not production tested.



AC TEST CONDITIONS

Input Pulse Levels	0.2V to $V_{CC} - 0.2V$
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	$C_L = 30pF + 1TTL, I_{OH}/I_{OL} = -8mA/16mA$

AC ELECTRICAL CHARACTERISTICS

(1) READ CYCLE

PARAMETER	SYM.	LY6125616-12		LY6125616-15		LY6125616-20		LY6125616-25		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t_{RC}	12	-	15	-	20	-	25	-	ns
Address Access Time	t_{AA}	-	12	-	15	-	20	-	25	ns
Chip Enable Access Time	t_{ACE}	-	12	-	15	-	20	-	25	ns
Output Enable Access Time	t_{OE}	-	6	-	7	-	8	-	9	ns
Chip Enable to Output in Low-Z	t_{CLZ}^*	3	-	4	-	4	-	4	-	ns
Output Enable to Output in Low-Z	t_{OLZ}^*	0	-	0	-	0	-	0	-	ns
Chip Disable to Output in High-Z	t_{CHZ}^*	-	6	-	7	-	8	-	9	ns
Output Disable to Output in High-Z	t_{OHZ}^*	-	6	-	7	-	8	-	9	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	3	-	3	-	ns
LB#, UB# Access Time	t_{BA}	-	6	-	7	-	8	-	9	ns
LB#, UB# to High-Z Output	t_{BHZ}^*	-	6	-	7	-	8	-	9	ns
LB#, UB# to Low-Z Output	t_{BLZ}^*	4	-	4	-	4	-	4	-	ns

(2) WRITE CYCLE

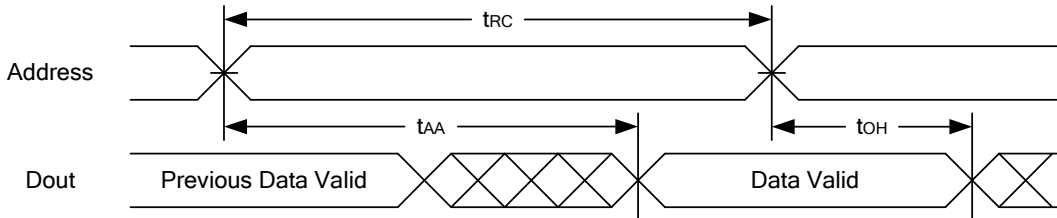
PARAMETER	SYM.	LY6125616-12		LY6125616-15		LY6125616-20		LY6125616-25		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t_{WC}	12	-	15	-	20	-	25	-	ns
Address Valid to End of Write	t_{AW}	8	-	12	-	16	-	20	-	ns
Chip Enable to End of Write	t_{CW}	8	-	12	-	16	-	20	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	8	-	10	-	11	-	12	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	0	-	ns
Data to Write Time Overlap	t_{DW}	6	-	8	-	9	-	10	-	ns
Data Hold from End of Write Time	t_{DH}	0	-	0	-	0	-	0	-	ns
Output Active from End of Write	t_{OW}^*	3	-	4	-	5	-	6	-	ns
Write to Output in High-Z	t_{WHZ}^*	-	6	-	8	-	9	-	10	ns
LB#, UB# Valid to End of Write	t_{BW}	8	-	12	-	16	-	20	-	ns

*These parameters are guaranteed by device characterization, but not production tested.

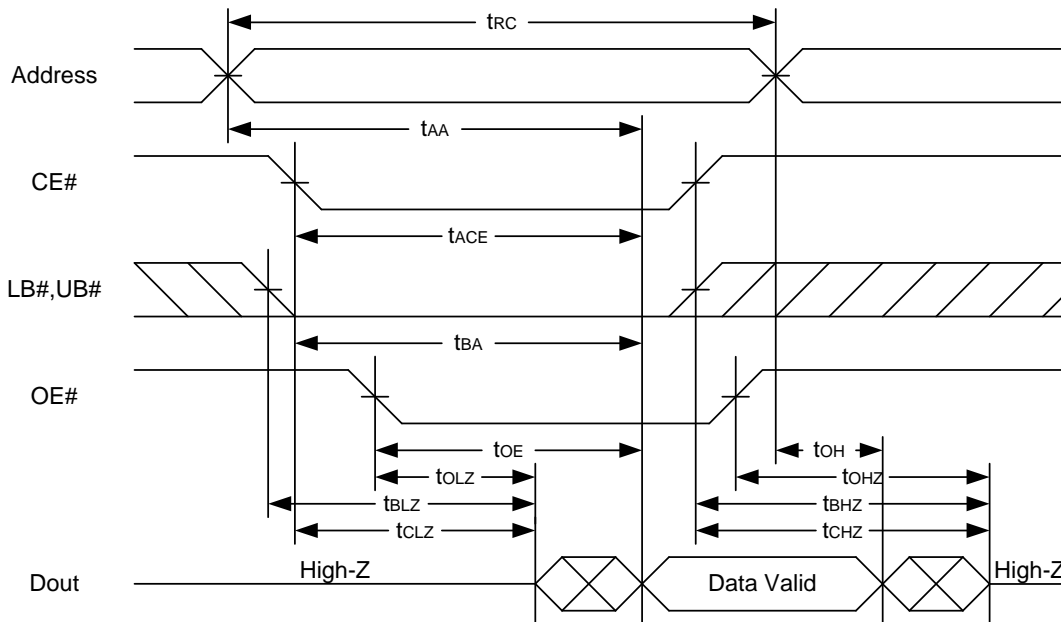


TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)



READ CYCLE 2 (CE# and OE# Controlled) (1,3,4,5)

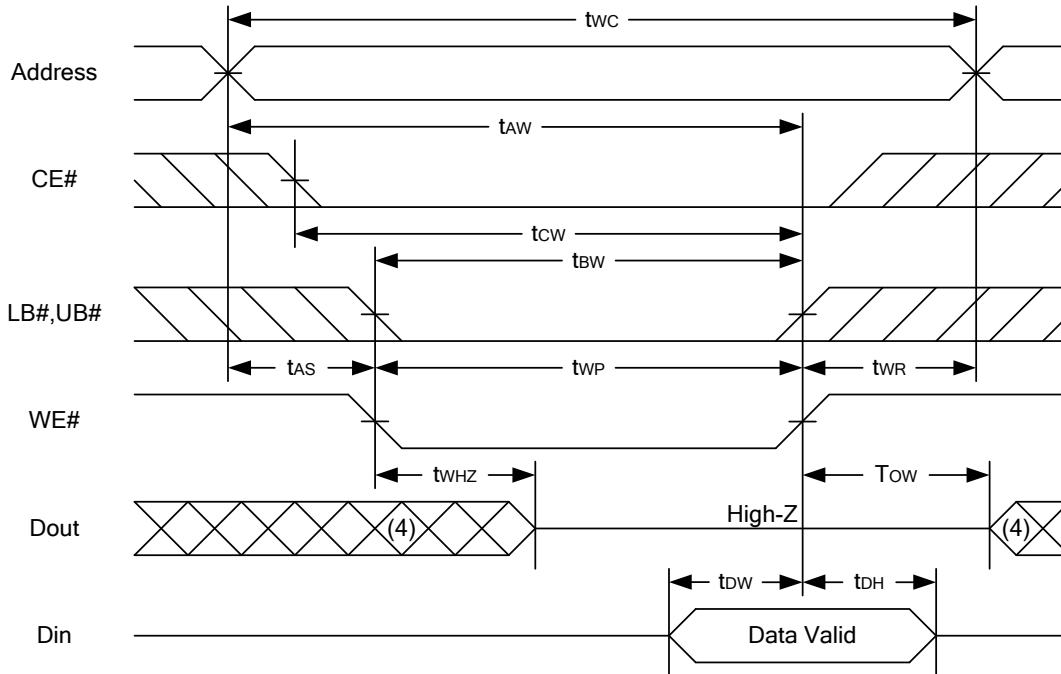


Notes :

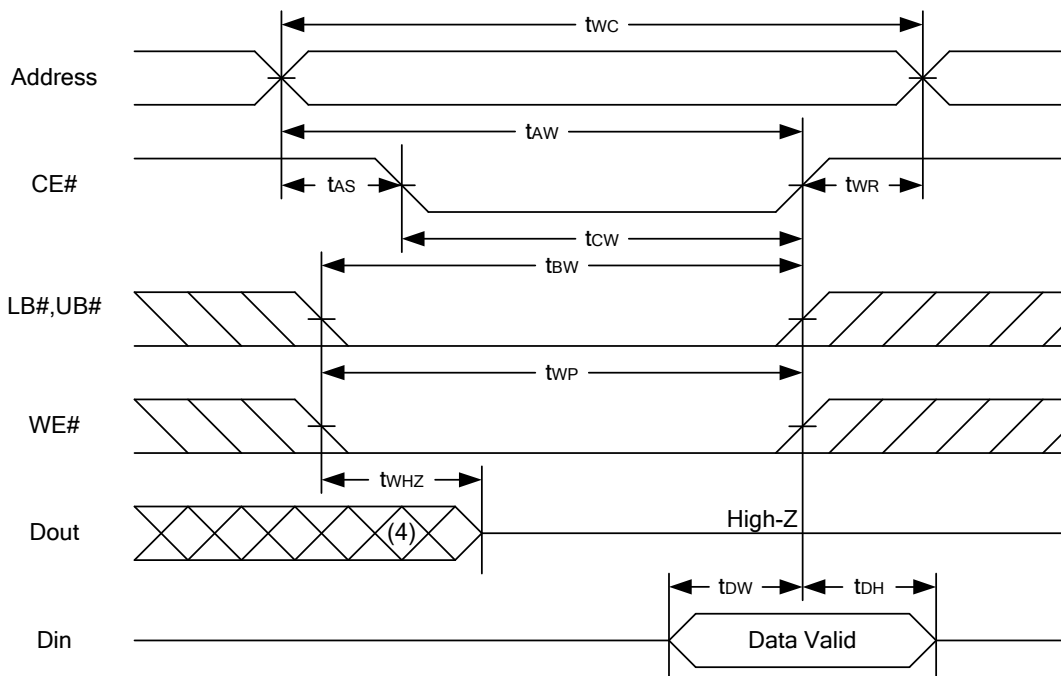
1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low, LB# or UB# = low.
3. Address must be valid prior to or coincident with CE# = low, LB# or UB# = low transition; otherwise t_{AA} is the limiting parameter.
4. t_{CLZ} , t_{BLZ} , t_{OLZ} , t_{CHZ} , t_{BHZ} and t_{OHZ} are specified with $C_L = 5pF$. Transition is measured $\pm 500mV$ from steady state.
5. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{BHZ} is less than t_{BLZ} , t_{OHZ} is less than t_{OLZ} .



WRITE CYCLE 1 (WE# Controlled) (1,2,3,5,6)

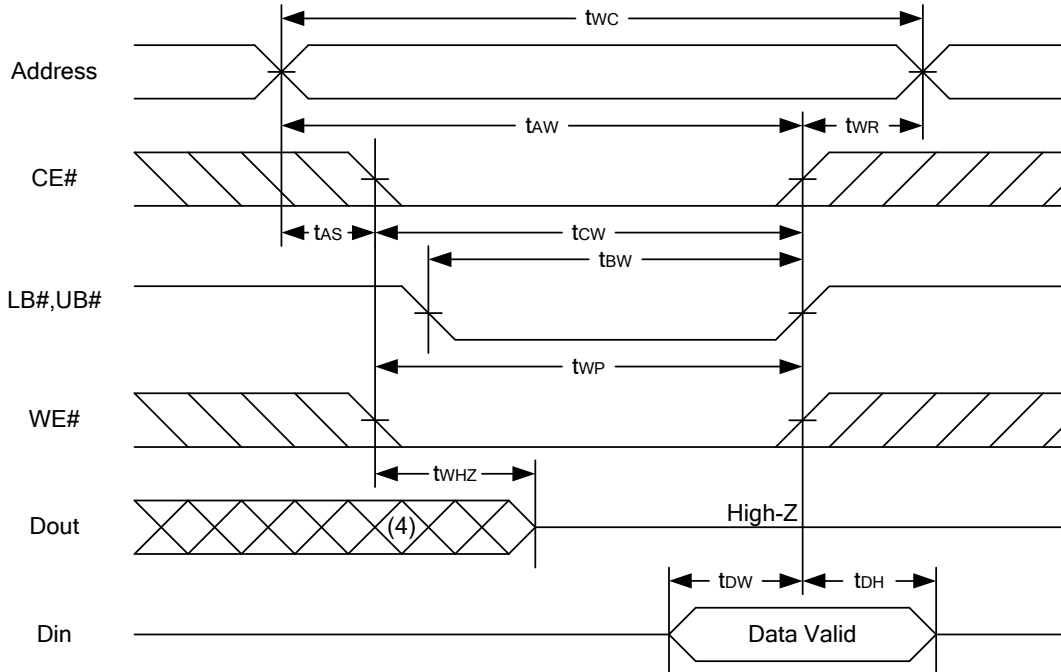


WRITE CYCLE 2 (CE# Controlled) (1,2,5,6)





WRITE CYCLE 3 (LB#,UB# Controlled) (1,2,5,6)



Notes :

1. WE#, CE#, LB#, UB# must be high during all address transitions.
2. A write occurs during the overlap of a low CE#, low WE#, LB# or UB# = low.
3. During a WE# controlled write cycle with OE# low, tWP must be greater than tWHZ + tDW to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the CE#, LB#, UB# low transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
6. tDW and tWHZ are specified with CL = 5pF. Transition is measured ±500mV from steady state.

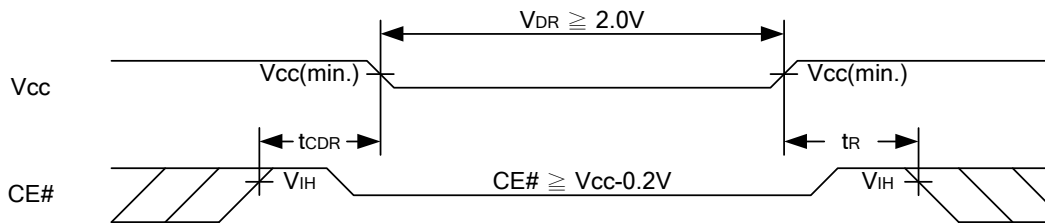


DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Vcc for Data Retention	V _{DR}	CE# ≥ V _{CC} - 0.2V	2.0	-	5.5	V
Data Retention Current	I _{DR}	V _{CC} = 2.0V	-	-	10	mA
		CE# ≥ V _{CC} - 0.2V	-	0.05	2	mA
		other pins at 0.2V or V _{CC} -0.2V	-	10	50	μA
Chip Disable to Data Retention Time	t _{CDR}	See Data Retention Waveforms (below)	0	-	-	ns
Recovery Time	t _R		t _{RC} *	-	-	ns

*t_{RC} = Read Cycle Time

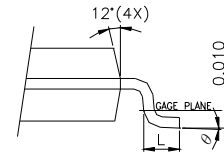
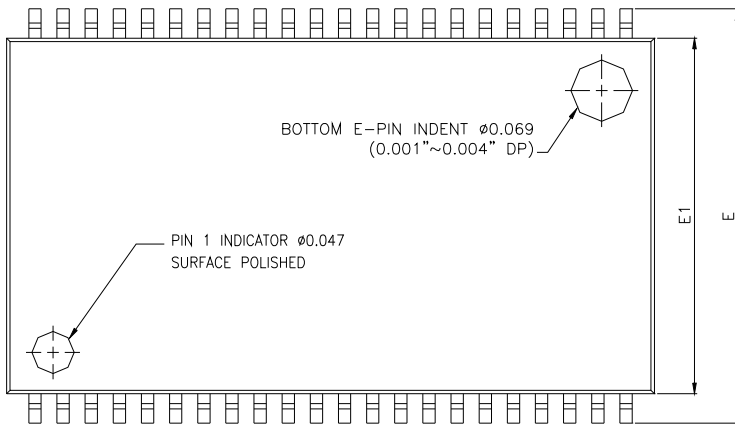
DATA RETENTION WAVEFORM



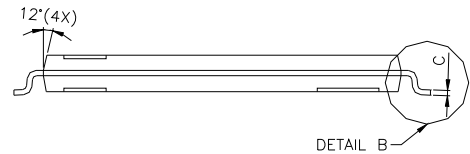
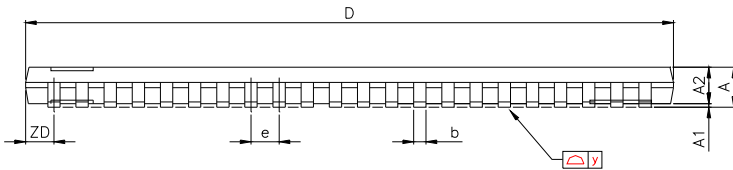


PACKAGE OUTLINE DIMENSION

44-pin 400mil TSOP-II Package Outline Dimension



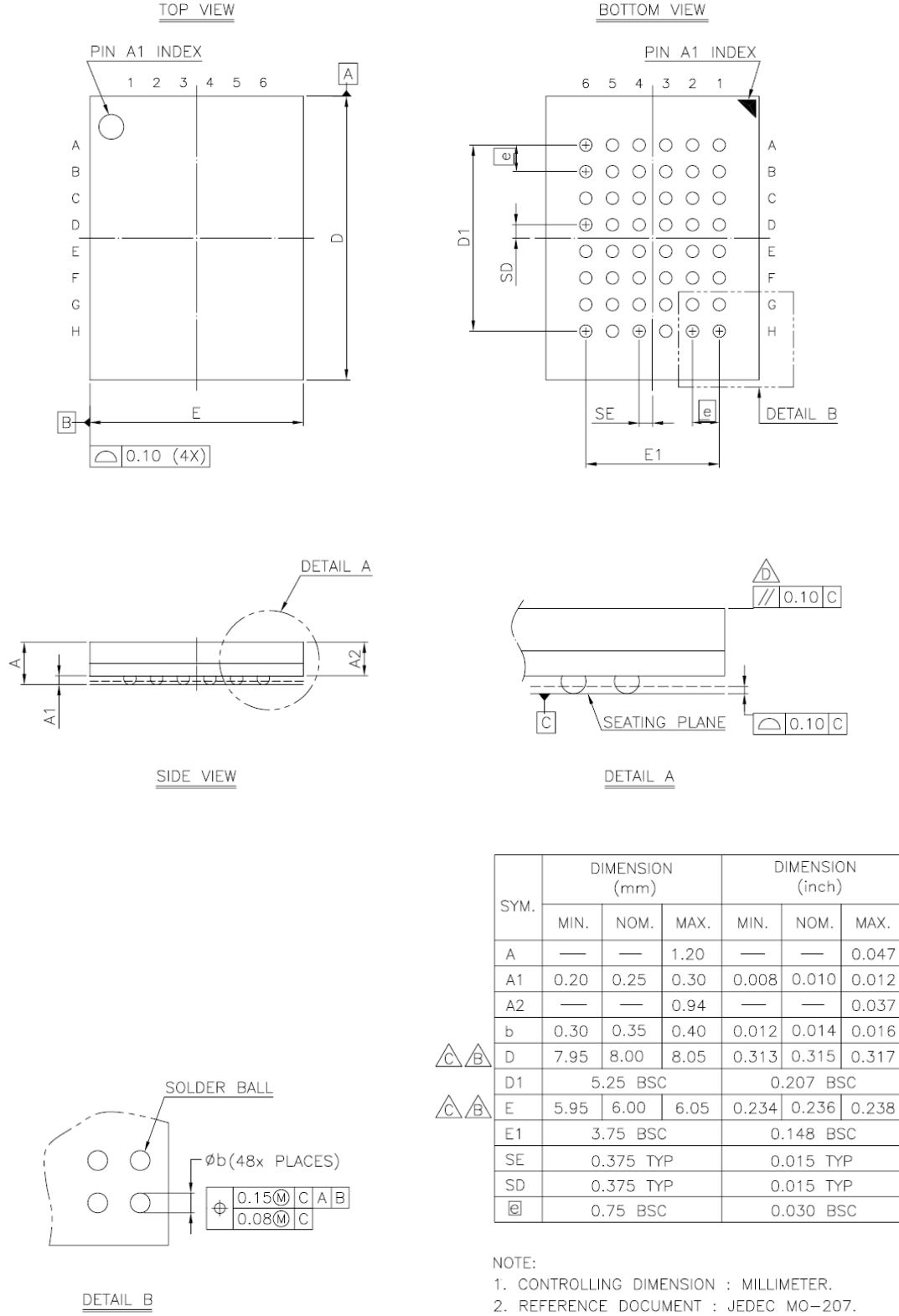
DETAIL B



DETAIL B

SYMBOLS	DIMENSIONS IN MILLMETERS			DIMENSIONS IN MILS		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	-	-	1.20	-	-	47.2
A1	0.05	0.10	0.15	2.0	3.9	5.9
A2	0.95	1.00	1.05	37.4	39.4	41.3
b	0.30	-	0.45	11.8	-	17.7
c	0.12	-	0.21	4.7	-	8.3
D	18.212	18.415	18.618	717	725	733
E	11.506	11.760	12.014	453	463	473
E1	9.957	10.160	10.363	392	400	408
e	-	0.800	-	-	31.5	-
L	0.40	0.50	0.60	15.7	19.7	23.6
ZD	-	0.805	-	-	31.7	-
y	-	-	0.076	-	-	3
θ	0°	3°	6°	0°	3°	6°

48-ball 6mm x 8mm TFBGA Package Outline Dimension





ORDERING INFORMATION

LY6125616 U V - WW XX Y Z

Z : Packing Type

Blank : Tube or Tray
Tray : 44-pin 400 mil TSOP-II
48-ball 6 mm x 8 mm TFBGA
T : Tape Reel

Y : Temperature Range

Blank : (Commercial) 0°C ~ 70°C
E : (Extended) -20°C ~ +80°C
I : (Industrial) -40°C ~ +85°C

XX : Power Type

LL : Ultra Low Power

WW : Access Time(Speed)

V : Lead Information

L : Green Package

U : Package Type

M : 44-pin 400 mil TSOP-II
G : 48-ball 6 mm x 8 mm TFBGA



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LY6125616

Rev. 2.3

5V 256K X 16 BIT HIGH SPEED CMOS SRAM

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