



REVISION HISTORY

| <u>Revision</u> | <u>Description</u> | <u>Issue Date</u> |
|-----------------|--|-------------------|
| Rev. 0.1 | Preliminary | Apr.19.2006 |
| Rev. 0.2 | Deleted I _{SB} Spec. | May.24.2006 |
| Rev. 0.3 | Deleted -10/-12/-15 Spec. | May.13.2007 |
| Rev. 0.4 | Revised Test Condition of I _{CC} /I _{SB1} /I _{DR} Revised V _{TERM} to V _{T1} and V _{T2} Revised FEATURES & ORDERING INFORMATION <u>Lead free and green package available to Green package available</u> | Apr.17.2009 |
| | Deleted T _{SOLDER} in <u>ABSOLUTE MAXIMUM RATINGS</u> Added packing type in <u>ORDERING INFORMATION</u> | |
| Rev. 0.5 | Added I grade | Apr.27.2010 |
| Rev. 0.6 | Revised <u>ORDERING INFORMATION</u> in page 9 | Aug.25.2010 |



FEATURES

- Fast access time : 20/25ns
- **Very low power consumption:**
Operating current(Normal version):
110/90mA(TYP.)
Operating current(20/25ns LL version):
40/35mA(TYP.)
- Standby current(Normal version):
0.5mA(TYP.)
Standby current(20/25ns LL version):
10µA(TYP.)
- Single 3.3V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data retention voltage : 2.0V (MIN.)
- **Green package available**
- Package : 44-pin 400 mil TSOP-II

GENERAL DESCRIPTION

The LY61L2568 is a 2,097,152-bit low power CMOS static random access memory organized as 262,144 words by 8 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

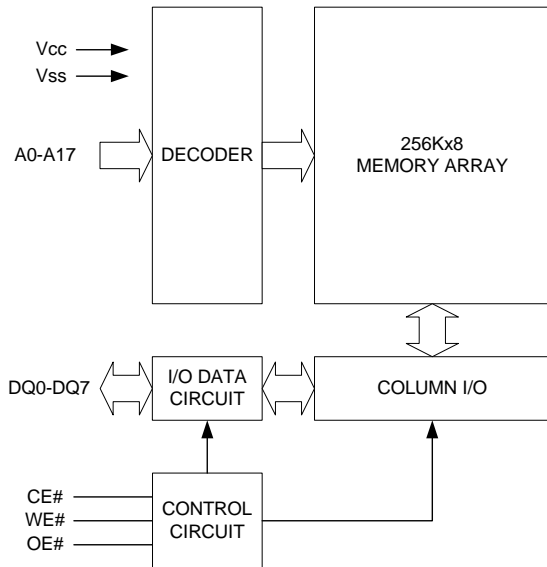
The LY61L2568 is well designed for very low power system applications, and particularly well suited for battery back-up nonvolatile memory application.

The LY61L2568 operates from a single power supply of 3.3V and all inputs and outputs are fully TTL compatible

PRODUCT FAMILY

| Product Family | Operating Temperature | Vcc Range | Speed | Power Dissipation | |
|----------------|-----------------------|------------|---------|--------------------|---------------------|
| | | | | Standby(IsB1,TYP.) | Operating(Icc,TYP.) |
| LY61L2568 | 0 ~ 70°C | 3.0 ~ 3.6V | 20/25ns | 0.5mA | 110/90mA |
| LY61L2568(I) | -20 ~ 80°C | 3.0 ~ 3.6V | 20/25ns | 0.5mA | 110/90mA |
| LY61L2568(I) | -40 ~ 85°C | 3.0 ~ 3.6V | 20/25ns | 0.5mA | 110/90mA |
| LY61L2568(LL) | 0 ~ 70°C | 3.0 ~ 3.6V | 20/25ns | 10µA(LL) | 40/35mA(LL) |
| LY61L2568(LLE) | -20 ~ 80°C | 3.0 ~ 3.6V | 20/25ns | 10µA(LL) | 40/35mA(LL) |
| LY61L2568(LLI) | -40 ~ 85°C | 3.0 ~ 3.6V | 20/25ns | 10µA(LL) | 40/35mA(LL) |

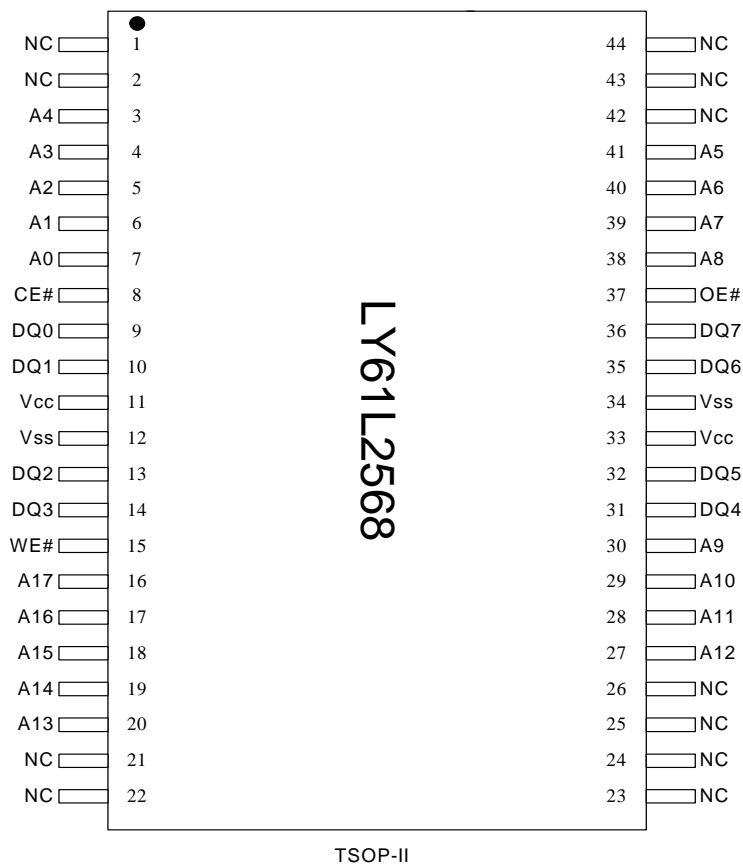
FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

| SYMBOL | DESCRIPTION |
|-----------|---------------------|
| A0 - A17 | Address Inputs |
| DQ0 – DQ7 | Data Inputs/Outputs |
| CE# | Chip Enable Inputs |
| WE# | Write Enable Input |
| OE# | Output Enable Input |
| Vcc | Power Supply |
| Vss | Ground |
| NC | No Connection |

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS*

| PARAMETER | SYMBOL | RATING | UNIT |
|--|------------------|------------------------------|------|
| Voltage on Vcc relative to Vss | V _{T1} | -0.5 to 4.6 | V |
| Voltage on any other pin relative to Vss | V _{T2} | -0.5 to V _{cc} +0.5 | V |
| Operating Temperature | T _A | 0 to 70(C grade) | °C |
| | | -20 to 80(E grade) | |
| | | -40 to 85(I grade) | |
| Storage Temperature | T _{STG} | -65 to 150 | °C |
| Power Dissipation | P _D | 1 | W |
| DC Output Current | I _{OUT} | 50 | mA |

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

| MODE | CE# | OE# | WE# | I/O OPERATION | SUPPLY CURRENT |
|----------------|-----|-----|-----|------------------|------------------|
| Standby | H | X | X | High-Z | I _{SB1} |
| Output Disable | L | H | H | High-Z | I _{cc} |
| Read | L | L | H | D _{OUT} | I _{cc} |
| Write | L | X | L | D _{IN} | I _{cc} |

Note: H = V_{IH}, L = V_{IL}, X = Don't care.

DC ELECTRICAL CHARACTERISTICS

| PARAMETER | SYMBOL | TEST CONDITION | MIN. | TYP. ⁴ | MAX. | UNIT | |
|--|------------------------------|---|---------|-------------------|----------------------|-----------------|----|
| Supply Voltage | V _{cc} | | 3.0 | 3.3 | 3.6 | V | |
| Input High Voltage | V _{IH} ¹ | | 2.2 | - | V _{cc} +0.3 | V | |
| Input Low Voltage | V _{IL} ² | | -0.3 | - | 0.6 | V | |
| Input Leakage Current | I _{LI} | V _{cc} ≥ V _{IN} ≥ V _{ss} | -1 | - | 1 | μA | |
| Output Leakage Current | I _{LO} | V _{cc} ≥ V _{OUT} ≥ V _{ss} , Output Disabled | -1 | - | 1 | μA | |
| Output High Voltage | V _{OH} | I _{OH} = -1mA | 2.4 | - | - | V | |
| Output Low Voltage | V _{OL} | I _{OL} = 2mA | - | - | 0.4 | V | |
| Average Operating Power supply Current | I _{cc} | Cycle time = Min. CE# = V _{IL} , I _{I/O} = 0mA Others at V _{IL} or V _{IH} | 20 | - | 110 | 150 | mA |
| | | | 25 | - | 90 | 115 | mA |
| | | | 20LL | - | 40 | 50 | mA |
| | | | 25LL | - | 35 | 45 | mA |
| Standby Power Supply Current | I _{SB1} | CE# ≥ V _{cc} - 0.2V Others at 0.2V or V _{cc} - 0.2V | Normal | - | 0.5 | 5 ⁵ | mA |
| | | | 20/25LL | - | 10 | 50 ⁶ | μA |

Notes:

- V_{IH}(max) = V_{cc} + 3.0V for pulse width less than 10ns.
- V_{IL}(min) = V_{ss} - 3.0V for pulse width less than 10ns.
- Over/Undershoot specifications are characterized, not 100% tested.
- Typical values are included for reference only and are not guaranteed or tested.
Typical values are measured at V_{cc} = V_{cc}(TYP.) and T_A = 25°C
- 1mA for special request
- 20μA for special request

**CAPACITANCE (T_A = 25°C, f = 1.0MHz)**

| PARAMETER | SYMBOL | MIN. | MAX | UNIT |
|--------------------------|------------------|------|-----|------|
| Input Capacitance | C _{IN} | - | 8 | pF |
| Input/Output Capacitance | C _{I/O} | - | 10 | pF |

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

| | |
|--|--|
| Input Pulse Levels | 0.2V to V _{CC} - 0.2V |
| Input Rise and Fall Times | 3ns |
| Input and Output Timing Reference Levels | 1.5V |
| Output Load | C _L = 30pF + 1TTL, I _{OH} /I _{OL} = -8mA/16mA |

AC ELECTRICAL CHARACTERISTICS**(1) READ CYCLE**

| PARAMETER | SYM. | LY61L2568-20 | | LY61L2568-25 | | UNIT |
|------------------------------------|--------------------|--------------|------|--------------|------|------|
| | | MIN. | MAX. | MIN. | MAX. | |
| Read Cycle Time | t _{RC} | 20 | - | 25 | - | ns |
| Address Access Time | t _{AA} | - | 20 | - | 25 | ns |
| Chip Enable Access Time | t _{ACE} | - | 20 | - | 25 | ns |
| Output Enable Access Time | t _{OE} | - | 8 | - | 9 | ns |
| Chip Enable to Output in Low-Z | t _{CLZ} * | 4 | - | 4 | - | N`s |
| Output Enable to Output in Low-Z | t _{OLZ} * | 0 | - | 0 | - | ns |
| Chip Disable to Output in High-Z | t _{CHZ} * | - | 8 | - | 9 | ns |
| Output Disable to Output in High-Z | t _{OHZ} * | - | 8 | - | 9 | ns |
| Output Hold from Address Change | t _{OH} | 3 | - | 3 | - | ns |

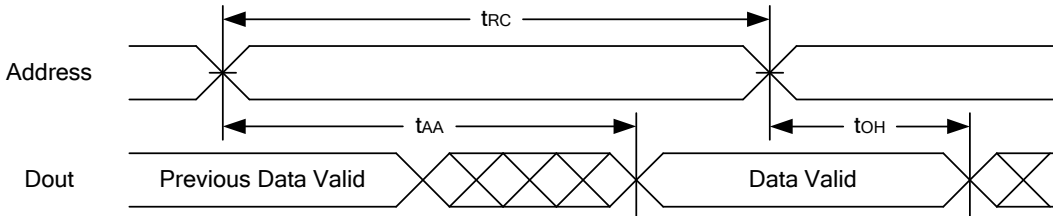
(2) WRITE CYCLE

| PARAMETER | SYM. | LY61L2568-20 | | LY61L2568-25 | | UNIT |
|----------------------------------|--------------------|--------------|------|--------------|------|------|
| | | MIN. | MAX. | MIN. | MAX. | |
| Write Cycle Time | t _{WC} | 20 | - | 25 | - | ns |
| Address Valid to End of Write | t _{AW} | 16 | - | 20 | - | ns |
| Chip Enable to End of Write | t _{CW} | 16 | - | 20 | - | ns |
| Address Set-up Time | t _{AS} | 0 | - | 0 | - | ns |
| Write Pulse Width | t _{WP} | 11 | - | 12 | - | ns |
| Write Recovery Time | t _{WR} | 0 | - | 0 | - | ns |
| Data to Write Time Overlap | t _{DW} | 9 | - | 10 | - | ns |
| Data Hold from End of Write Time | t _{DH} | 0 | - | 0 | - | ns |
| Output Active from End of Write | t _{OW} * | 5 | - | 6 | - | ns |
| Write to Output in High-Z | t _{WHZ} * | - | 9 | - | 10 | ns |

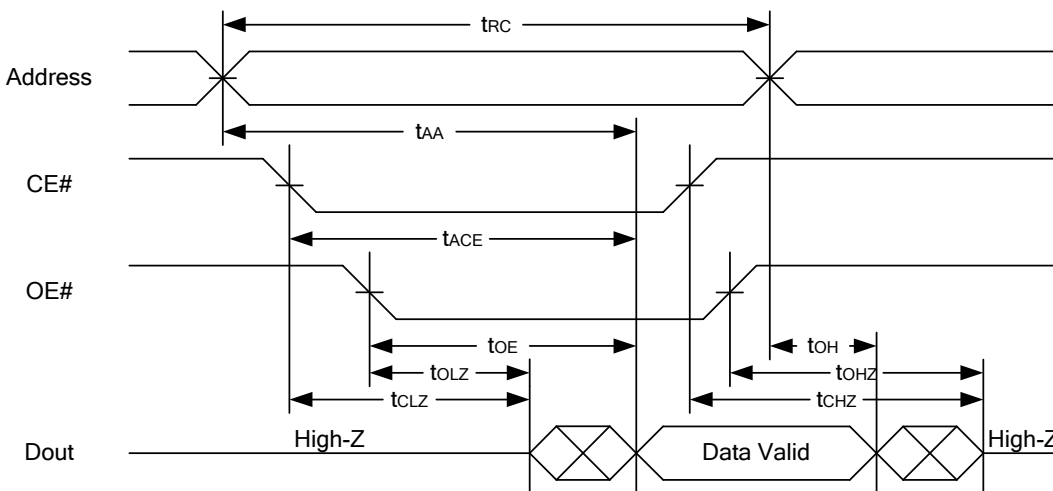
*These parameters are guaranteed by device characterization, but not production tested.

TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)

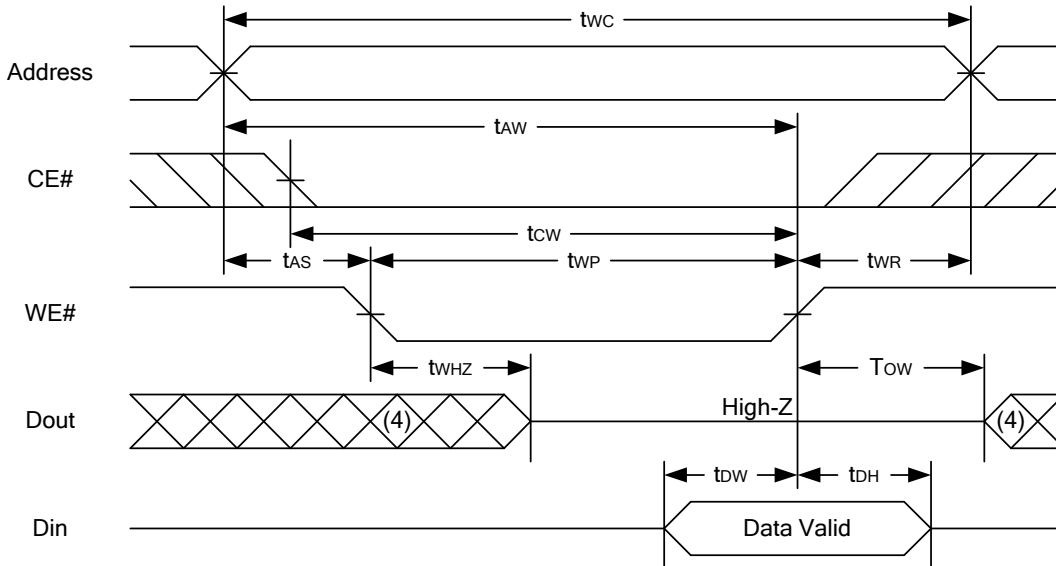
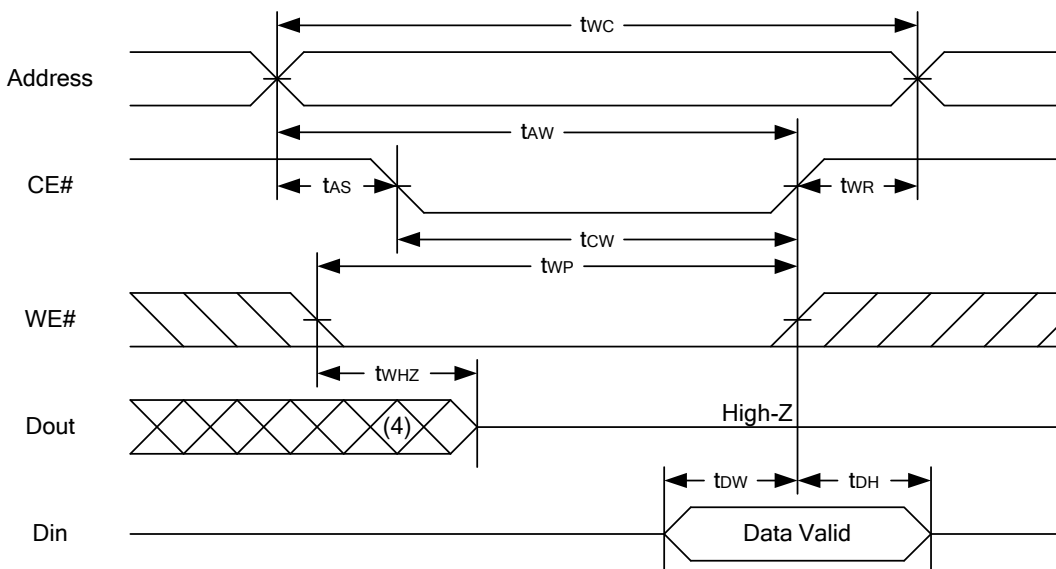


READ CYCLE 2 (CE# and OE# Controlled) (1,3,4,5)



Notes :

1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low.
3. Address must be valid prior to or coincident with CE# = low; otherwise t_{AA} is the limiting parameter.
4. t_{CLZ} , t_{OLZ} , t_{CHZ} and t_{OHZ} are specified with $C_L = 5pF$. Transition is measured $\pm 500mV$ from steady state.
5. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{OHZ} is less than t_{OLZ} .

WRITE CYCLE 1 (WE# Controlled) (1,2,3,5,6)

WRITE CYCLE 2 (CE# Controlled) (1,2,5,6)

Notes :

1. WE#, CE# must be high during all address transitions.
2. A write occurs during the overlap of a low CE#, low WE#.
3. During a WE# controlled write cycle with OE# low, twp must be greater than twhz + tdw to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the CE# low transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
6. tow and twhz are specified with CL = 5pF. Transition is measured ±500mV from steady state.

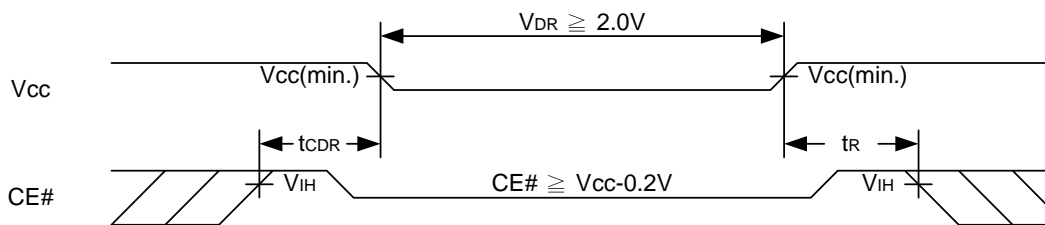


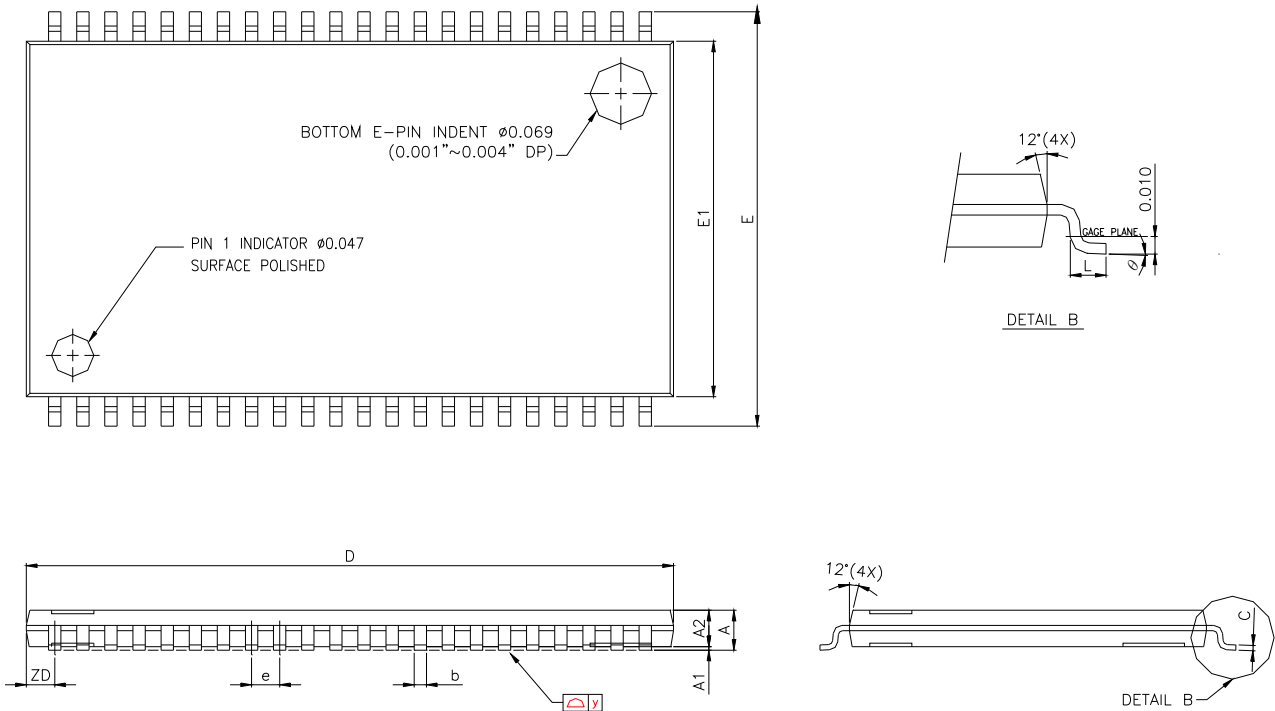
DATA RETENTION CHARACTERISTICS

| PARAMETER | SYMBOL | TEST CONDITION | MIN. | TYP. | MAX. | UNIT | |
|-------------------------------------|------------------|--|------------------|------|------|------|----|
| Vcc for Data Retention | V _{DR} | CE# ≥ V _{CC} - 0.2V | 2.0 | - | 3.6 | V | |
| Data Retention Current | I _{DR} | V _{CC} = 2.0V CE# ≥ V _{CC} - 0.2V | Normal | - | 0.5 | 1 | mA |
| | | Others at 0.2V or V _{CC} - 0.2V | 20/25LL | - | 5 | 40 | μA |
| Chip Disable to Data Retention Time | t _{CDR} | See Data Retention Waveforms (below) | 0 | - | - | ns | |
| Recovery Time | t _R | | t _{RC*} | - | - | ns | |

t_{RC*} = Read Cycle Time

DATA RETENTION WAVEFORM



PACKAGE OUTLINE DIMENSION
44-pin 400mil TSOP-II Package Outline Dimension


| SYMBOLS | DIMENSIONS IN MILLMETERS | | | DIMENSIONS IN MILS | | |
|---------|--------------------------|--------|--------|--------------------|------|------|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | - | - | 1.20 | - | - | 47.2 |
| A1 | 0.05 | 0.10 | 0.15 | 2.0 | 3.9 | 5.9 |
| A2 | 0.95 | 1.00 | 1.05 | 37.4 | 39.4 | 41.3 |
| b | 0.30 | - | 0.45 | 11.8 | - | 17.7 |
| c | 0.12 | - | 0.21 | 4.7 | - | 8.3 |
| D | 18.212 | 18.415 | 18.618 | 717 | 725 | 733 |
| E | 11.506 | 11.760 | 12.014 | 453 | 463 | 473 |
| E1 | 9.957 | 10.160 | 10.363 | 392 | 400 | 408 |
| e | - | 0.800 | - | - | 31.5 | - |
| L | 0.40 | 0.50 | 0.60 | 15.7 | 19.7 | 23.6 |
| ZD | - | 0.805 | - | - | 31.7 | - |
| y | - | - | 0.076 | - | - | 3 |
| θ | 0° | 3° | 6° | 0° | 3° | 6° |



ORDERING INFORMATION

LY61L2568 U V - WW XX Y Z

Z : Packing Type

| |
|-------------------------------|
| Blank : Tube or Tray |
| Tray : 44-pin 400 mil TSOP-II |
| T : Tape Reel |

Y : Temperature Range

| |
|---------------------------------|
| Blank : (Commercial) 0°C ~ 70°C |
| E : (Extended) -20°C ~ +80°C |
| I : (Industrial) -40°C ~ +85°C |

XX : Power Type LL : Ultra Low Power

WW : Access Time(Speed)

V : Lead Information L : Green Package

U : Package Type M : 44-pin 400 mil TSOP-II



®

Lyontek Inc.

LY61L2568

Rev. 0.6

256K X 8 BIT HIGH SPEED CMOS SRAM

THIS PAGE IS LEFT BLANK INTENTIONALLY.