



### REVISION HISTORY

<u>Revision</u>	<u>Description</u>	<u>Issue Date</u>
Rev. 0.1	Initial Issue	Sep.25.2008
Rev. 0.2	Revised <b>FEATURES &amp; ORDERING INFORMATION</b> <b>Lead free and green package available</b> to <b>Green package available</b> Added packing type in <b>ORDERING INFORMATION</b> Deleted T <sub>SOLDER</sub> in <b>ABSOLUTE MAXIMUM RATINGS</b> Added PKG type : 48 TFBGA	May.20.2009
Rev. 0.3	Revised V <sub>DR</sub>	Sep.11.2009
Rev. 0.4	Revised <b>ORDERING INFORMATION</b> in page 11	Aug.25.2010

### FEATURES

- Fast access time : 55/70ns
- Low power consumption:  
Operating current : 45/30mA (TYP.)  
Standby current : 10 $\mu$ A (TYP.) LL-version
- Single 4.5V ~ 5.5V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data byte control : LB# (DQ0 ~ DQ7)  
UB# (DQ8 ~ DQ15)
- Data retention voltage : 1.5V (MIN.)
- **Green package available**
- Package : 48-pin 12mm x 20mm TSOP-I  
48-ball 6mm x 8mm TFBGA

### GENERAL DESCRIPTION

The LY62102516 is a 16,777,216-bit low power CMOS static random access memory organized as 1,048,576 words by 16 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

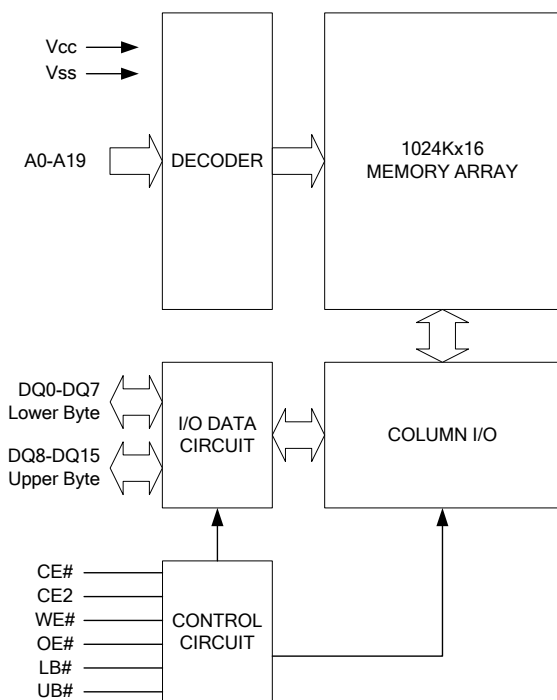
The LY62102516 is well designed for low power application, and particularly well suited for battery back-up nonvolatile memory application.

The LY62102516 operates from a single power supply of 4.5V ~ 5.5V and all inputs and outputs are fully TTL compatible

### PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation	
				Standby(Isb1,TYP.)	Operating(Icc,TYP.)
LY62102516	0 ~ 70°C	4.5 ~ 5.5V	55/70ns	10 $\mu$ A(LL)	45/30mA
LY62102516(E)	-20 ~ 80°C	4.5 ~ 5.5V	55/70ns	10 $\mu$ A(LL)	45/30mA
LY62102516(I)	-40 ~ 85°C	4.5 ~ 5.5V	55/70ns	10 $\mu$ A(LL)	45/30mA

### FUNCTIONAL BLOCK DIAGRAM

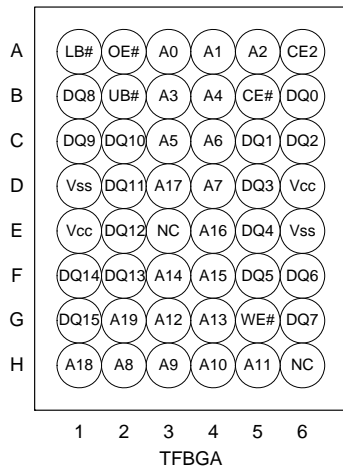
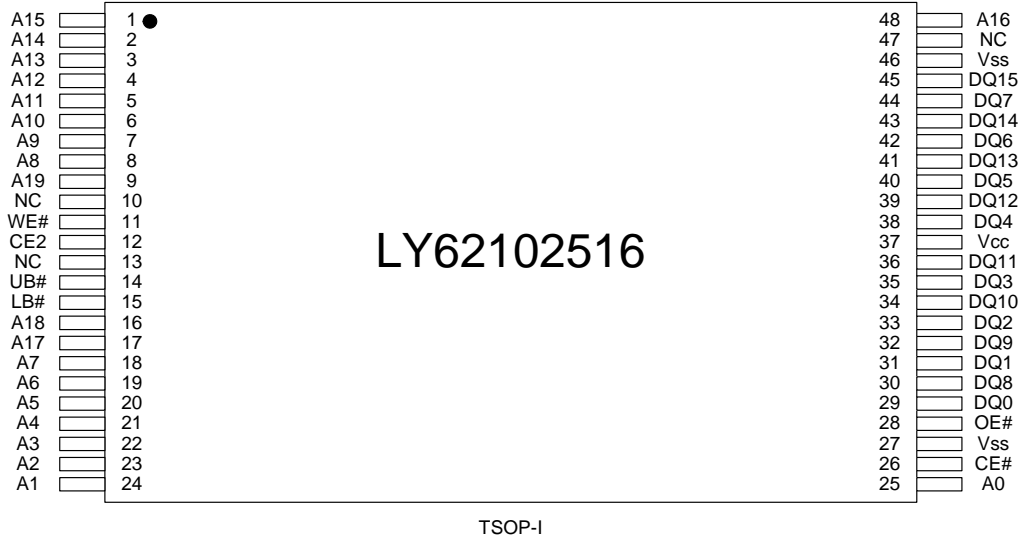


### PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A19	Address Inputs
DQ0 - DQ15	Data Inputs/Outputs
CE#, CE2	Chip Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
LB#	Lower Byte Control
UB#	Upper Byte Control
Vcc	Power Supply
Vss	Ground



### PIN CONFIGURATION



### ABSOLUTE MAXIMUM RATINGS\*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on Vcc relative to Vss	VT1	-0.5 to 6.5	V
Voltage on any other pin relative to Vss	VT2	-0.5 to Vcc+0.5	V
Operating Temperature	TA	0 to 70(C grade)	°C
		-20 to 80(E grade)	
		-40 to 85(I grade)	
Storage Temperature	TSTG	-65 to 150	°C
Power Dissipation	PD	1	W
DC Output Current	IOUT	50	mA

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.



### TRUTH TABLE

MODE	CE#	CE2	OE#	WE#	LB#	UB#	I/O OPERATION		SUPPLY CURRENT
							DQ0-DQ7	DQ8-DQ15	
Standby	H	X	X	X	X	X	High - Z	High - Z	I <sub>SB</sub> , I <sub>SB1</sub>
	X	L	X	X	X	X	High - Z	High - Z	
	X	X	X	X	H	H	High - Z	High - Z	
Output Disable	L	H	H	H	L	X	High - Z	High - Z	I <sub>CC</sub> , I <sub>CC1</sub>
	L	H	H	H	X	L	High - Z	High - Z	
Read	L	H	L	H	L	H	D <sub>OUT</sub>	High - Z	I <sub>CC</sub> , I <sub>CC1</sub>
	L	H	L	H	H	L	High - Z	D <sub>OUT</sub>	
	L	H	L	H	L	L	D <sub>OUT</sub>	D <sub>OUT</sub>	
Write	L	H	X	L	L	H	D <sub>IN</sub>	High - Z	I <sub>CC</sub> , I <sub>CC1</sub>
	L	H	X	L	H	L	High - Z	D <sub>IN</sub>	
	L	H	X	L	L	L	D <sub>IN</sub>	D <sub>IN</sub>	

Note: H = V<sub>IH</sub>, L = V<sub>IL</sub>, X = Don't care.

### DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP. <sup>4</sup>	MAX.	UNIT	
Supply Voltage	V <sub>CC</sub>		4.5	5.0	5.5	V	
Input High Voltage	V <sub>IH</sub> <sup>1</sup>		2.4	-	V <sub>CC</sub> +0.3	V	
Input Low Voltage	V <sub>IL</sub> <sup>2</sup>		-0.2	-	0.6	V	
Input Leakage Current	I <sub>LI</sub>	V <sub>CC</sub> ≥ V <sub>IN</sub> ≥ V <sub>SS</sub>	-1	-	1	μA	
Output Leakage Current	I <sub>LO</sub>	V <sub>CC</sub> ≥ V <sub>OUT</sub> ≥ V <sub>SS</sub> Output Disabled	-1	-	1	μA	
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -1mA	2.4	-	-	V	
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2mA	-	-	0.4	V	
Average Operating Power supply Current	I <sub>CC</sub>	Cycle time = Min. CE# = V <sub>IL</sub> and CE2 = V <sub>IH</sub> I <sub>I/O</sub> = 0mA Other pins at V <sub>IL</sub> or V <sub>IH</sub>	-55	-	45	60	mA
			-70	-	30	45	mA
	I <sub>CC1</sub>	Cycle time = 1μs CE# ≤ 0.2V and CE2 ≥ V <sub>CC</sub> -0.2V I <sub>I/O</sub> = 0mA Other pins at 0.2V or V <sub>CC</sub> -0.2V	-	-	8	16	
Standby Power Supply Current	I <sub>SB</sub>	CE# = V <sub>IH</sub> or CE2 = V <sub>IL</sub> Other pins at V <sub>IL</sub> or V <sub>IH</sub>	-	-	0.3	2	
			I <sub>SB1</sub>	CE# ≥ V <sub>CC</sub> -0.2V or CE2 ≤ 0.2V Other pins at 0.2V or V <sub>CC</sub> -0.2V	-LL	-	10
	-LLE	-			10	80	μA
	-LLI	-			10	100	μA

Notes:

- V<sub>IH</sub>(max) = V<sub>CC</sub> + 3.0V for pulse width less than 10ns.
- V<sub>IL</sub>(min) = V<sub>SS</sub> - 3.0V for pulse width less than 10ns.
- Over/Undershoot specifications are characterized, not 100% tested.
- Typical values are included for reference only and are not guaranteed or tested.  
Typical values are measured at V<sub>CC</sub> = V<sub>CC</sub>(TYP.) and T<sub>A</sub> = 25°C

**CAPACITANCE (T<sub>A</sub> = 25°C, f = 1.0MHz)**

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C <sub>IN</sub>	-	6	pF
Input/Output Capacitance	C <sub>I/O</sub>	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

**AC TEST CONDITIONS**

Input Pulse Levels	0.2V to V <sub>CC</sub> - 0.2V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	C <sub>L</sub> = 30pF + 1TTL, I <sub>OH</sub> /I <sub>OL</sub> = -1mA/2mA

**AC ELECTRICAL CHARACTERISTICS****(1) READ CYCLE**

PARAMETER	SYM.	LY62102516-55		LY62102516-70		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t <sub>RC</sub>	55	-	70	-	ns
Address Access Time	t <sub>AA</sub>	-	55	-	70	ns
Chip Enable Access Time	t <sub>ACE</sub>	-	55	-	70	ns
Output Enable Access Time	t <sub>OE</sub>	-	30	-	35	ns
Chip Enable to Output in Low-Z	t <sub>CLZ</sub> *	10	-	10	-	ns
Output Enable to Output in Low-Z	t <sub>OLZ</sub> *	5	-	5	-	ns
Chip Disable to Output in High-Z	t <sub>CHZ</sub> *	-	20	-	25	ns
Output Disable to Output in High-Z	t <sub>OHZ</sub> *	-	20	-	25	ns
Output Hold from Address Change	t <sub>OH</sub>	10	-	10	-	ns
LB#, UB# Access Time	t <sub>BA</sub>	-	55	-	70	ns
LB#, UB# to High-Z Output	t <sub>BHZ</sub> *	-	25	-	30	ns
LB#, UB# to Low-Z Output	t <sub>B LZ</sub> *	10	-	10	-	ns

**(2) WRITE CYCLE**

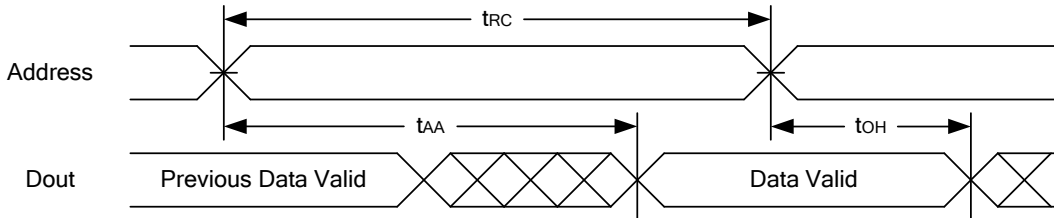
PARAMETER	SYM.	LY62102516-55		LY62102516-70		UNIT
		MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t <sub>WC</sub>	55	-	70	-	ns
Address Valid to End of Write	t <sub>AW</sub>	50	-	60	-	ns
Chip Enable to End of Write	t <sub>CW</sub>	50	-	60	-	ns
Address Set-up Time	t <sub>AS</sub>	0	-	0	-	ns
Write Pulse Width	t <sub>WP</sub>	45	-	55	-	ns
Write Recovery Time	t <sub>WR</sub>	0	-	0	-	ns
Data to Write Time Overlap	t <sub>DW</sub>	25	-	30	-	ns
Data Hold from End of Write Time	t <sub>DH</sub>	0	-	0	-	ns
Output Active from End of Write	t <sub>OW</sub> *	5	-	5	-	ns
Write to Output in High-Z	t <sub>WHZ</sub> *	-	20	-	25	ns
LB#, UB# Valid to End of Write	t <sub>BW</sub>	45	-	60	-	ns

\*These parameters are guaranteed by device characterization, but not production tested.

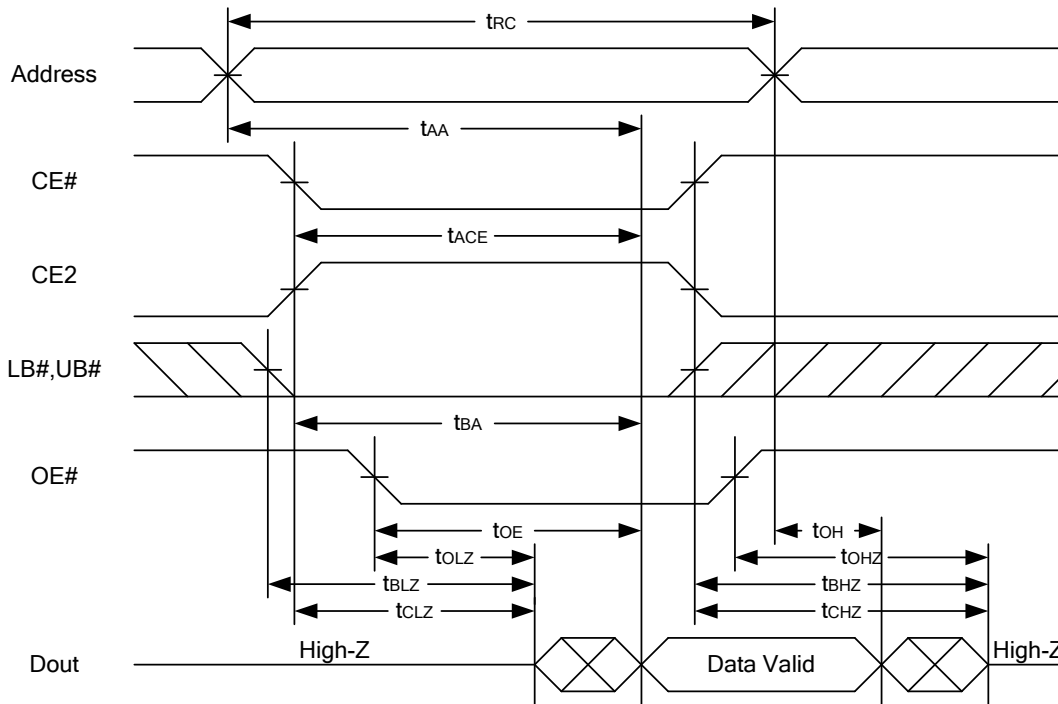


### TIMING WAVEFORMS

#### READ CYCLE 1 (Address Controlled) (1,2)



#### READ CYCLE 2 (CE# and CE2 and OE# Controlled) (1,3,4,5)

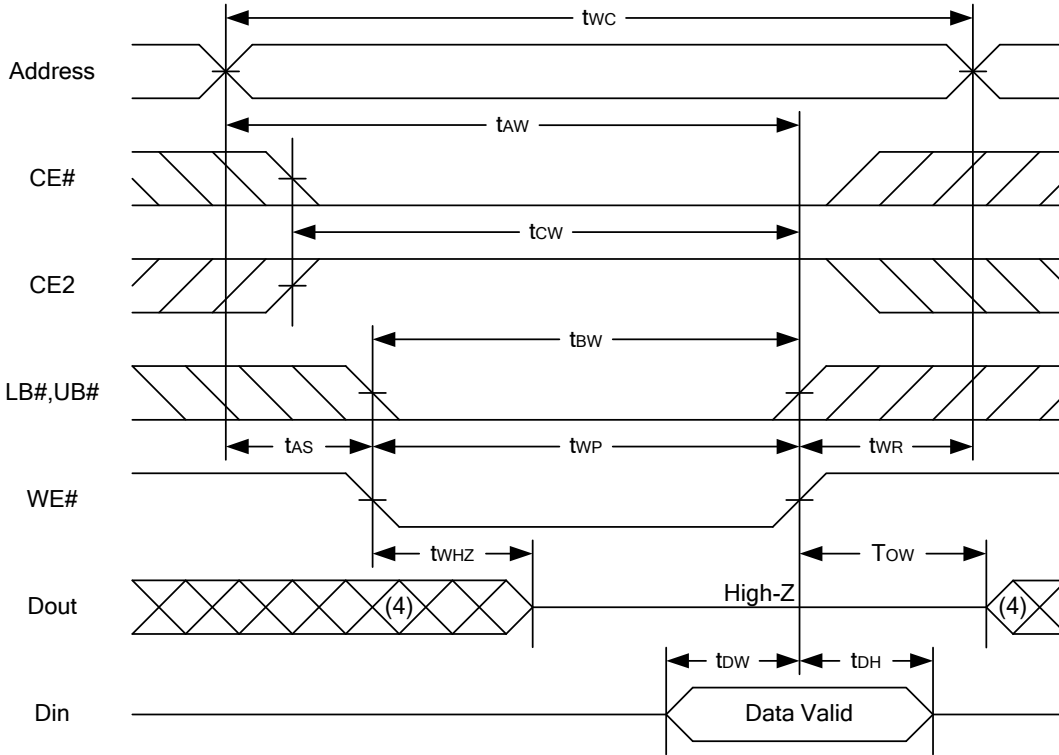


Notes :

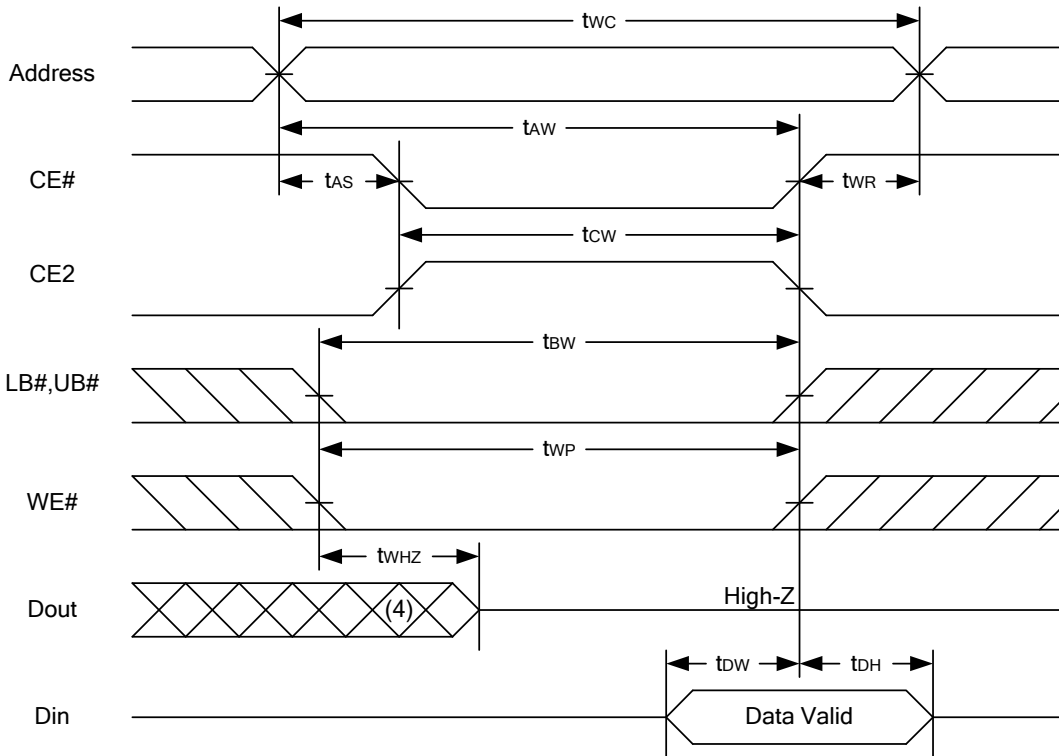
1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low, CE2 = high, LB# or UB# = low.
3. Address must be valid prior to or coincident with CE# = low, CE2 = high, LB# or UB# = low transition; otherwise  $t_{AA}$  is the limiting parameter.
4.  $t_{CLZ}$ ,  $t_{BLZ}$ ,  $t_{OLZ}$ ,  $t_{CHZ}$ ,  $t_{BZH}$  and  $t_{OZH}$  are specified with  $C_L = 5pF$ . Transition is measured  $\pm 500mV$  from steady state.
5. At any given temperature and voltage condition,  $t_{CHZ}$  is less than  $t_{CLZ}$ ,  $t_{BZH}$  is less than  $t_{BLZ}$ ,  $t_{OZH}$  is less than  $t_{OLZ}$ .



#### WRITE CYCLE 1 (WE# Controlled) (1,2,3,5,6)

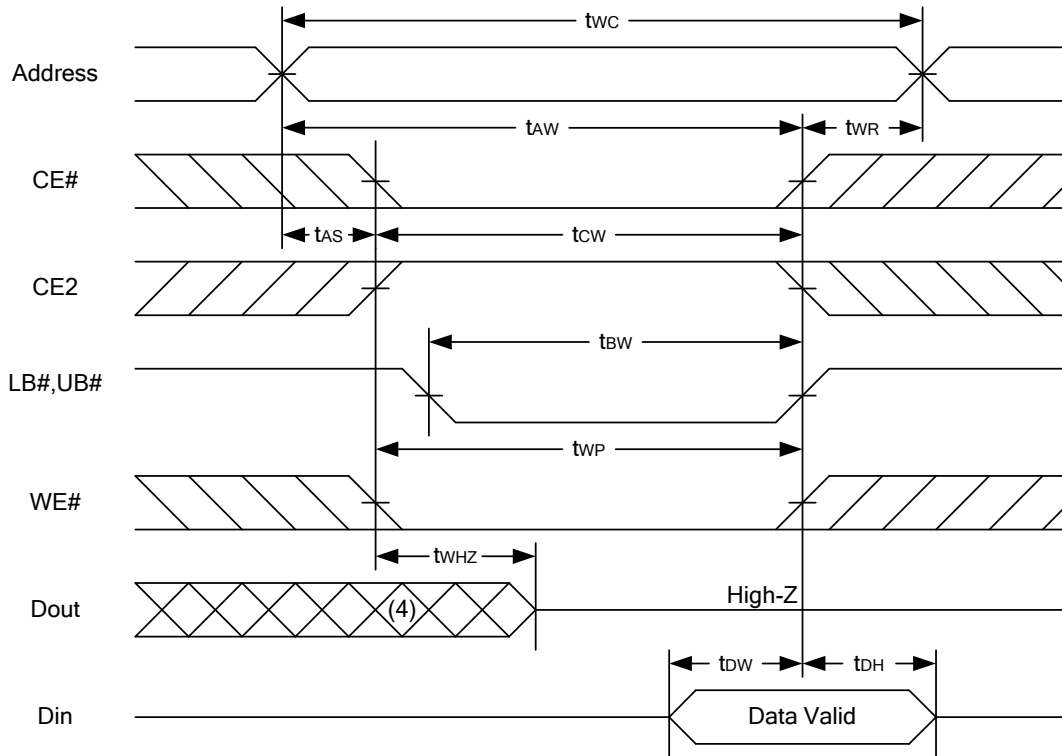


#### WRITE CYCLE 2 (CE# and CE2 Controlled) (1,2,5,6)





#### WRITE CYCLE 3 (LB#,UB# Controlled) (1,2,5,6)



Notes :

1. WE#, CE#, LB#, UB# must be high or CE2 must be low during all address transitions.
2. A write occurs during the overlap of a low CE#, high CE2, low WE#, LB# or UB# = low.
3. During a WE# controlled write cycle with OE# low, tWP must be greater than tWHZ + tDW to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the CE#, LB#, UB# low transition and CE2 high transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
6. tOW and tWHZ are specified with CL = 5pF. Transition is measured ±500mV from steady state.



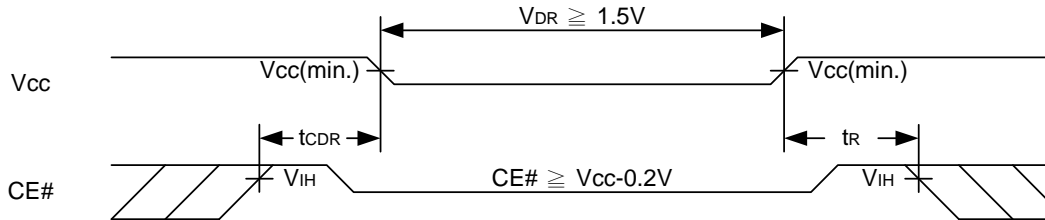
**DATA RETENTION CHARACTERISTICS**

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
V <sub>CC</sub> for Data Retention	V <sub>DR</sub>	CE# ≥ V <sub>CC</sub> - 0.2V or CE2 ≤ 0.2V	1.5	-	5.5	V	
Data Retention Current	I <sub>DR</sub>	V <sub>CC</sub> = 1.5V	-LL	-	8	50	μA
		CE# ≥ V <sub>CC</sub> -0.2V or CE2 ≤ 0.2V other pins at 0.2V or V <sub>CC</sub> -0.2V	-LLE	-	8	60	μA
			-LLI	-	8	80	μA
Chip Disable to Data Retention Time	t <sub>CDR</sub>	See Data Retention Waveforms (below)	0	-	-	ns	
Recovery Time	t <sub>R</sub>		t <sub>RC</sub> *	-	-	ns	

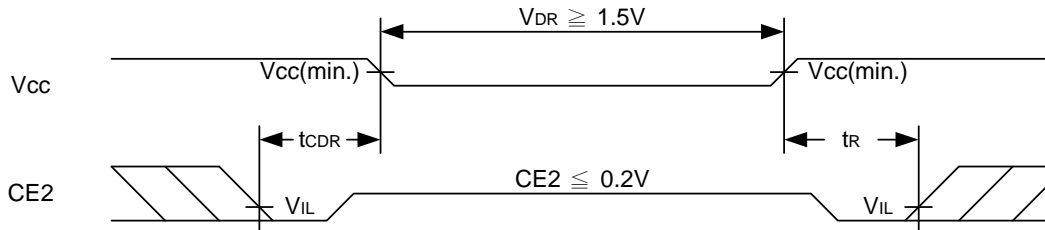
t<sub>RC</sub>\* = Read Cycle Time

**DATA RETENTION WAVEFORM**

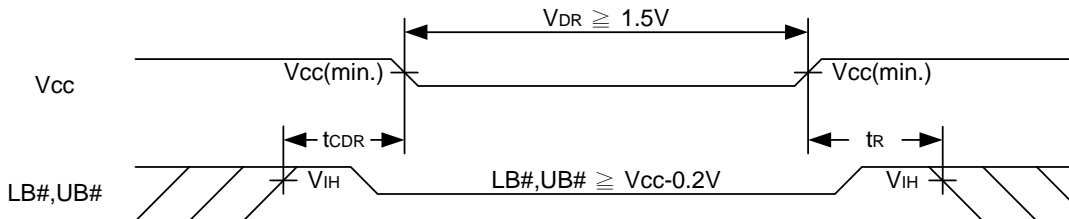
**Low V<sub>CC</sub> Data Retention Waveform (1) (CE# controlled)**



**Low V<sub>CC</sub> Data Retention Waveform (2) (CE2 controlled)**

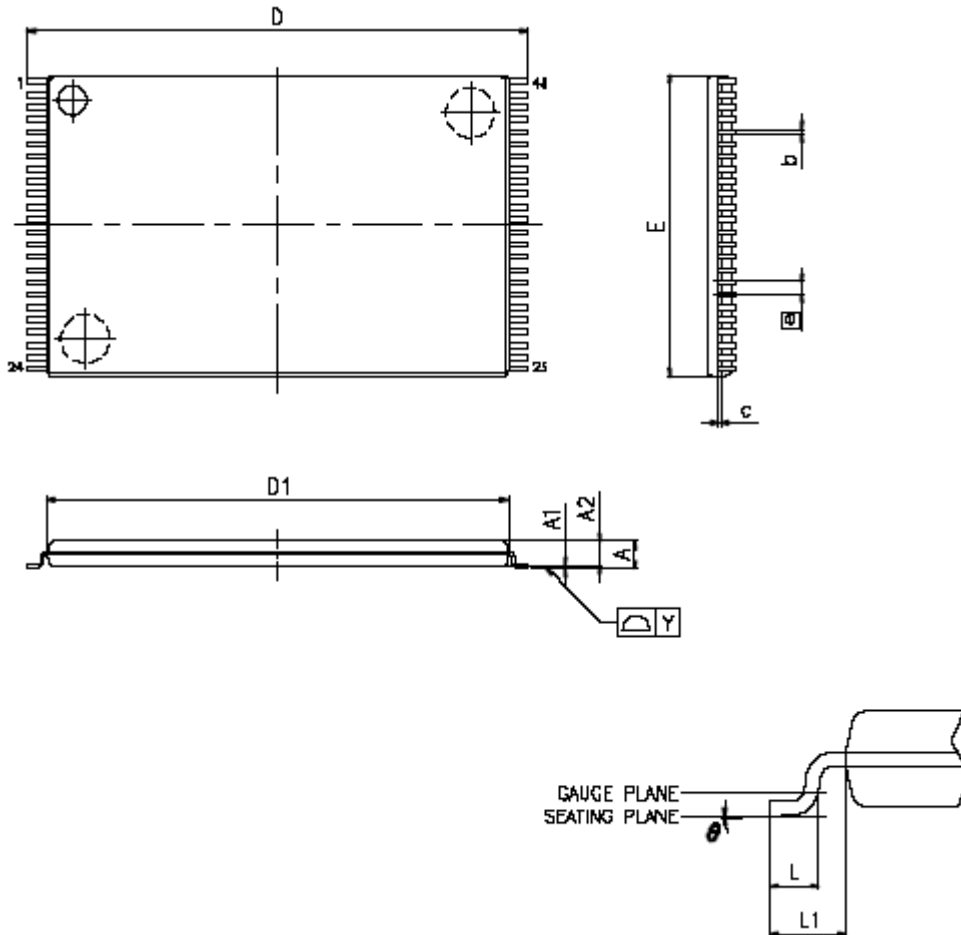


**Low V<sub>CC</sub> Data Retention Waveform (3) (LB#, UB# controlled)**



### PACKAGE OUTLINE DIMENSION

48-pin 12mm x 20mm TSOP-I Package Outline Dimension



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

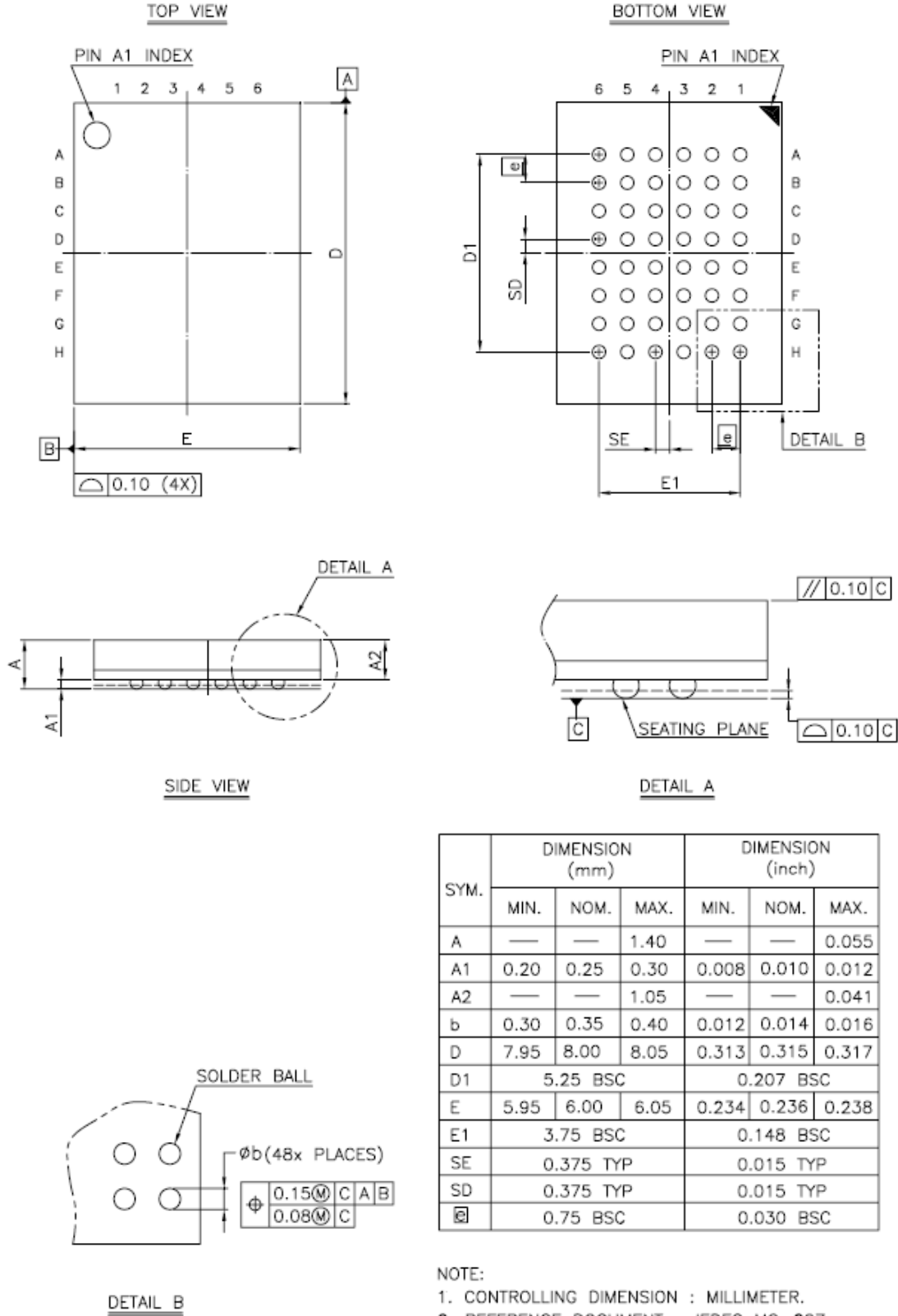
SYMBOLS	MIN.	NOM.	MAX
A	-	-	1.20
A1	0.05	-	0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
c	0.10	-	0.21
D	19.80	20.00	20.20
D1	18.30	18.40	18.50
E	11.90	12.00	12.10
a	0.50 BASIC		
L	0.50	0.60	0.70
L1	-	0.80	-
Y	-	-	0.10
θ	0°	-	5°

NOTES:

1. JEDEC OUTLINE : MO-142 DD
2. PROFILE TOLERANCE ZONES FOR D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION ON E IS 0.15mm PER SIDE AND ON D1 IS 0.25mm PER SIDE.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.



**48-ball 6mm x 8mm TFBGA Package Outline Dimension**





### ORDERING INFORMATION

LY62102516 U V - WW XX Y Z

Z : Packing Type

Blank : Tube or Tray Tray : 48-pin 12 mm x 20 mm TSOP-I 48-ball 6 mm x 8 mm TFBGA T : Tape Reel
--

Y : Temperature Range

Blank : (Commercial) 0°C ~ 70°C E : (Extended) -20°C ~ +80°C I : (Industrial) -40°C ~ +85°C
---

XX : Power Type

LL : Ultra Low Power

WW : Access Time(Speed)

V : Lead Information

L : Green Package

U : Package Type

L : 48-pin 12 mm x 20 mm TSOP-I G : 48-ball 6 mm x 8 mm TFBGA
--



**Lyontek Inc.**

**LY62102516**

Rev. 0.4

**1024K X 16 BIT LOW POWER CMOS SRAM**

---

THIS PAGE IS LEFT BLANK INTENTIONALLY.