



REVISION HISTORY

<u>Revision</u>	<u>Description</u>	<u>Issue Date</u>
Rev. 1.0	Initial Issue	Jul.25.2004
Rev. 1.1	Revised Icc	Aug.13.2004
Rev. 1.2	Deleted L grade Added SL grade Added I _{SB1} /I _{DR} values when T _A = 25°C and T _A = 40°C Revised FEATURES & ORDERING INFORMATION Lead free and green package available to Green package available Added packing type in ORDERING INFORMATION Revised V _{TERM} to V _{T1} and V _{T2} Deleted T _{SOLDER} in ABSOLUTE MAXIMUN RATINGS	Mar.30.2009
Rev. 1.3	Revised PACKAGE OUTLINE DIMENSION in page 9 & 10	Dec.18.2009
Rev. 1.4	Revised PACKAGE OUTLINE DIMENSION in page 10/11/12/13	May.7.2010
Rev. 1.5	Revised ORDERING INFORMATION in page 14	Aug.25.2010
Rev. 1.6	Revised ORDERING INFORMATION	Dec.10.2010
Rev. 1.7	Deleted E grade Added -45ns Spec. Revised ORDERING INFORMATION	Feb.26.2015
Rev. 1.8	Revised PIN CONFIGURATION in page 2 Deleted 32 pin 600 mil P-DIP Package Outline Dimension in page 12	Jun.17.2016
Rev. 1.9	Deleted 32-pin 600 mil P-DIP in FEATURES Deleted WRITE CYCLE Notes : 1.WE#, CE# must be high or CE2 must be low during all address transitions in page 7	Jun.28.2016

FEATURES

- Fast access time : 35/45/55/70ns
- Low power consumption:
 Operating current : 12/11/10/7mA (TYP.)
 Standby current : 1 μ A (TYP.) LL-version
 0.8 μ A (TYP.) SL-version
- Single 2.7V ~ 3.6V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data retention voltage : 1.5V (MIN.)
- **Green package available**
- Package : 32-pin 450 mil SOP
 32-pin 8mm x 20mm TSOP I
 32-pin 8mm x 13.4mm sTSP
 36-ball 6mm x 8mm TFBGA

GENERAL DESCRIPTION

The LY62L1024 is a 1,048,576-bit low power CMOS static random access memory organized as 131,072 words by 8 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

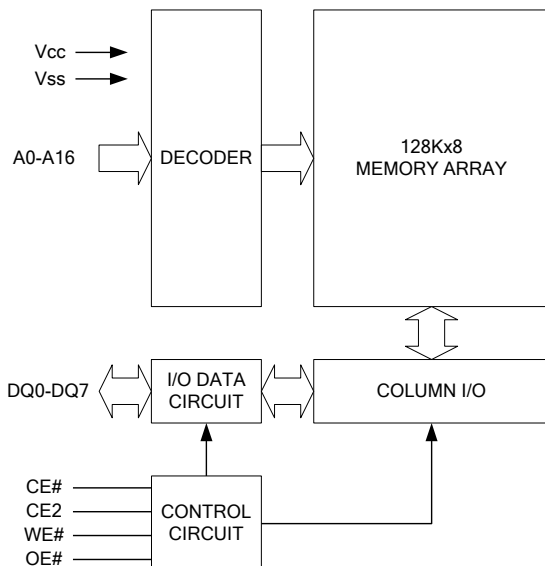
The LY62L1024 is well designed for very low power system applications, and particularly well suited for battery back-up nonvolatile memory application.

The LY62L1024 operates from a single power supply of 2.7V ~ 3.6V and all inputs and outputs are fully TTL compatible

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation	
				Standby(I_{SB1} , TYP.)	Operating(I_{CC} , TYP.)
LY62L1024	0 ~ 70°C	2.7 ~ 3.6V	35/45/55/70ns	1 μ A(LL)/0.8 μ A(SL)	12/11/10/7mA
LY62L1024(I)	-40 ~ 85°C	2.7 ~ 3.6V	35/45/55/70ns	1 μ A(LL)/0.8 μ A(SL)	12/11/10/7mA

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A16	Address Inputs
DQ0 - DQ7	Data Inputs/Outputs
CE#, CE2	Chip Enable Inputs
WE#	Write Enable Input
OE#	Output Enable Input
Vcc	Power Supply
Vss	Ground
NC	No Connection

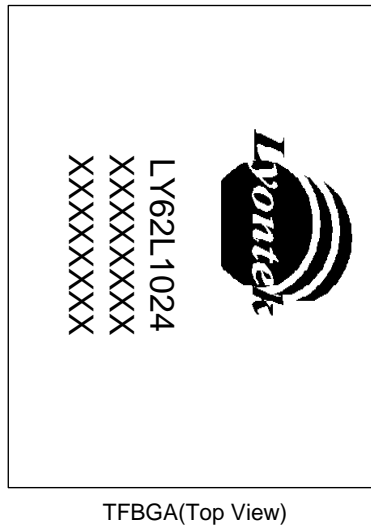
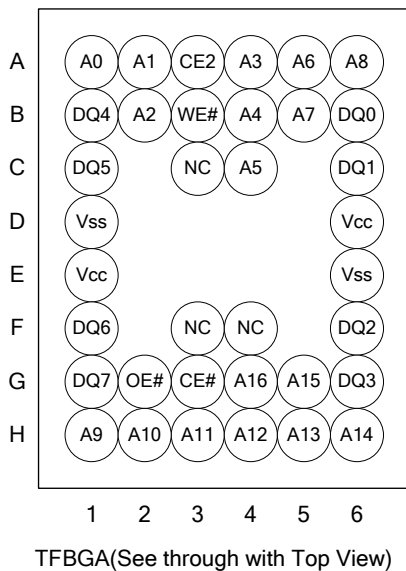
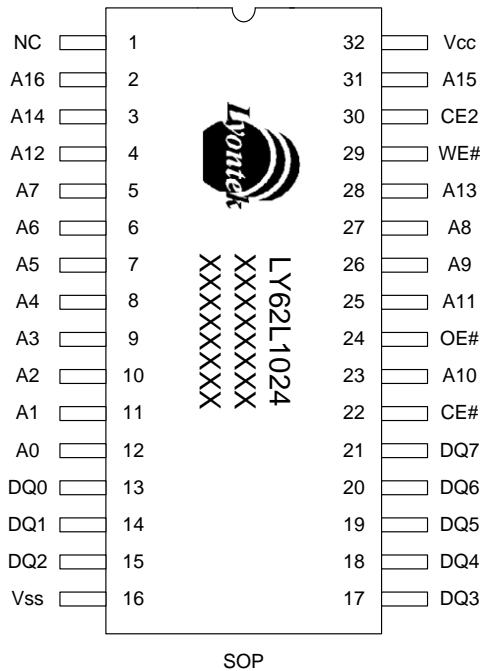
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PIN CONFIGURATION





ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on Vcc relative to Vss	V _{T1}	-0.5 to 4.6	V
Voltage on any other pin relative to Vss	V _{T2}	-0.5 to V _{CC} +0.5	V
Operating Temperature	T _A	0 to 70(C grade)	°C
		-40 to 85(I grade)	
Storage Temperature	T _{STG}	-65 to 150	°C
Power Dissipation	P _D	1	W
DC Output Current	I _{OUT}	50	mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE#	CE2	OE#	WE#	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	X	High-Z	I _{SB} , I _{SB1}
	X	L	X	X	High-Z	I _{SB} , I _{SB1}
Output Disable	L	H	H	H	High-Z	I _{CC} , I _{CC1}
Read	L	H	L	H	D _{OUT}	I _{CC} , I _{CC1}
Write	L	H	X	L	D _{IN}	I _{CC} , I _{CC1}

Note: H = V_{IH}, L = V_{IL}, X = Don't care.



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP. ⁴	MAX.	UNIT		
Supply Voltage	V _{CC}		2.7	3.0	3.6	V		
Input High Voltage	V _{IH} ¹		2.2	-	V _{CC} +0.3	V		
Input Low Voltage	V _{IL} ²		- 0.2	-	0.6	V		
Input Leakage Current	I _{LI}	V _{CC} ≥ V _{IN} ≥ V _{SS}	- 1	-	1	μA		
Output Leakage Current	I _{LO}	V _{CC} ≥ V _{OUT} ≥ V _{SS} , Output Disabled	- 1	-	1	μA		
Output High Voltage	V _{OH}	I _{OH} = -1mA	2.2	2.7	-	V		
Output Low Voltage	V _{OL}	I _{OL} = 2mA	-	-	0.4	V		
Average Operating Power supply Current	I _{CC}	Cycle time = Min. CE# = V _{IL} and CE2 = V _{IH} , I _{I/O} = 0mA Other pins at V _{IL} or V _{IH}	- 35	-	12	35	mA	
			- 45	-	11	33	mA	
			- 55	-	10	30	mA	
			- 70	-	7	25	mA	
	I _{CC1}	Cycle time = 1μs CE# = 0.2V and CE2 ≥ V _{CC} -0.2V, I _{I/O} = 0mA Other pins at 0.2V or V _{CC} - 0.2V	-	1	5	mA		
Standby Power Supply Current	I _{SB}	CE# = V _{IH} or CE2 = V _{IL} , other pins at V _{IL} or V _{IH}	-	0.3	0.5	mA		
	I _{SB1}	CE# ≥ V _{CC} -0.2V or CE2 ≤ 0.2V Others at 0.2V or V _{CC} - 0.2V	LL	-	1	10	μA	
			LLI	-	1	20	μA	
			SL ^{*5}	25°C	-	0.8	2	μA
			SLI ^{*5}	40°C	-	1	2	μA
			SL	-	0.8	5	μA	
SLI	-	0.8	8	μA				

Notes:

- V_{IH}(max) = V_{CC} + 3.0V for pulse width less than 10ns.
- V_{IL}(min) = V_{SS} - 3.0V for pulse width less than 10ns.
- Over/Undershoot specifications are characterized, not 100% tested.
- Typical values are included for reference only and are not guaranteed or tested.
Typical values are measured at V_{CC} = V_{CC}(TYP.) and T_A = 25°C
- This parameter is measured at V_{CC} = 3.0V

CAPACITANCE (T_A = 25°C, f = 1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C _{IN}	-	6	pF
Input/Output Capacitance	C _{I/O}	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0.2V to V _{CC} - 0.2V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	C _L = 30pF + 1TTL, I _{OH} /I _{OL} = -1mA/2mA

AC ELECTRICAL CHARACTERISTICS
(1) READ CYCLE

PARAMETER	SYM.	LY62L1024-35		LY62L1024-45		LY62L1024-55		LY62L1024-70		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t _{RC}	35	-	45	-	55	-	70	-	ns
Address Access Time	t _{AA}	-	35	-	45	-	55	-	70	ns
Chip Enable Access Time	t _{ACE}	-	35	-	45	-	55	-	70	ns
Output Enable Access Time	t _{OE}	-	25	-	25	-	30	-	35	ns
Chip Enable to Output in Low-Z	t _{CLZ} *	10	-	10	-	10	-	10	-	ns
Output Enable to Output in Low-Z	t _{OLZ} *	5	-	5	-	5	-	5	-	ns
Chip Disable to Output in High-Z	t _{CHZ} *	-	15	-	15	-	20	-	25	ns
Output Disable to Output in High-Z	t _{OHZ} *	-	15	-	15	-	20	-	25	ns
Output Hold from Address Change	t _{OH}	10	-	10	-	10	-	10	-	ns

(2) WRITE CYCLE

PARAMETER	SYM.	LY62L1024-35		LY62L1024-45		LY62L1024-55		LY62L1024-70		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t _{WC}	35	-	45	-	55	-	70	-	ns
Address Valid to End of Write	t _{AW}	30	-	40	-	50	-	60	-	ns
Chip Enable to End of Write	t _{CW}	30	-	40	-	50	-	60	-	ns
Address Set-up Time	t _{AS}	0	-	0	-	0	-	0	-	ns
Write Pulse Width	t _{WP}	25	-	35	-	45	-	55	-	ns
Write Recovery Time	t _{WR}	0	-	0	-	0	-	0	-	ns
Data to Write Time Overlap	t _{DW}	20	-	20	-	25	-	30	-	ns
Data Hold from End of Write Time	t _{DH}	0	-	0	-	0	-	0	-	ns
Output Active from End of Write	t _{OW} *	5	-	5	-	5	-	5	-	ns
Write to Output in High-Z	t _{WHZ} *	-	15	-	15	-	20	-	25	ns

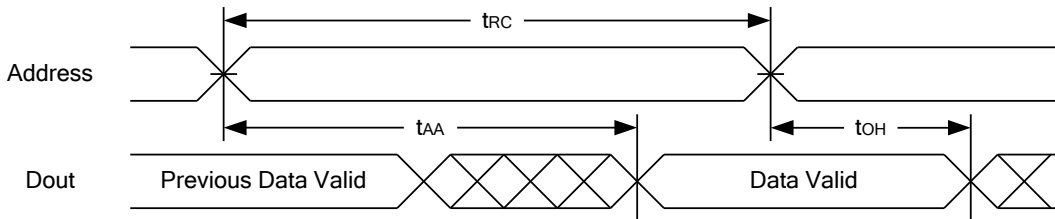
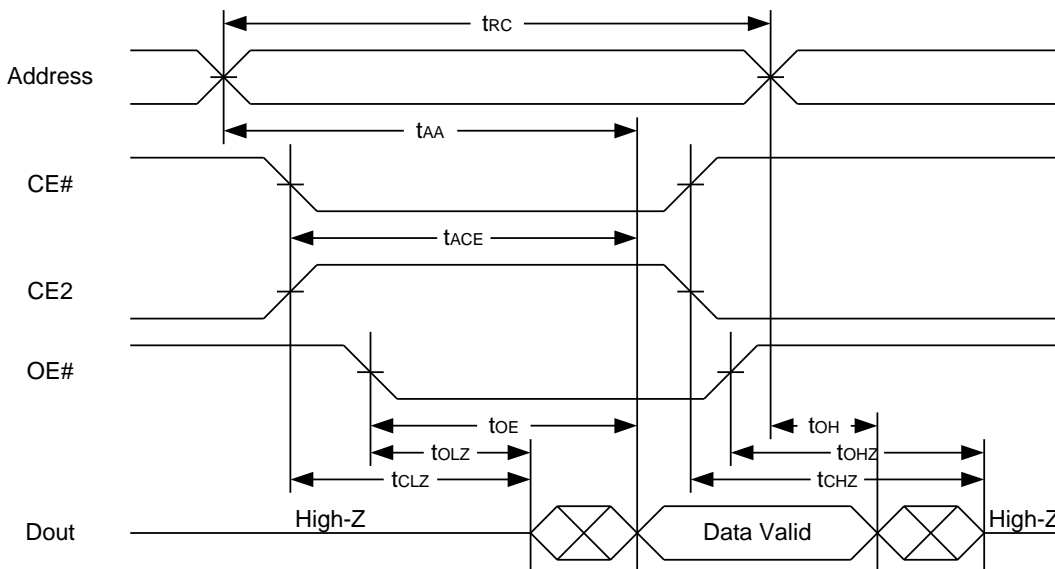
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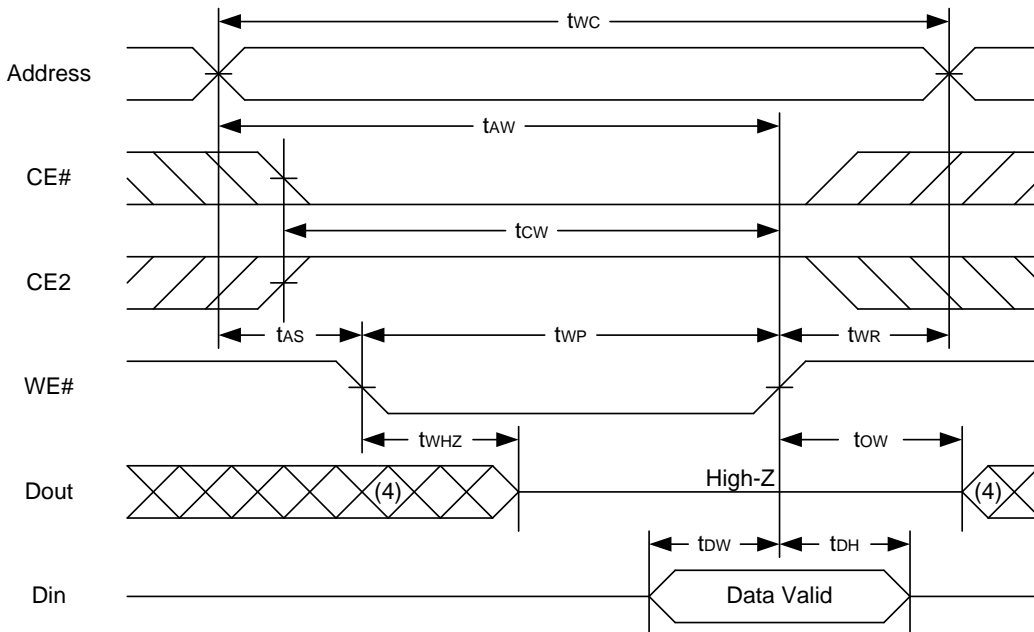
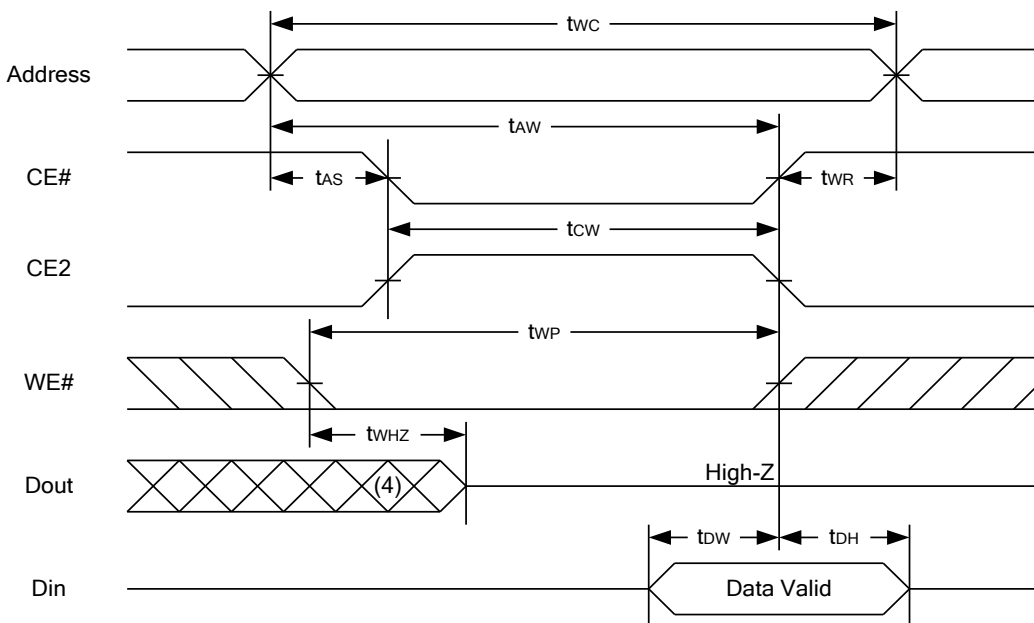
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TIMING WAVEFORMS
READ CYCLE 1 (Address Controlled) (1,2)

READ CYCLE 2 (CE# and CE2 and OE# Controlled) (1,3,4,5)

Notes :

1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low., CE2 = high.
3. Address must be valid prior to or coincident with CE# = low, CE2 = high; otherwise tAA is the limiting parameter.
4. tCLZ, tOLZ, tCHZ and tOHZ are specified with CL = 5pF. Transition is measured ±500mV from steady state.
5. At any given temperature and voltage condition, tCHZ is less than tCLZ, tOHZ is less than tOLZ.

WRITE CYCLE 1 (WE# Controlled) (1,2,4,5)

WRITE CYCLE 2 (CE# and CE2 Controlled) (1,4,5)

Notes :

1. A write occurs during the overlap of a low CE#, high CE2, low WE#.
2. During a WE#-controlled write cycle with OE# low, twp must be greater than twhz + tdw to allow the drivers to turn off and data to be placed on the bus.
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the CE#-low transition and CE2 high transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
5. tow and twhz are specified with CL = 5pF. Transition is measured ±500mV from steady state.

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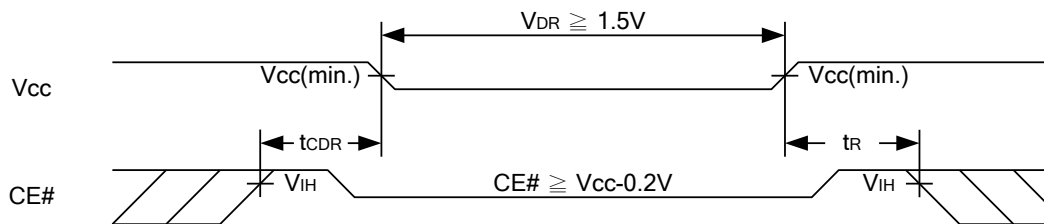
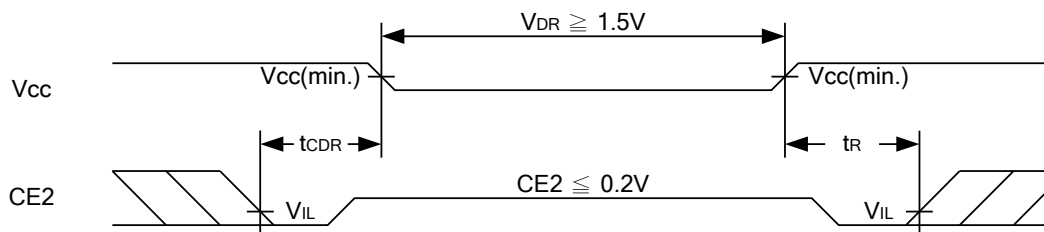
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DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
V _{CC} for Data Retention	V _{DR}	CE# ≥ V _{CC} - 0.2V or CE2 ≤ 0.2V	1.5	-	3.6	V	
Data Retention Current	I _{DR}	V _{CC} = 1.5V CE# ≥ V _{CC} - 0.2V or CE2 ≤ 0.2V Other pins at 0.2V or V _{CC} -0.2V	LL	-	0.5	5	μA
			LLI	-	0.5	10	μA
			SL 25°C	-	0.4	2	μA
			SLI 40°C	-	0.5	2	μA
			SL	-	0.4	5	μA
			SLI	-	0.4	8	μA
Chip Disable to Data Retention Time	t _{CDR}	See Data Retention Waveforms (below)	0	-	-	ns	
Recovery Time	t _R		t _{RC*}	-	-	ns	

 t_{RC*} = Read Cycle Time

DATA RETENTION WAVEFORM
Low V_{CC} Data Retention Waveform (1) (CE# controlled)

Low V_{CC} Data Retention Waveform (2) (CE2 controlled)

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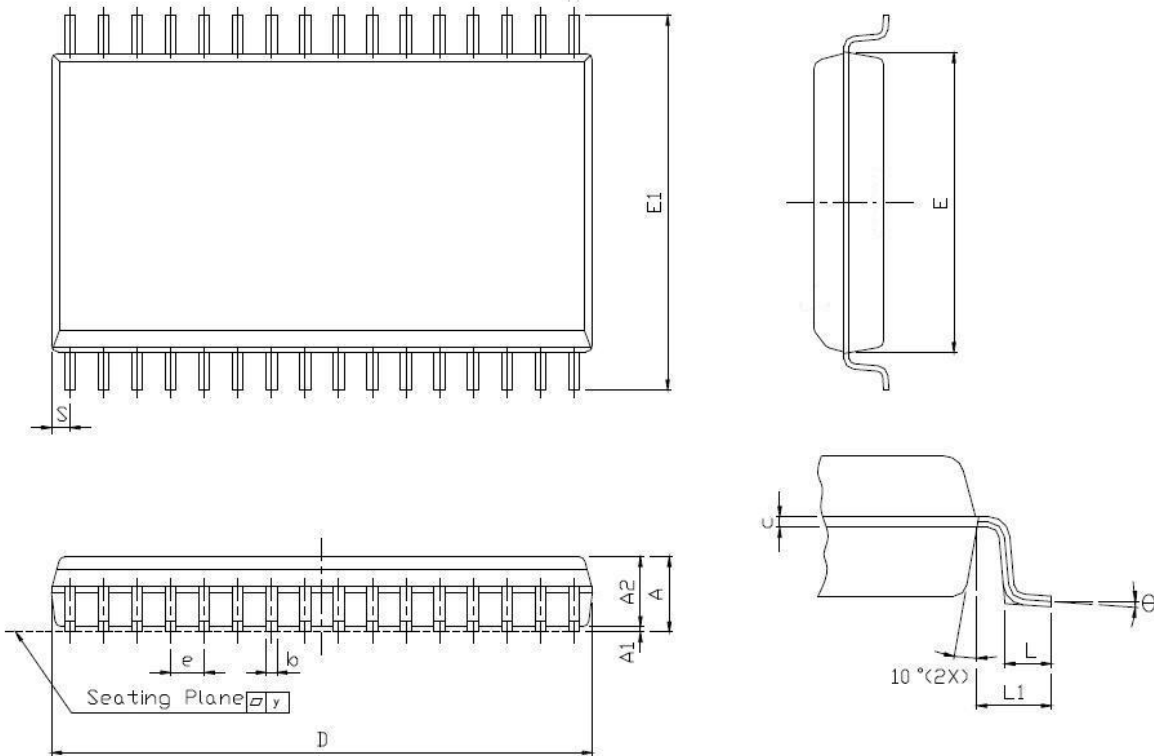
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PACKAGE OUTLINE DIMENSION

32 pin 450 mil SOP Package Outline Dimension



SYM.	UNIT	INCH.(BASE)	MM(REF)
A		0.120(MAX)	3.048(MAX)
A1		0.004(MIN)	0.102(MIN)
A2		0.116(MAX)	2.946(MAX)
b		0.016(TYP)	0.406(TYP)
c		0.008(TYP)	0.203(TYP)
D		0.817(MAX)	20.75(MAX)
E		0.445±0.006	11.303±0.152
E1		0.555±0.025	14.097±0.635
e		0.050(TYP)	1.270(TYP)
L		0.033±0.017	0.838±0.432
L1		0.055±0.008	1.397±0.203
S		0.026(MAX)	0.660(MAX)
y		0.004(MAX)	0.101(MAX)
Θ		0° -10°	0° -10°

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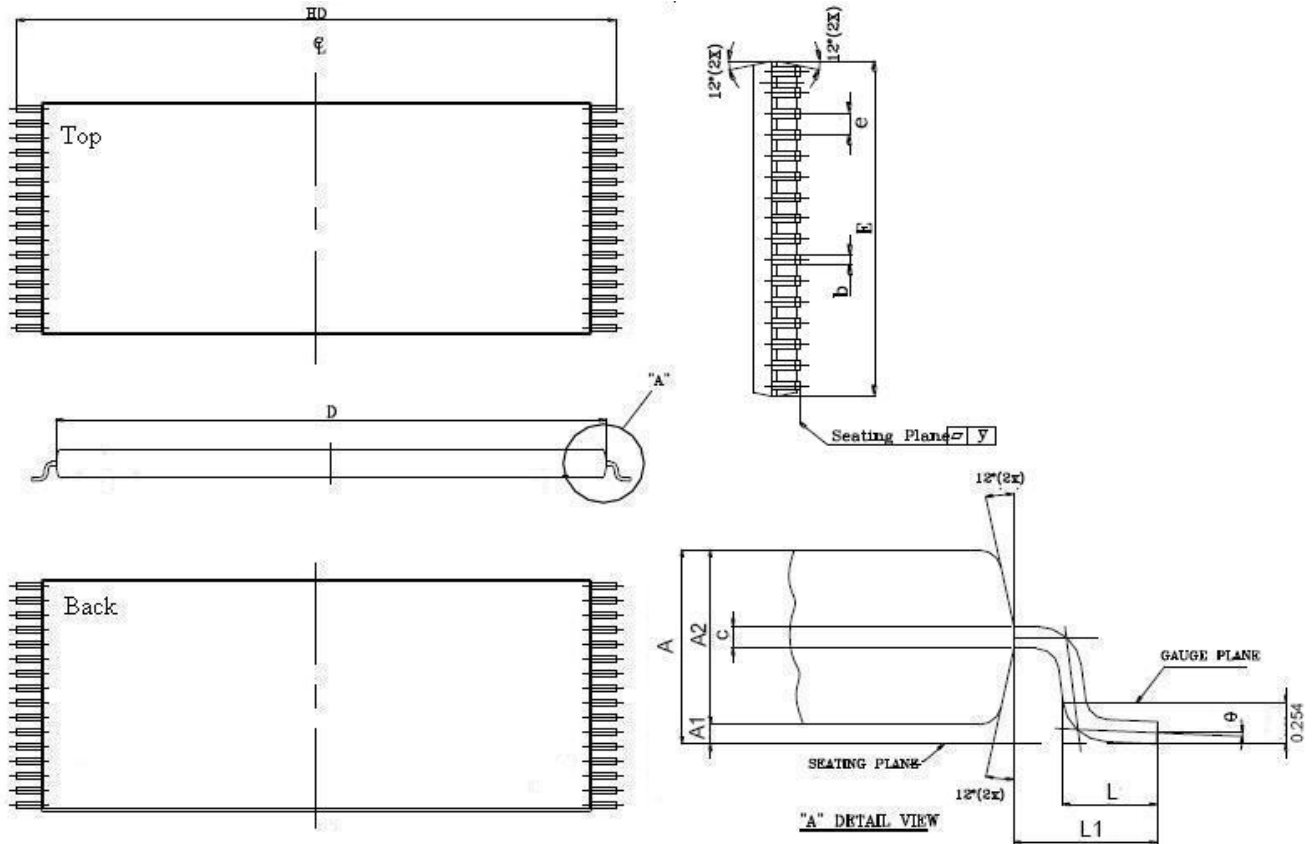
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32 pin 8mm x 20mm TSOP I Package Outline Dimension



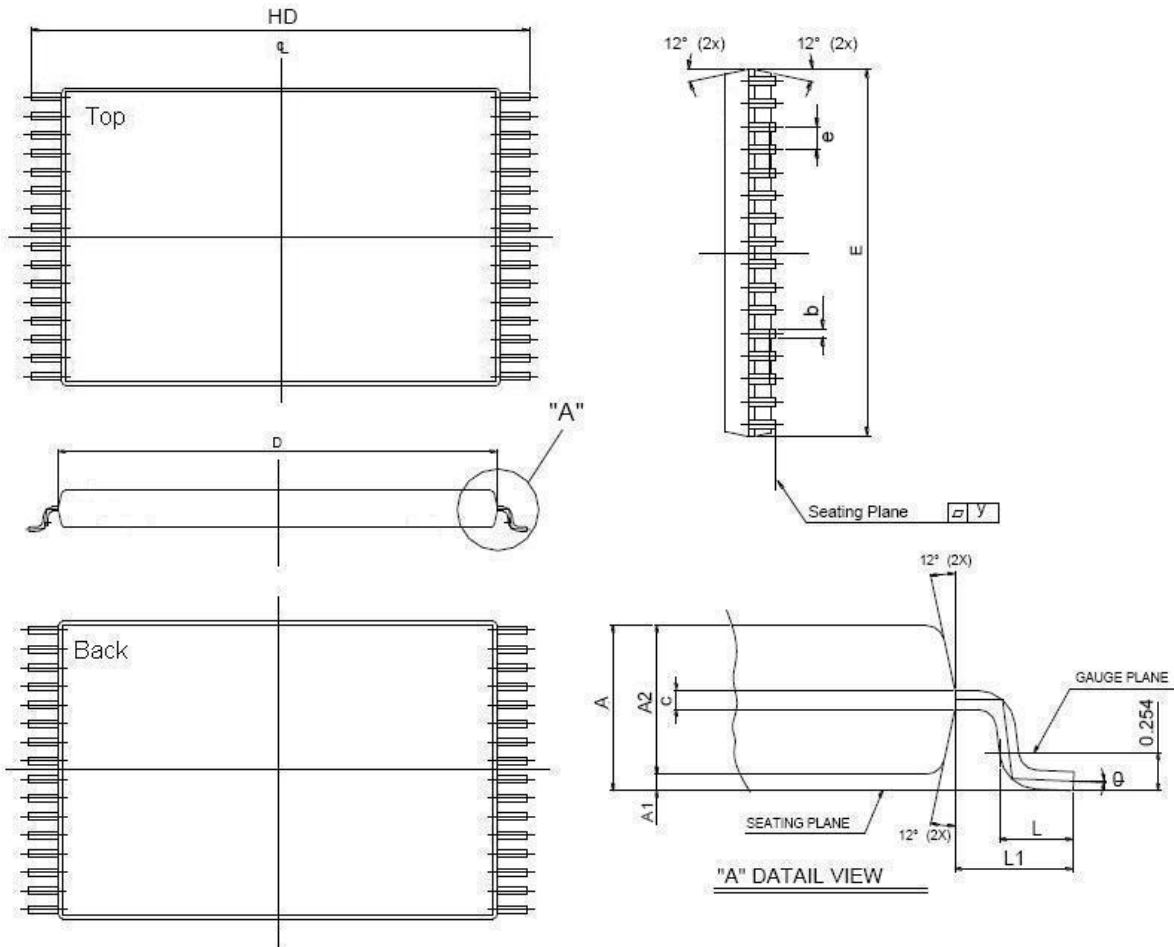
SYM.	UNIT	
	INCH(BASE)	MM(REF)
A	0.047 (MAX)	1.20 (MAX)
A1	0.004 ±0.002	0.10 ±0.05
A2	0.039 ±0.002	1.00 ±0.05
b	0.009 ±0.002	0.22 ±0.05
c	0.006 ±0.002	0.155 ±0.055
D	0.724 ±0.008	18.40 ±0.20
E	0.315 ±0.008	8.00 ±0.20
e	0.020 (TYP)	0.50 (TYP)
HD	0.787 ±0.008	20.00 ±0.20
L	0.024 ±0.004	0.60 ±0.10
L1	0.0315 ±0.004	0.08 ±0.10
y	0.003 (MAX)	0.08 (MAX)
Θ	0°~5°	0°~5°

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32 pin 8mm x 13.4mm sTSSOP Package Outline Dimension


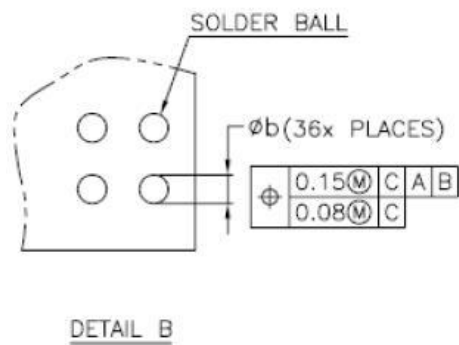
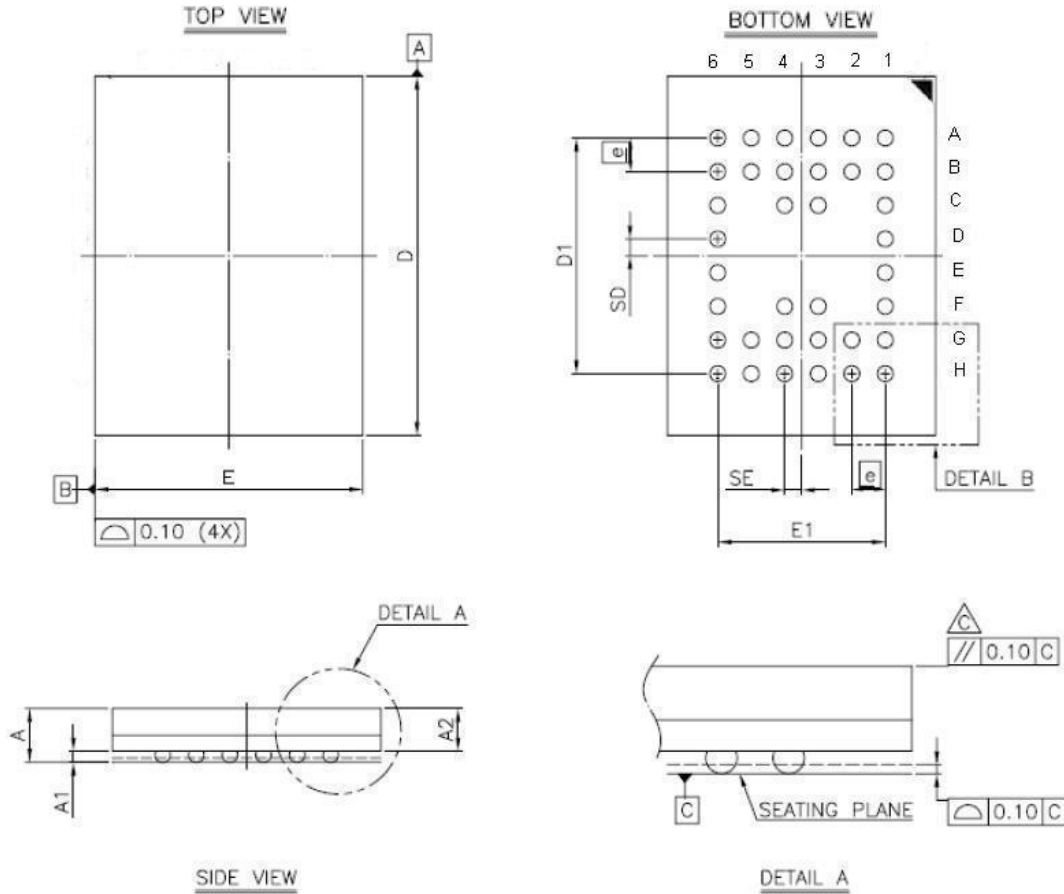
SYM.	UNIT	
	INCH(BASE)	MM(REF)
A	0.049 (MAX)	1.25 (MAX)
A1	0.004 ±0.002	0.10 ±0.05
A2	0.039 ±0.002	1.00 ±0.05
b	0.009 ±0.002	0.22 ±0.05
c	0.006 ±0.002	0.155 ±0.055
D	0.465 ±0.008	11.80 ±0.20
E	0.315 ±0.008	8.00 ±0.20
e	0.020 (TYP)	0.50 (TYP)
HD	0.528±0.008	13.40 ±0.20.
L	0.02 ±0.008	0.50 ±0.20
L1	0.031 ±0.005	0.8 ±0.125
y	0.003 (MAX)	0.076 (MAX)
θ	0°~5°	0°~5°

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36 ball 6mm x 8mm TFBGA Package Outline Dimension


SYM.	DIMENSION (mm)			DIMENSION (inch)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A1	0.20	0.25	0.30	0.008	0.010	0.012
A2	—	—	0.94	—	—	0.037
b	0.30	0.35	0.40	0.012	0.014	0.016
D	7.95	8.00	8.05	0.313	0.315	0.317
D1	5.25 BSC			0.207 BSC		
E	5.95	6.00	6.05	0.234	0.236	0.238
E1	3.75 BSC			0.148 BSC		
SE	0.375 TYP			0.015 TYP		
SD	0.375 TYP			0.015 TYP		
e	0.75 BSC			0.030 BSC		

NOTE:

1. CONTROLLING DIMENSION : MILLIMETER.
2. REFERENCE DOCUMENT : JEDEC MO-207.

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ORDERING INFORMATION

Package Type	Access Time (Speed)(ns)	Power Type	Temperature Range(°C)	Packing Type	Lyontek Item No.
32Pin(450mil) SOP	35	Ultra Low Power	0°C~70°C	Tube	LY62L1024SL-35LL
				Tape Reel	LY62L1024SL-35LLT
			-40°C~85°C	Tube	LY62L1024SL-35LLI
				Tape Reel	LY62L1024SL-35LLIT
	45	Special Ultra Low Power	0°C~70°C	Tube	LY62L1024SL-45SL
				Tape Reel	LY62L1024SL-45SLT
			-40°C~85°C	Tube	LY62L1024SL-45SLI
				Tape Reel	LY62L1024SL-45SLIT
	55	Special Ultra Low Power	0°C~70°C	Tube	LY62L1024SL-55SL
				Tape Reel	LY62L1024SL-55SLT
			-40°C~85°C	Tube	LY62L1024SL-55SLI
				Tape Reel	LY62L1024SL-55SLIT
		Ultra Low Power	0°C~70°C	Tube	LY62L1024SL-55LL
				Tape Reel	LY62L1024SL-55LLT
			-40°C~85°C	Tube	LY62L1024SL-55LLI
				Tape Reel	LY62L1024SL-55LLIT
70	Special Ultra Low Power	0°C~70°C	Tube	LY62L1024SL-70SL	
			Tape Reel	LY62L1024SL-70SLT	
		-40°C~85°C	Tube	LY62L1024SL-70SLI	
			Tape Reel	LY62L1024SL-70SLIT	
	Ultra Low Power	0°C~70°C	Tube	LY62L1024SL-70LL	
			Tape Reel	LY62L1024SL-70LLT	
		-40°C~85°C	Tube	LY62L1024SL-70LLI	
			Tape Reel	LY62L1024SL-70LLIT	

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ORDERING INFORMATION

Package Type	Access Time (Speed)(ns)	Power Type	Temperature Range(°C)	Packing Type	Lyontek Item No.
32Pin (8mmx20mm) TSOP I	35	Ultra Low Power	0°C~70°C	Tray	LY62L1024LL-35LL
				Tape Reel	LY62L1024LL-35LLT
			-40°C~85°C	Tray	LY62L1024LL-35LLI
				Tape Reel	LY62L1024LL-35LLIT
	45	Special Ultra Low Power	0°C~70°C	Tray	LY62L1024LL-45SL
				Tape Reel	LY62L1024LL-45SLT
			-40°C~85°C	Tray	LY62L1024LL-45SLI
				Tape Reel	LY62L1024LL-45SLIT
	55	Special Ultra Low Power	0°C~70°C	Tray	LY62L1024LL-55SL
				Tape Reel	LY62L1024LL-55SLT
			-40°C~85°C	Tray	LY62L1024LL-55SLI
				Tape Reel	LY62L1024LL-55SLIT
		Ultra Low Power	0°C~70°C	Tray	LY62L1024LL-55LL
				Tape Reel	LY62L1024LL-55LLT
			-40°C~85°C	Tray	LY62L1024LL-55LLI
				Tape Reel	LY62L1024LL-55LLIT
	70	Special Ultra Low Power	0°C~70°C	Tray	LY62L1024LL-70SL
				Tape Reel	LY62L1024LL-70SLT
			-40°C~85°C	Tray	LY62L1024LL-70SLI
				Tape Reel	LY62L1024LL-70SLIT
Ultra Low Power		0°C~70°C	Tray	LY62L1024LL-70LL	
			Tape Reel	LY62L1024LL-70LLT	
		-40°C~85°C	Tray	LY62L1024LL-70LLI	
			Tape Reel	LY62L1024LL-70LLIT	

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ORDERING INFORMATION

Package Type	Access Time (Speed)(ns)	Power Type	Temperature Range(°C)	Packing Type	Lyontek Item No.
32Pin (8mmx13.4mm) sTSOP	35	Ultra Low Power	0°C~70°C	Tray	LY62L1024RL-35LL
				Tape Reel	LY62L1024RL-35LLT
			-40°C~85°C	Tray	LY62L1024RL-35LLI
				Tape Reel	LY62L1024RL-35LLIT
	45	Special Ultra Low Power	0°C~70°C	Tray	LY62L1024RL-45SL
				Tape Reel	LY62L1024RL-45SLT
			-40°C~85°C	Tray	LY62L1024RL-45SLI
				Tape Reel	LY62L1024RL-45SLIT
	55	Special Ultra Low Power	0°C~70°C	Tray	LY62L1024RL-55SL
				Tape Reel	LY62L1024RL-55SLT
			-40°C~85°C	Tray	LY62L1024RL-55SLI
				Tape Reel	LY62L1024RL-55SLIT
		Ultra Low Power	0°C~70°C	Tray	LY62L1024RL-55LL
				Tape Reel	LY62L1024RL-55LLT
			-40°C~85°C	Tray	LY62L1024RL-55LLI
				Tape Reel	LY62L1024RL-55LLIT
70	Special Ultra Low Power	0°C~70°C	Tray	LY62L1024RL-70SL	
			Tape Reel	LY62L1024RL-70SLT	
		-40°C~85°C	Tray	LY62L1024RL-70SLI	
			Tape Reel	LY62L1024RL-70SLIT	
	Ultra Low Power	0°C~70°C	Tray	LY62L1024RL-70LL	
			Tape Reel	LY62L1024RL-70LLT	
		-40°C~85°C	Tray	LY62L1024RL-70LLI	
			Tape Reel	LY62L1024RL-70LLIT	

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Package Type	Access Time (Speed)(ns)	Power Type	Temperature Range(°C)	Packing Type	Lyontek Item No.
36Ball (6mmx8mm) TFBGA	35	Ultra Low Power	-40°C ~85°C	Tray	LY62L1024GL-35LLI
				Tape Reel	LY62L1024GL-35LLIT
	45	Special Ultra Low Power	-40°C ~85°C	Tray	LY62L1024GL-45SLI
				Tape Reel	LY62L1024GL-45SLIT
	55	Special Ultra Low Power	-40°C ~85°C	Tray	LY62L1024GL-55SLI
				Tape Reel	LY62L1024GL-55SLIT
		Ultra Low Power	-40°C ~85°C	Tray	LY62L1024GL-55LLI
				Tape Reel	LY62L1024GL-55LLIT
	70	Special Ultra Low Power	-40°C ~85°C	Tray	LY62L1024GL-70SLI
				Tape Reel	LY62L1024GL-70SLIT
		Ultra Low Power	-40°C ~85°C	Tray	LY62L1024GL-70LLI
				Tape Reel	LY62L1024GL-70LLIT

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Lyontek Inc.

LY62L1024

Rev. 1.9

128K X 8 BIT LOW POWER CMOS SRAM

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