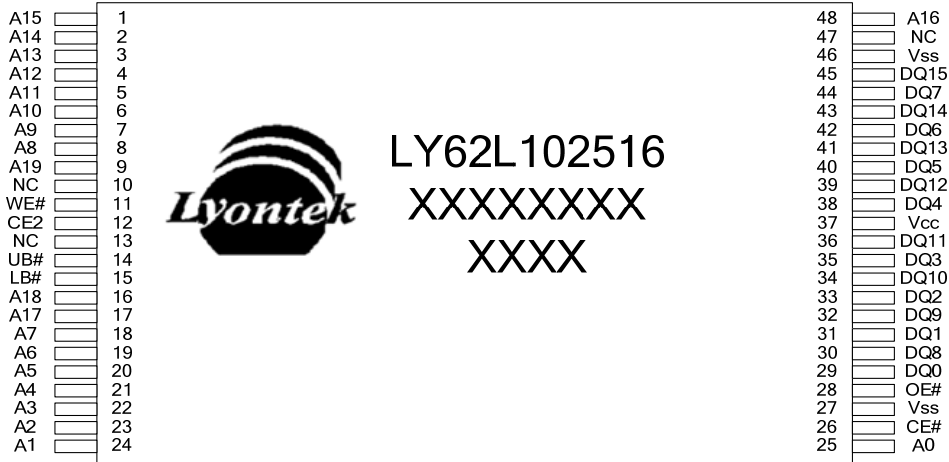




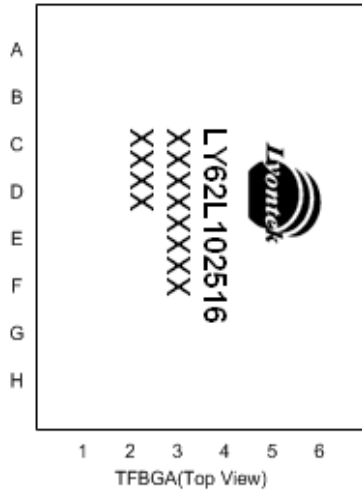
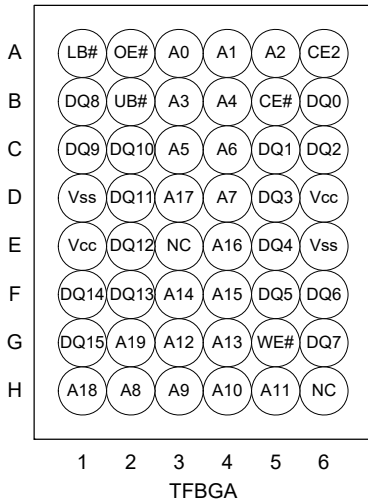
REVISION HISTORY

<u>Revision</u>	<u>Description</u>	<u>Issue Date</u>
Rev. 0.1	Initial Issue	Feb.20.2008
Rev. 0.2	Added SL Spec.	Jul.2.2008
Rev. 0.3	Added I _{SB1} /I _{DR} values when T _A = 25°C and T _A = 40°C Revised FEATURES & ORDERING INFORMATION Lead free and green package available to Green package available Added packing type in ORDERING INFORMATION	Mar.30.2009
Rev. 0.4	Deleted T _{SOLDER} in ABSOLUTE MAXIMUM RATINGS	May.7.2010
Rev. 1.0	Revised PACKAGE OUTLINE DIMENSION in page 10 Deleted Notes item 1 and 2 in page 3 1. V _{IH} (max) = V _{CC} + 2.0V for pulse width less than 6ns. 2. V _{IL} (min) = V _{SS} - 2.0V for pulse width less than 6ns.	Aug.29.2013
Rev. 1.1	Revised ORDERING INFORMATION Deleted WRITE CYCLE Notes : 1.WE#,CE#, LB#, UB# must be high or CE2 must be low during all address transitions. In page 8.	May.18.2016

PIN CONFIGURATION



TSOP-4



TFBGA(Top View)



ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on Vcc relative to Vss	V _{T1}	-0.5 to 4.6	V
Voltage on any other pin relative to Vss	V _{T2}	-0.5 to V _{CC} +0.5	V
Operating Temperature	T _A	0 to 70(C grade)	°C
		-20 to 80(E grade)	
		-40 to 85(I grade)	
Storage Temperature	T _{STG}	-65 to 150	°C
Power Dissipation	P _D	1	W
DC Output Current	I _{OUT}	50	mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE#	CE2	OE#	WE#	LB#	UB#	I/O OPERATION		SUPPLY CURRENT
							DQ0-DQ7	DQ8-DQ15	
Standby	H	X	X	X	X	X	High - Z	High - Z	I _{SB} , I _{SB1}
	X	L	X	X	X	X	High - Z	High - Z	
	X	X	X	X	H	H	High - Z	High - Z	
Output Disable	L	H	H	H	L	X	High - Z	High - Z	I _{CC} , I _{CC1}
	L	H	H	H	X	L	High - Z	High - Z	
Read	L	H	L	H	L	H	D _{OUT}	High - Z	I _{CC} , I _{CC1}
	L	H	L	H	H	L	High - Z	D _{OUT}	
	L	H	L	H	L	L	D _{OUT}	D _{OUT}	
Write	L	H	X	L	L	H	D _{IN}	High - Z	I _{CC} , I _{CC1}
	L	H	X	L	H	L	High - Z	D _{IN}	
	L	H	X	L	L	L	D _{IN}	D _{IN}	

Note: H = V_{IH}, L = V_{IL}, X = Don't care.



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.*4	MAX.	UNIT		
Supply Voltage	V _{CC}		2.7	3.0	3.6	V		
Input High Voltage	V _{IH} ^{*1}		2.2	-	V _{CC} +0.3	V		
Input Low Voltage	V _{IL} ^{*2}		-0.2	-	0.6	V		
Input Leakage Current	I _{LI}	V _{CC} ≥ V _{IN} ≥ V _{SS}	-1	-	1	μA		
Output Leakage Current	I _{LO}	V _{CC} ≥ V _{OUT} ≥ V _{SS} , Output Disabled	-1	-	1	μA		
Output High Voltage	V _{OH}	I _{OH} = -1mA	2.2	2.7	-	V		
Output Low Voltage	V _{OL}	I _{OL} = 2mA	-	-	0.4	V		
Average Operating Power supply Current	I _{CC}	Cycle time = Min. CE# = V _{IL} and CE2 = V _{IH} I _{I/O} = 0mA Other pins at V _{IL} or V _{IH}	-55	-	45	60	mA	
			-70	-	30	45	mA	
	I _{CC1}	Cycle time = 1μs CE# ≤ 0.2V and CE2 ≥ V _{CC} -0.2V I _{I/O} = 0mA other pins at 0.2V or V _{CC} -0.2V	-	8	16	mA		
Standby Power Supply Current	I _{SB}	CE# = V _{IH} or CE2 = V _{IL} Other pins at V _{IL} or V _{IH}	-	0.3	2	mA		
	I _{SB1}	CE# ≥ V _{CC} -0.2V or CE2 ≤ 0.2V Other pins at 0.2V or V _{CC} -0.2V	LL	-	10	60	μA	
			LLE	-	10	80	μA	
			LLI	-	10	100	μA	
			SL ^{*5}	25°C	-	4	6	μA
			SLE ^{*5}		-	4	6	μA
			SLI ^{*5}	40°C	-	4	6	μA
			SL		-	4	30	μA
			SLE		-	4	30	μA
SLI	-	4	40	μA				

Notes:

- V_{IH}(max) = V_{CC} + 2.0V for pulse width less than 6ns.
- V_{IL}(min) = V_{SS} - 2.0V for pulse width less than 6ns.
- Over/Undershoot specifications are characterized, not 100% tested.
- Typical values are included for reference only and are not guaranteed or tested.
Typical values are measured at V_{CC} = V_{CC}(TYP.) and T_A = 25°C
- This parameter is measured at V_{CC} = 3.0V

**CAPACITANCE (T_A = 25°C, f = 1.0MHz)**

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C _{IN}	-	6	pF
Input/Output Capacitance	C _{I/O}	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0.2V to V _{CC} - 0.2V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	C _L = 30pF + 1TTL, I _{OH} /I _{OL} = -1mA/2mA

AC ELECTRICAL CHARACTERISTICS**(1) READ CYCLE**

PARAMETER	SYM.	LY62L102516-55		LY62L102516-70		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t _{RC}	55	-	70	-	ns
Address Access Time	t _{AA}	-	55	-	70	ns
Chip Enable Access Time	t _{ACE}	-	55	-	70	ns
Output Enable Access Time	t _{OE}	-	30	-	35	ns
Chip Enable to Output in Low-Z	t _{CLZ} *	10	-	10	-	ns
Output Enable to Output in Low-Z	t _{OLZ} *	5	-	5	-	ns
Chip Disable to Output in High-Z	t _{CHZ} *	-	20	-	25	ns
Output Disable to Output in High-Z	t _{OHZ} *	-	20	-	25	ns
Output Hold from Address Change	t _{OH}	10	-	10	-	ns
LB#, UB# Access Time	t _{BA}	-	55	-	70	ns
LB#, UB# to High-Z Output	t _{BHZ} *	-	25	-	30	ns
LB#, UB# to Low-Z Output	t _{BLZ} *	10	-	10	-	ns

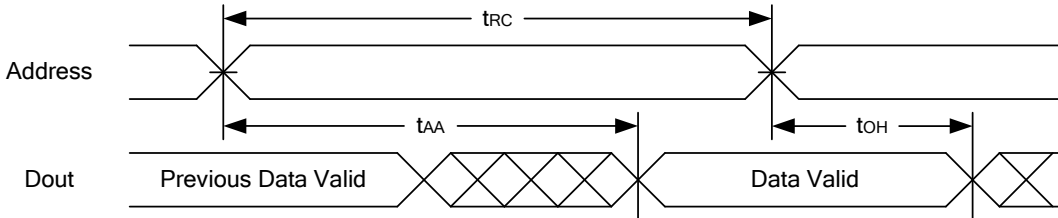
(2) WRITE CYCLE

PARAMETER	SYM.	LY62L102516-55		LY62L102516-70		UNIT
		MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t _{WC}	55	-	70	-	ns
Address Valid to End of Write	t _{AW}	50	-	60	-	ns
Chip Enable to End of Write	t _{CW}	50	-	60	-	ns
Address Set-up Time	t _{AS}	0	-	0	-	ns
Write Pulse Width	t _{WP}	45	-	55	-	ns
Write Recovery Time	t _{WR}	0	-	0	-	ns
Data to Write Time Overlap	t _{DW}	25	-	30	-	ns
Data Hold from End of Write Time	t _{DH}	0	-	0	-	ns
Output Active from End of Write	t _{OW} *	5	-	5	-	ns
Write to Output in High-Z	t _{WHZ} *	-	20	-	25	ns
LB#, UB# Valid to End of Write	t _{BW}	45	-	60	-	ns

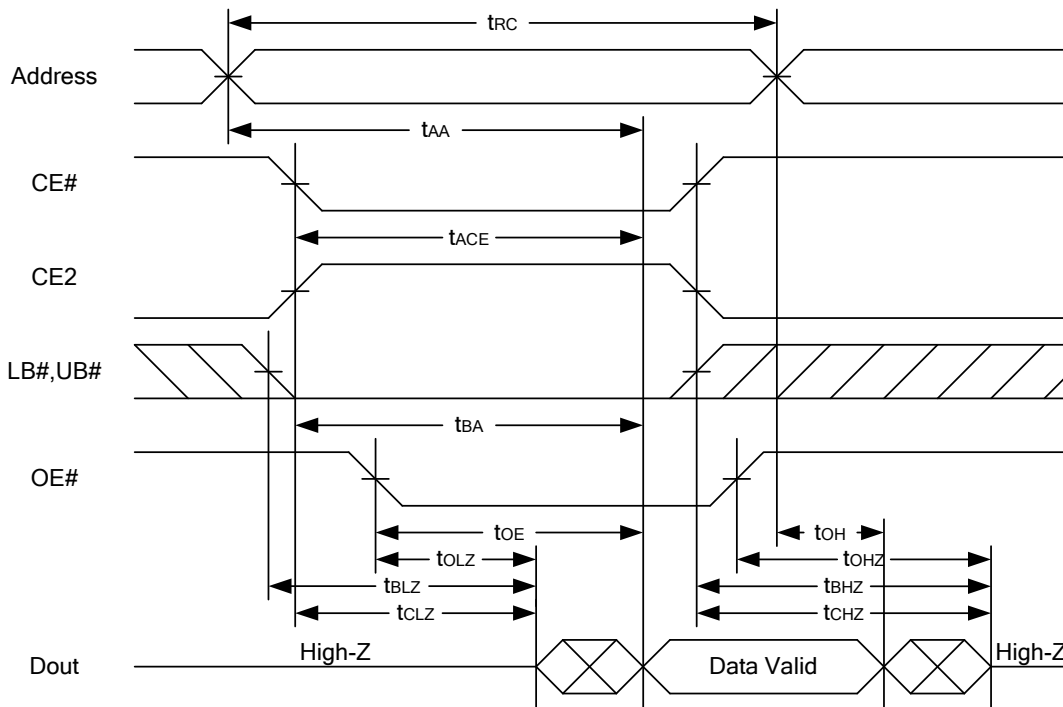
*These parameters are guaranteed by device characterization, but not production tested.

TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)



READ CYCLE 2 (CE# and CE2 and OE# Controlled) (1,3,4,5)

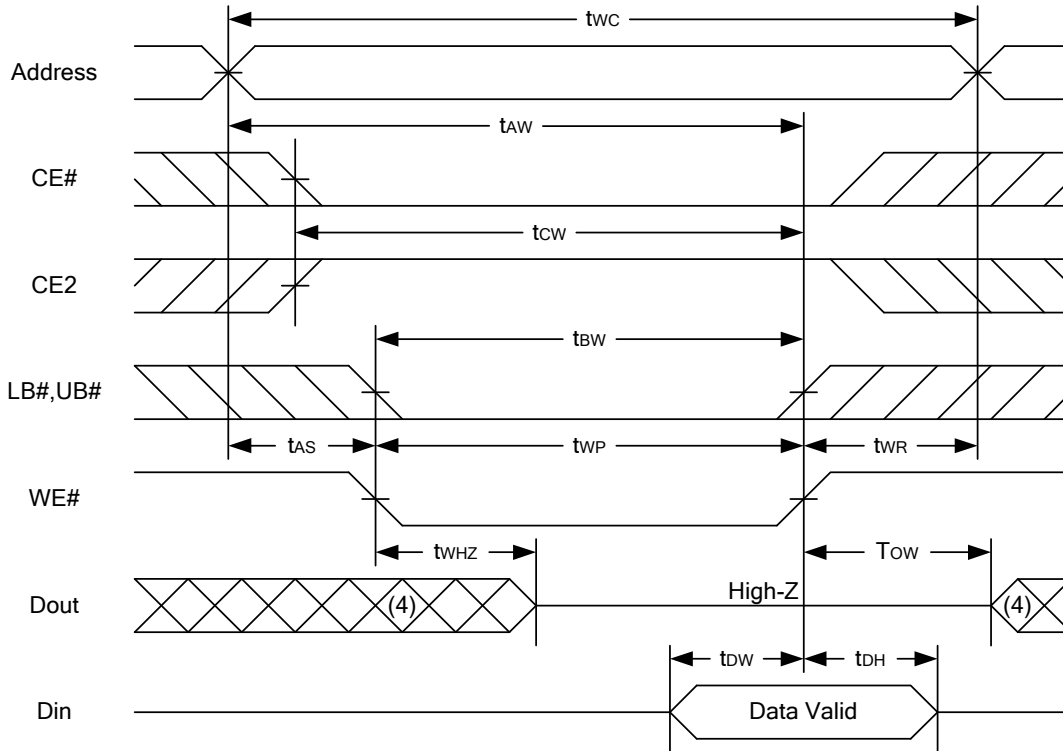


Notes :

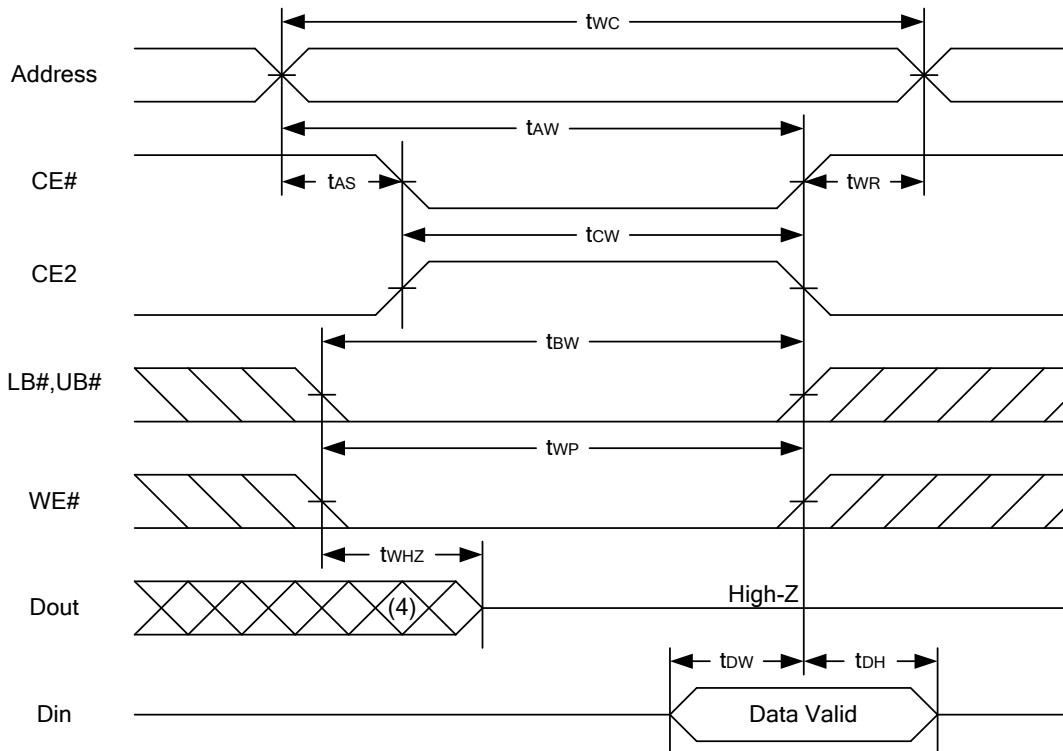
1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low, CE2 = high, LB# or UB# = low.
3. Address must be valid prior to or coincident with CE# = low, CE2 = high, LB# or UB# = low transition; otherwise tAA is the limiting parameter.
4. tCLZ, tBLZ, tOLZ, tCHZ, tBHZ and tOHZ are specified with CL = 5pF. Transition is measured ±500mV from steady state.
5. At any given temperature and voltage condition, tCHZ is less than tCLZ, tBHZ is less than tBLZ, tOHZ is less than tOLZ.



WRITE CYCLE 1 (WE# Controlled) (1,2,4,5)

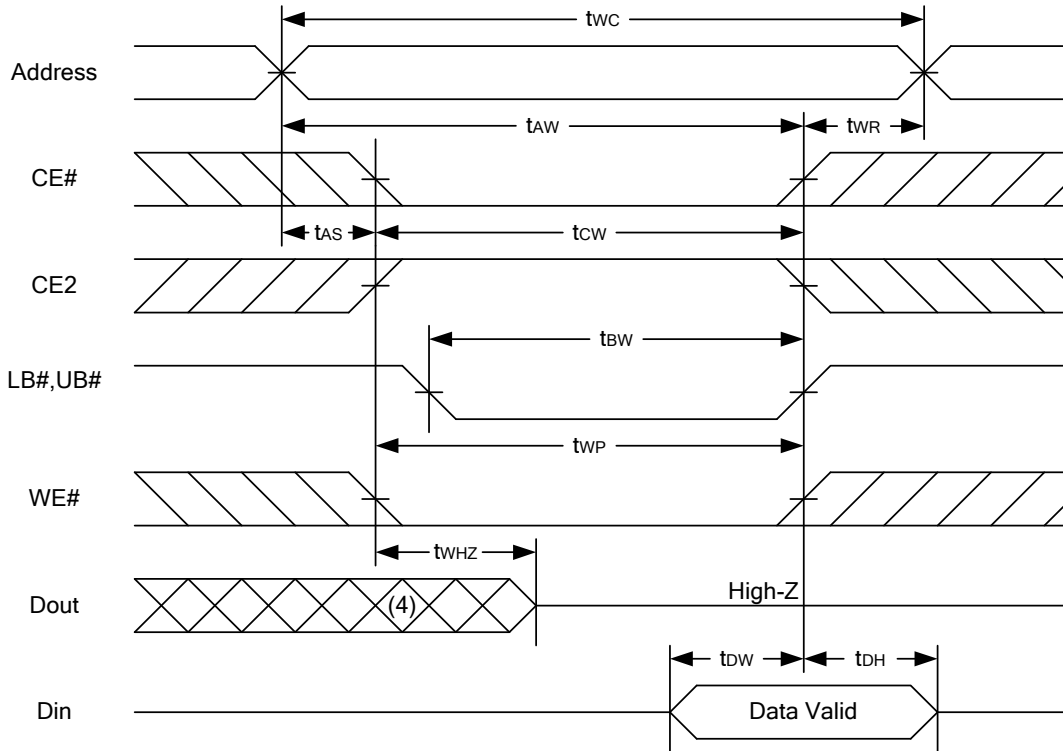


WRITE CYCLE 2 (CE# and CE2 Controlled) (1,4,5)





WRITE CYCLE 3 (LB#,UB# Controlled) (1,4,5)



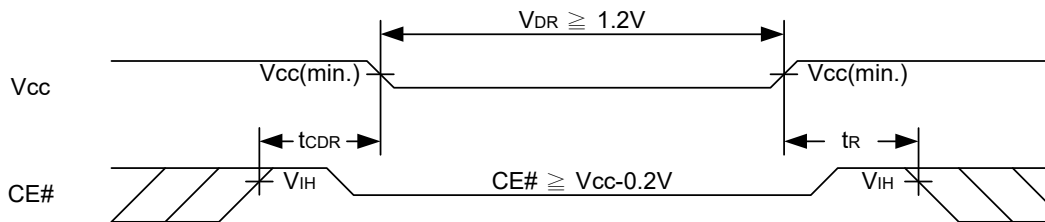
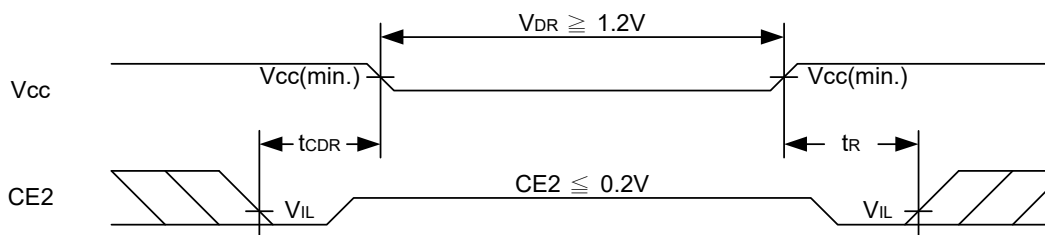
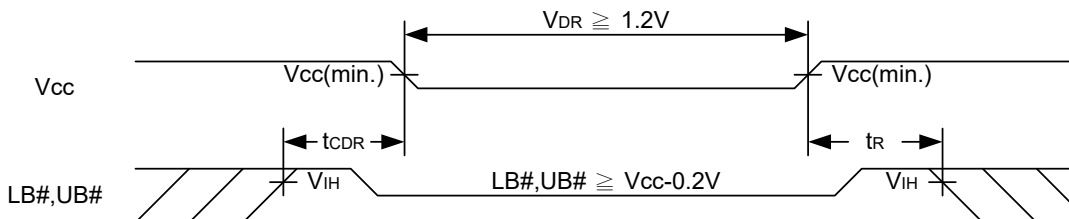
Notes :

1. A write occurs during the overlap of a low CE#, high CE2, low WE#, LB# or UB# = low.
2. During a WE# controlled write cycle with OE# low, t_{WP} must be greater than $t_{WHZ} + t_{cW}$ to allow the drivers to turn off and data to be placed on the bus.
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the CE#, LB#, UB# low transition and CE2 high transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
5. t_{cW} and t_{WHZ} are specified with $C_L = 5pF$. Transition is measured $\pm 500mV$ from steady state.

DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT		
V _{CC} for Data Retention	V _{DR}	CE# ≥ V _{CC} - 0.2V or CE2 ≤ 0.2V	1.2	-	3.6	V		
Data Retention Current	I _{DR}	V _{CC} = 1.2V CE# ≥ V _{CC} - 0.2V or CE2 ≤ 0.2V other pins at 0.2V or V _{CC} - 0.2V	LL	-	4	50	μA	
			LLE	-	4	60	μA	
			LLI	-	4	80	μA	
			SL	25°C	-	2.5	5	μA
			SLE	40°C	-	2.5	5	μA
			SLI		-	2.5	5	μA
			SL/SLE	-	2.5	30	μA	
SLI	-	2.5	40	μA				
Chip Disable to Data Retention Time	t _{CDR}	See Data Retention Waveforms (below)	0	-	-	ns		
Recovery Time	t _R		t _{RC} *	-	-	ns		

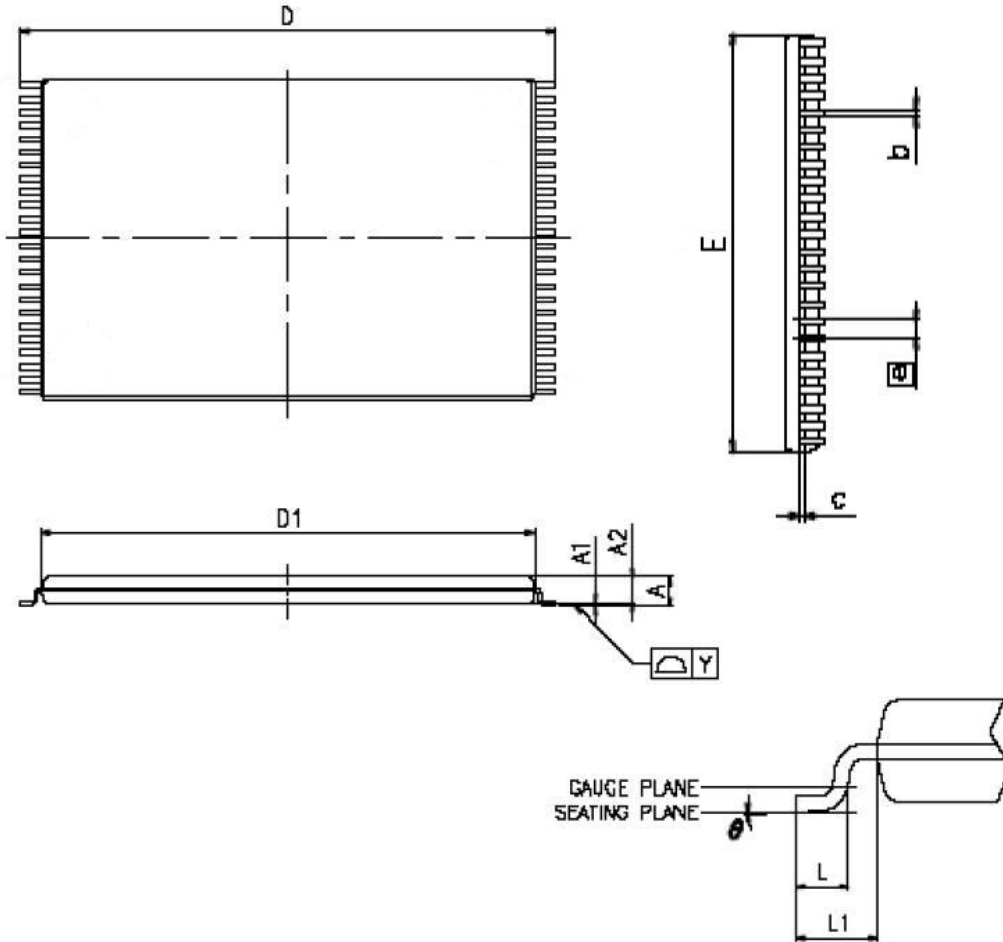
 t_{RC}* = Read Cycle Time

DATA RETENTION WAVEFORM
Low V_{CC} Data Retention Waveform (1) (CE# controlled)

Low V_{CC} Data Retention Waveform (2) (CE2 controlled)

Low V_{CC} Data Retention Waveform (3) (LB#, UB# controlled)




PACKAGE OUTLINE DIMENSION

48-pin 12mm x 20mm TSOP-I Package Outline Dimension

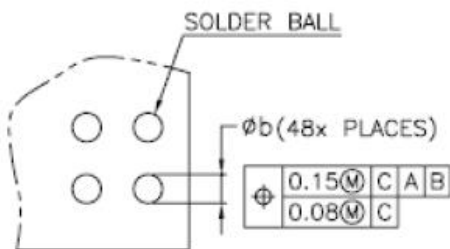
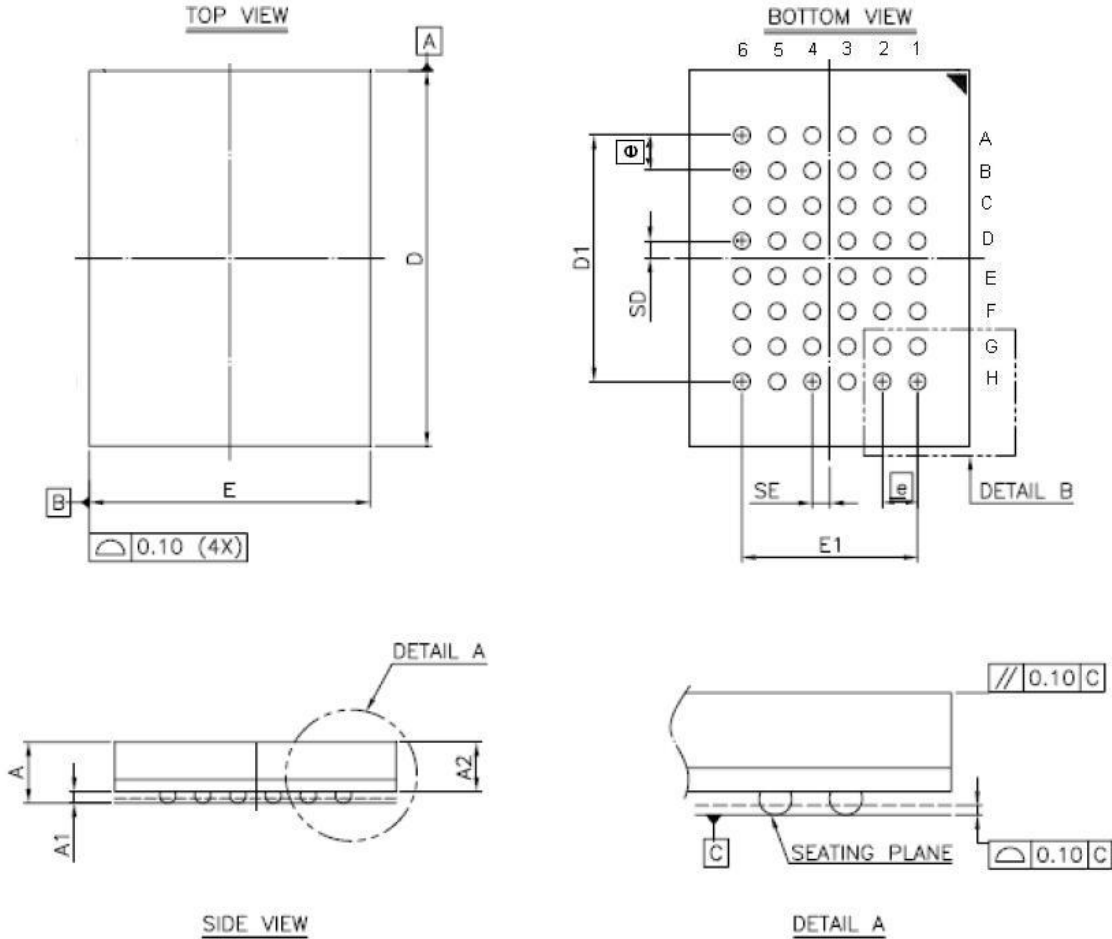


VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX
A	-	-	1.20
A1	0.05	-	0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
c	0.10	-	0.21
D	19.80	20.00	20.20
D1	18.30	18.40	18.50
E	11.90	12.00	12.10
ϵ	0.50 BASIC		
L	0.50	0.60	0.70
L1	-	0.80	-
Y	-	-	0.10
θ	θ	-	5°

NOTES:

- 1 JEDEC OUTLINE : MO-142 DD
2. PROFILE TOLERANCE ZONES FOR D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION ON E IS 0.15mm PER SIDE AND ON D1 IS 0.25mm PER SIDE.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

48-ball 6mm × 8mm TFBGA Package Outline Dimension

DETAIL B

SYM.	DIMENSION (mm)			DIMENSION (inch)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.40	—	—	0.055
A1	0.20	0.25	0.30	0.008	0.010	0.012
A2	—	—	1.05	—	—	0.041
b	0.30	0.35	0.40	0.012	0.014	0.016
D	7.95	8.00	8.05	0.313	0.315	0.317
D1	5.25 BSC			0.207 BSC		
E	5.95	6.00	6.05	0.234	0.236	0.238
E1	3.75 BSC			0.148 BSC		
SE	0.375 TYP			0.015 TYP		
SD	0.375 TYP			0.015 TYP		
\square	0.75 BSC			0.030 BSC		

NOTE:

1. CONTROLLING DIMENSION : MILLIMETER.
2. REFERENCE DOCUMENT : JEDEC MO-207.



ORDERING INFORMATION

Package Type	Access Time (Speed)(ns)	Power Type	Temperature Range(°C)	Packing Type	Lyontek Item No.
48-Pin 12mmx20mm TSOP-I	55	Ultra Low Power	0°C~70°C	Tray	LY62L102516LL-55LL
				Tape Reel	LY62L102516LL-55LLT
			-20°C~80°C	Tray	LY62L102516LL-55LLE
				Tape Reel	LY62L102516LL-55LLET
			-40°C~85°C	Tray	LY62L102516LL-55LLI
				Tape Reel	LY62L102516LL-55LLIT
	70	Ultra Low Power	0°C~70°C	Tray	LY62L102516LL-70LL
				Tape Reel	LY62L102516LL-70LLT
			-20°C~80°C	Tray	LY62L102516LL-70LLE
				Tape Reel	LY62L102516LL-70LLET
			-40°C~85°C	Tray	LY62L102516LL-70LLI
				Tape Reel	LY62L102516LL-70LLIT
48-ball 6mmx8mm TFBGA	55	Special Ultra Low Power	0°C~70°C	Tray	LY62L102516GL-55SL
				Tape Reel	LY62L102516GL-55SLT
			-20°C~80°C	Tray	LY62L102516GL-55SLE
				Tape Reel	LY62L102516GL-55SLET
			-40°C~85°C	Tray	LY62L102516GL-55SLI
				Tape Reel	LY62L102516GL-55SLIT
	70	Special Ultra Low Power	0°C~70°C	Tray	LY62L102516GL-70SL
				Tape Reel	LY62L102516GL-70SLT
			-20°C~80°C	Tray	LY62L102516GL-70SLE
				Tape Reel	LY62L102516GL-70SLET
			-40°C~85°C	Tray	LY62L102516GL-70SLI
				Tape Reel	LY62L102516GL-70SLIT



Lyontek Inc.

LY62L102516

Rev. 1.1

1024K X 16 BIT LOW POWER CMOS SRAM

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