



REVISION HISTORY

<u>Revision</u>	<u>Description</u>	<u>Issue Date</u>
Rev. 1.0	Initial Issue	Jun.08.2017
Rev. 1.1	Revised typo in <u>TIMING WAVEFORMS</u> of WRITE CYCLE in page 6 & 7	Jul.30.2020

FEATURE

- Fast access time : 55ns
- Low power consumption:
Operating current : 12mA (TYP.)
Standby current : 8 μ A (TYP.)
- Single 2.7V ~ 3.6V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data byte control : LB# (DQ0 ~ DQ7)
UB# (DQ8 ~ DQ15)
- Data retention voltage : 1.2V (MIN.)
- **Green package available**
- Package : 48-ball 8mm x 10mm TFBGA

GENERAL DESCRIPTION

The LY62L204916B is a 33,554,432-bit low power CMOS static random access memory organized as 2,097,152 words by 16 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

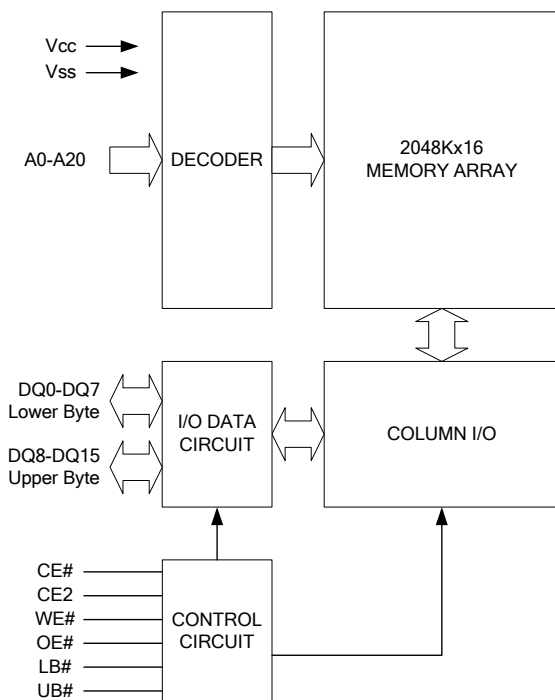
The LY62L204916B is well designed for low power application, and particularly well suited for battery back-up nonvolatile memory application.

The LY62L204916B operates from a single power supply of 2.7V ~ 3.6V and all inputs and outputs are fully TTL compatible

PRODUCT FAMILY

Product Family	Operating Temperature	V _{CC} Range	Speed	Power Dissipation	
				Standby(I _{SB1} , TYP.)	Operating(I _{CC} , TYP.)
LY62L204916B	0 ~ 70°C	2.7 ~ 3.6V	55ns	8 μ A	12mA
LY62L204916B(I)	-40 ~ 85°C	2.7 ~ 3.6V	55ns	8 μ A	12mA

FUNCTIONAL BLOCK DIAGRAM

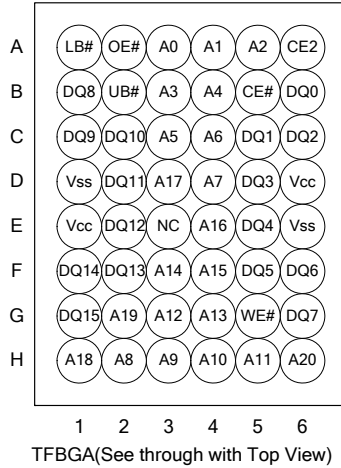


PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A20	Address Inputs
DQ0 - DQ15	Data Inputs/Outputs
CE#, CE2	Chip Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
LB#	Lower Byte Control
UB#	Upper Byte Control
V _{CC}	Power Supply
V _{SS}	Ground
NC	No Connection



PIN CONFIGURATION



TFBGA(Top View)

ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on V _{CC} relative to V _{SS}	V _{T1}	-0.5 to 4.6	V
Voltage on any other pin relative to V _{SS}	V _{T2}	-0.5 to V _{CC} +0.5	V
Operating Temperature	T _A	0 to 70(C grade)	°C
		-40 to 85(I grade)	
Storage Temperature	T _{STG}	-65 to 150	°C
Power Dissipation	P _D	1	W
DC Output Current	I _{OUT}	50	mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE#	CE2	OE#	WE#	LB#	UB#	I/O OPERATION		SUPPLY CURRENT
							DQ0 - DQ7	DQ8 - DQ15	
Standby	H	X	X	X	X	X	High-Z	High-Z	I _{SB1}
	X	L	X	X	X	X	High-Z	High-Z	
	X	X	X	X	H	H	High-Z	High-Z	
Output Disable	L	H	H	H	L	X	High-Z	High-Z	I _{CC} , I _{CC1}
	L	H	H	H	X	L	High-Z	High-Z	
Read	L	H	L	H	L	H	D _{OUT}	High-Z	I _{CC} , I _{CC1}
	L	H	L	H	H	L	High-Z	D _{OUT}	
	L	H	L	H	L	L	D _{OUT}	D _{OUT}	
Write	L	H	X	L	L	H	D _{IN}	High-Z	I _{CC} , I _{CC1}
	L	H	X	L	H	L	High-Z	D _{IN}	
	L	H	X	L	L	L	D _{IN}	D _{IN}	

Note: H= V_{IH}, L= V_{IL}, X= Don't care.



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.* ⁴	MAX.	UNIT		
Supply Voltage	V _{CC}		2.7	3.0	3.6	V		
Input High Voltage	V _{IH} ^{*1}		2.2	-	V _{CC} +0.3	V		
Input Low Voltage	V _{IL} ^{*2}		- 0.2	-	0.6	V		
Input Leakage Current	I _{LI}	V _{CC} ≥ V _{IN} ≥ V _{SS}	- 1	-	1	μA		
Output Leakage Current	I _{LO}	V _{CC} ≥ V _{OUT} ≥ V _{SS} Output Disabled	- 1	-	1	μA		
Output High Voltage	V _{OH}	I _{OH} = -1mA	2.2	2.7	-	V		
Output Low Voltage	V _{OL}	I _{OL} = 2mA	-	-	0.4	V		
Average Operating Power supply Current	I _{CC}	Cycle time = MIN. CE# ≤ 0.2V and CE2 ≥ V _{CC} -0.2V, I _{I/O} = 0mA Other pins at 0.2V or V _{CC} -0.2V	-	12	20	mA		
	I _{CC1}	Cycle time = 1μs CE# ≤ 0.2V and CE2 ≥ V _{CC} -0.2V, I _{I/O} = 0mA Other pins at 0.2V or V _{CC} -0.2V	-	3	5	mA		
Standby Power Supply Current	I _{SB1}	CE# ≥ V _{CC} -0.2V or CE2 ≤ 0.2V Others at 0.2V or V _{CC} -0.2V	-SL ^{*5}	25°C	-	8	16	μA
			-SLI ^{*5}	40°C	-	8	18	μA
			-SL ^{*6}		-	-	50	μA
			-SLI ^{*7}		-	-	80	μA

Notes:

- V_{IH}(max) = V_{CC} + 2.0V for pulse width less than 6ns.
- V_{IL}(min) = V_{SS} - 2.0V for pulse width less than 6ns.
- Over/Undershoot specifications are characterized on engineering evaluation stage, not for mass production test.
- Typical values, measured at V_{CC} = V_{CC}(TYP.) and T_A = 25°C, are included for reference only and are not guaranteed or tested.
- This parameter is measured at V_{CC}=3.0V.
- This parameter is measured at T_A = 70°C
- This parameter is measured at T_A = 85°C

CAPACITANCE (T_A = 25°C, f = 1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Input Capacitance	C _{IN}	-	8	pF
Input/Output Capacitance	C _{I/O}	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.



AC TEST CONDITIONS

Input Pulse Levels	0.2V to $V_{CC} - 0.2V$
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	$C_L = 30pF + 1TTL, I_{OH}/I_{OL} = -1mA/2mA$

AC ELECTRICAL CHARACTERISTICS

(1) READ CYCLE

PARAMETER	SYM.	LY62L204916B-55		UNIT
		MIN.	MAX.	
Read Cycle Time	t_{RC}	55	-	ns
Address Access Time	t_{AA}	-	55	ns
Chip Enable Access Time	t_{ACE}	-	55	ns
Output Enable Access Time	t_{OE}	-	30	ns
Chip Enable to Output in Low-Z	t_{CLZ}^*	10	-	ns
Output Enable to Output in Low-Z	t_{OLZ}^*	5	-	ns
Chip Disable to Output in High-Z	t_{CHZ}^*	-	20	ns
Output Disable to Output in High-Z	t_{OHZ}^*	-	20	ns
Output Hold from Address Change	t_{OH}	10	-	ns
LB#, UB# Access Time	t_{BA}	-	55	ns
LB#, UB# to High-Z Output	t_{BHZ}^*	-	20	ns
LB#, UB# to Low-Z Output	t_{BLZ}^*	10	-	ns

(2) WRITE CYCLE

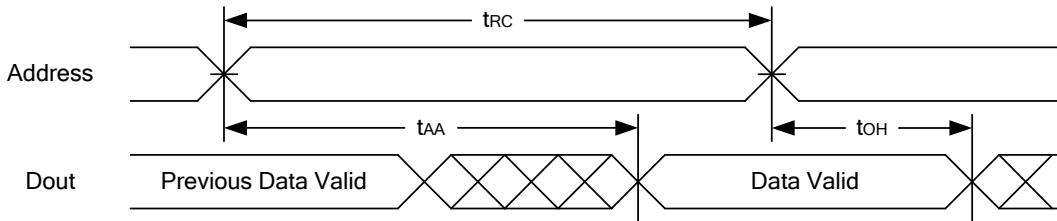
PARAMETER	SYM.	LY62L204916B-55		UNIT
		MIN.	MAX.	
Write Cycle Time	t_{WC}	55	-	ns
Address Valid to End of Write	t_{AW}	50	-	ns
Chip Enable to End of Write	t_{CW}	50	-	ns
Address Set-up Time	t_{AS}	0	-	ns
Write Pulse Width	t_{WP}	45	-	ns
Write Recovery Time	t_{WR}	0	-	ns
Data to Write Time Overlap	t_{DW}	25	-	ns
Data Hold from End of Write Time	t_{DH}	0	-	ns
Output Active from End of Write	t_{OW}^*	5	-	ns
Write to Output in High-Z	t_{WHZ}^*	-	20	ns
LB#, UB# Valid to End of Write	t_{BW}	50	-	ns

*These parameters are guaranteed by device characterization, but not production tested.

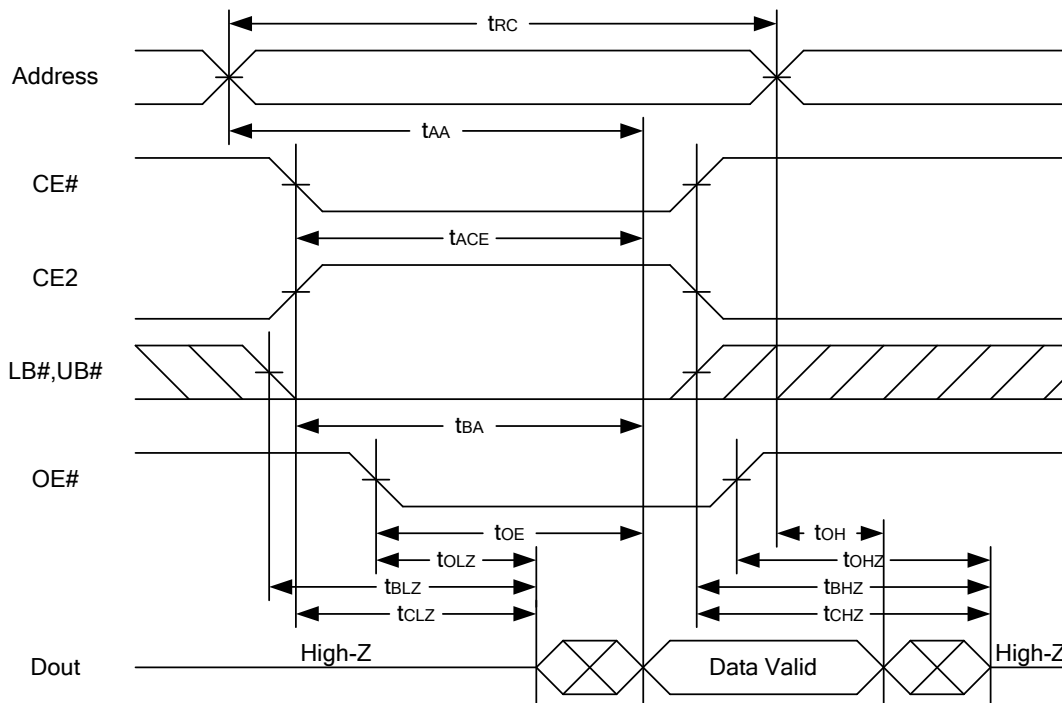


TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)



READ CYCLE 2 (CE# and CE2 and OE# Controlled) (1,3,4,5)

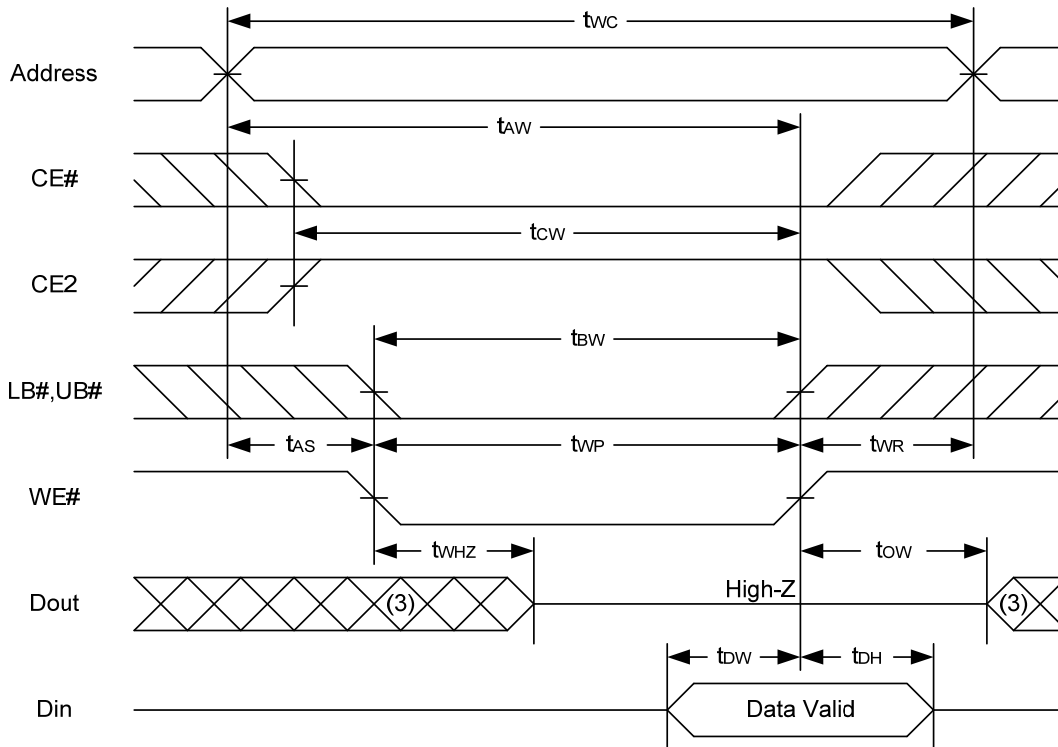


Notes :

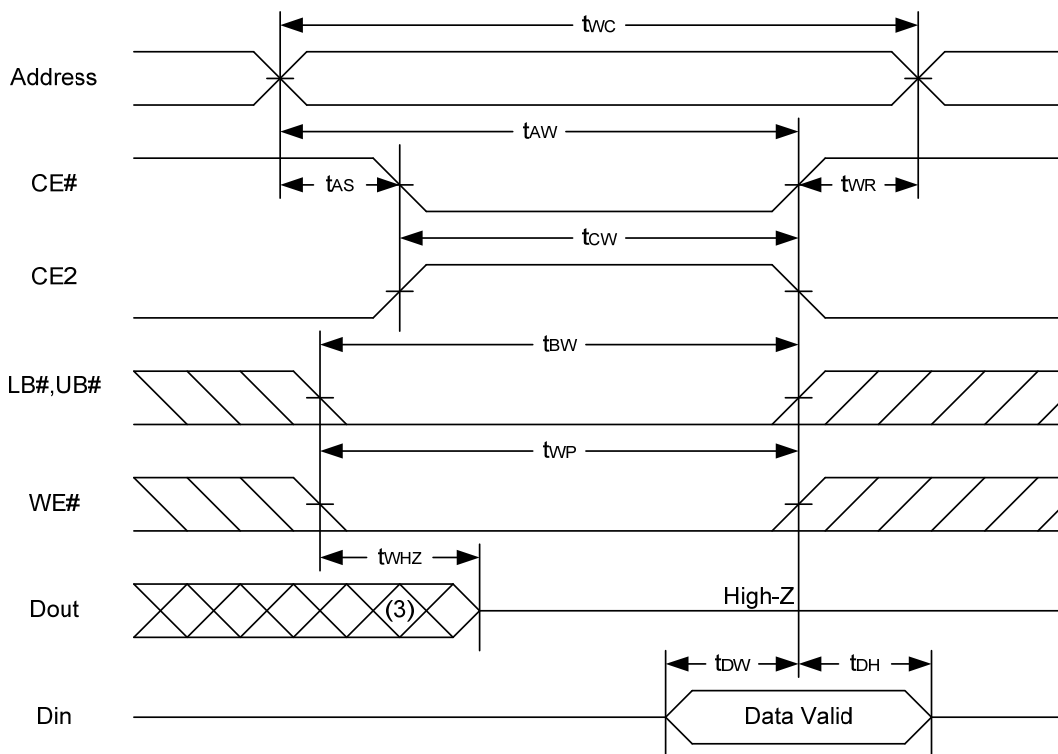
1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low, CE2 = high, LB# or UB# = low.
3. Address must be valid prior to or coincident with CE# = low, CE2 = high, LB# or UB# = low transition; otherwise tAA is the limiting parameter.
4. tCLZ, tBLZ, tOLZ, tCHZ, tBHZ and tOHZ are specified with CL = 5pF. Transition is measured ±500mV from steady state.
5. At any given temperature and voltage condition, tCHZ is less than tCLZ, tBHZ is less than tBLZ, tOHZ is less than tOLZ.



WRITE CYCLE 1 (WE# Controlled) (1,2,4,5)

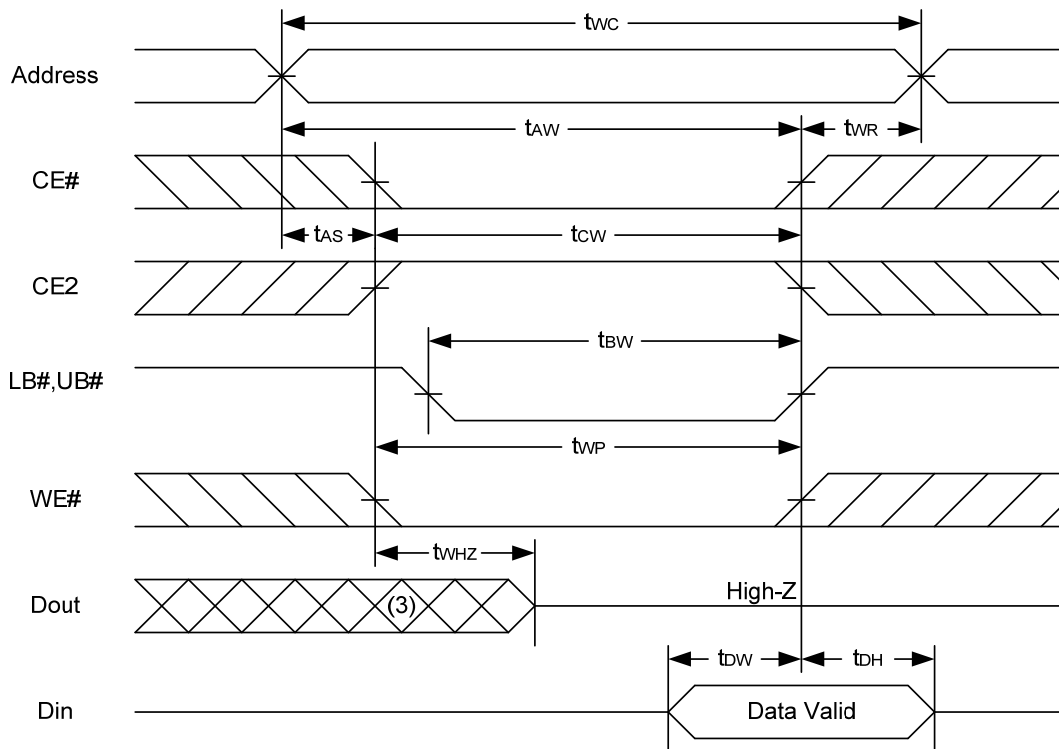


WRITE CYCLE 2 (CE# and CE2 Controlled) (1,4,5)





WRITE CYCLE 3 (LB#,UB# Controlled) (1,4,5)



Notes :

1. A write occurs during the overlap of a low CE#, high CE2, low WE#, LB# or UB# = low.
2. During a WE# controlled write cycle with OE# low, t_{wP} must be greater than $t_{wHZ} + t_{DW}$ to allow the drivers to turn off and data to be placed on the bus.
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the CE#, LB#, UB# low transition and CE2 high transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
5. t_{ow} and t_{wHZ} are specified with $C_L = 5pF$. Transition is measured $\pm 500mV$ from steady state.



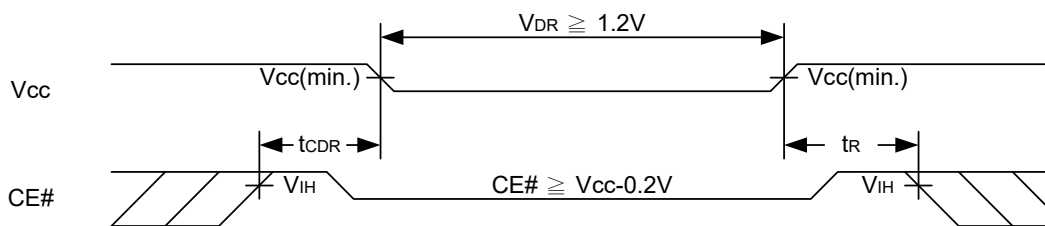
DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT		
V _{CC} for Data Retention	V _{DR}	CE# ≥ V _{CC} - 0.2V or CE2 ≤ 0.2V	1.2	-	3.6	V		
Data Retention Current	I _{DR}	V _{CC} = 1.2V CE# ≥ V _{CC} -0.2V or CE2 ≤ 0.2V Other pins at 0.2V or V _{CC} -0.2V	-SL	25°C	-	6.5	16	μA
			-SLI	40°C	-	6.5	18	μA
			-SL		-	-	50	μA
			-SLI		-	-	80	μA
Chip Disable to Data Retention Time	t _{CDR}	See Data Retention Waveforms (below)	0	-	-	ns		
Recovery Time	t _R		t _{RC} *	-	-	ns		

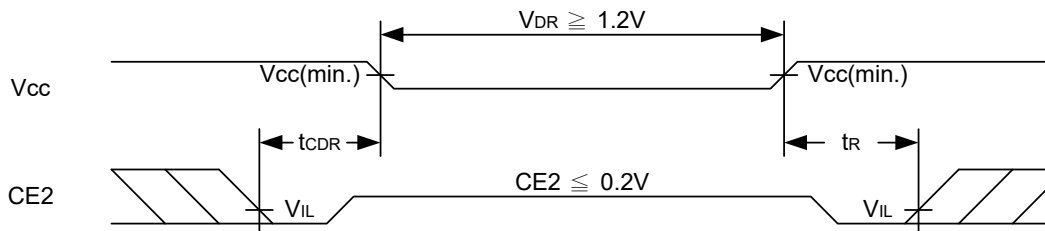
t_{RC}* = Read Cycle Time

DATA RETENTION WAVEFORM

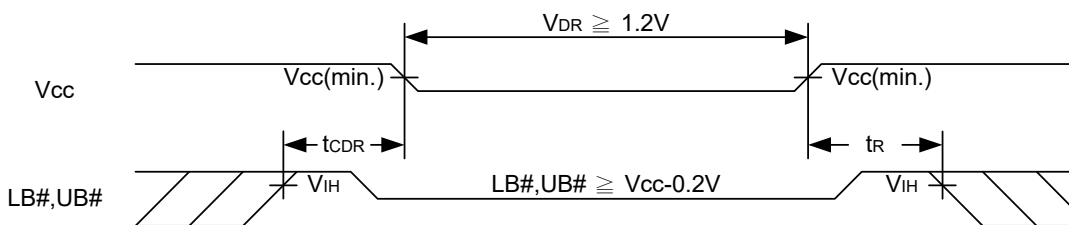
Low V_{CC} Data Retention Waveform (1) (CE# controlled)



Low V_{CC} Data Retention Waveform (2) (CE2 controlled)

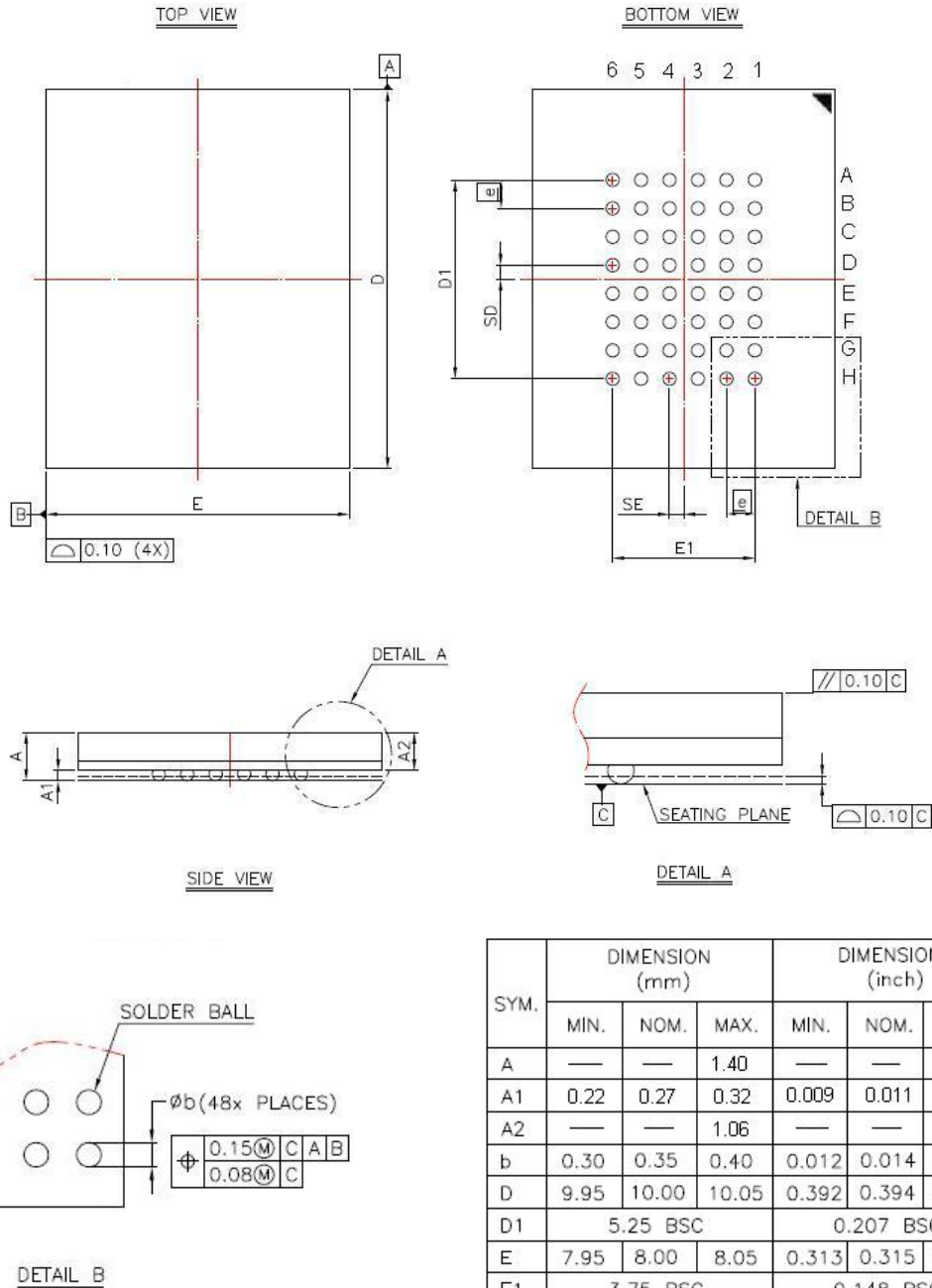


Low V_{CC} Data Retention Waveform (3) (LB#, UB# controlled)



PACKAGE OUTLINE DIMENSION

48-ball 8mm × 10mm TFBGA Package Outline Dimension



SYM.	DIMENSION (mm)			DIMENSION (inch)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.40	—	—	0.055
A1	0.22	0.27	0.32	0.009	0.011	0.013
A2	—	—	1.06	—	—	0.042
b	0.30	0.35	0.40	0.012	0.014	0.016
D	9.95	10.00	10.05	0.392	0.394	0.396
D1	5.25 BSC			0.207 BSC		
E	7.95	8.00	8.05	0.313	0.315	0.317
E1	3.75 BSC			0.148 BSC		
SE	0.375 TYP			0.015 TYP		
SD	0.375 TYP			0.015 TYP		
Ⓜ	0.75 BSC			0.030 BSC		

NOTE:
 1. CONTROLLING DIMENSION : MILLIMETER.
 2. REFERENCE DOCUMENT : JEDEC MO-207.



ORDERING INFORMATION

Package Type	Access Time (Speed)(ns)	Power Type	Temperature Range(°C)	Packing Type	Lyontek Item No.
48-ball (8mm x 10mm) TFBGA	55	Special Ultra Low Power	0°C~70°C	Tray	LY62L204916BGL-55SL
				Tape Reel	LY62L204916BGL-55SLT
			-40°C~85°C	Tray	LY62L204916BGL-55SLI
				Tape Reel	LY62L204916BGL-55SLIT



Lyontek Inc.

LY62L204916B

Rev. 1.1

2048K X 16 BITS LOW POWER CMOS SRAM

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