



#### REVISION HISTORY

<u>Revision</u>	<u>Description</u>	<u>Issue Date</u>
Rev. 1.0	Initial Issue	Jul.25.2004
Rev. 1.1	Revised <b>STSOP Package Outline Dimension</b>	Mar.26.2008
Rev. 1.2	Deleted L Spec. Revised $V_{TERM}$ to $V_{T1}$ and $V_{T2}$ Revised Test Condition of $I_{SB1}/I_{DR}$ Revised <b>FEATURES &amp; ORDERING INFORMATION</b> <b><u>Lead free and green package available</u> to <u>Green package available</u></b> Added packing type in <b><u>ORDERING INFORMATION</u></b> Deleted $T_{SOLDER}$ in <b><u>ABSOLUTE MAXIMUM RATINGS</u></b>	Apr.13.2009

### FEATURES

- Fast access time : 35/55/70ns
- Low power consumption:  
Operating current : 20/15/10mA (TYP.)  
Standby current : 0.5 $\mu$ A (TYP.) LL-version
- Single 2.7V ~ 3.6V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data retention voltage : 1.5V (MIN.)
- **Green package available**
- Package : 28-pin 600 mil PDIP  
28-pin 330 mil SOP  
28-pin 8mm x 13.4mm STSOP

### GENERAL DESCRIPTION

The LY62L256 is a 262,144-bit low power CMOS static random access memory organized as 32,768 words by 8 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

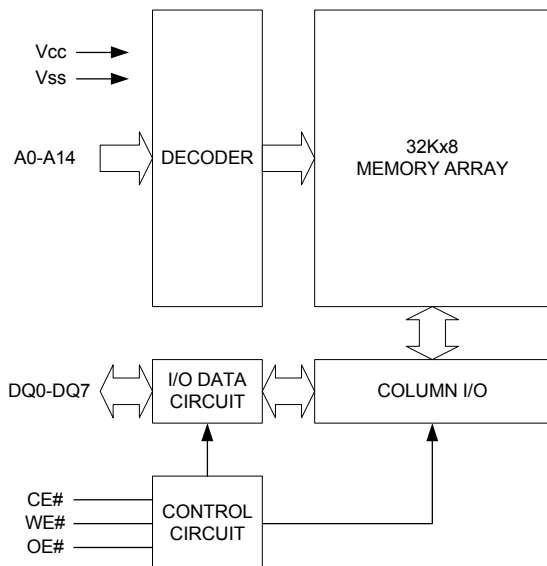
The LY62L256 is well designed for low power application, and particularly well suited for battery back-up nonvolatile memory application.

The LY62L256 operates from a single power supply of 2.7V ~ 3.6V and all inputs and outputs are fully TTL compatible

### PRODUCT FAMILY

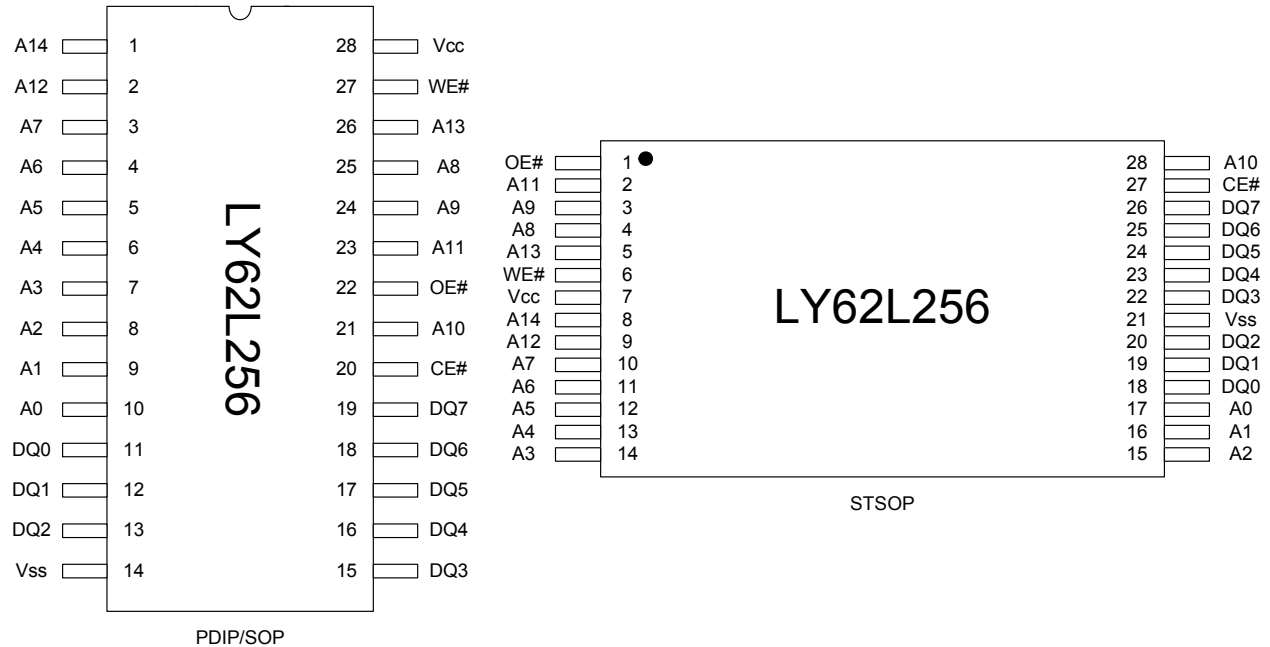
Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation	
				Standby(I <sub>SB1</sub> ,TYP.)	Operating(I <sub>CC</sub> ,TYP.)
LY62L256	0 ~ 70°C	2.7 ~ 3.6V	35/55/70ns	0.5 $\mu$ A(LL)	20/15/10mA
LY62L256(E)	-20 ~ 80°C	2.7 ~ 3.6V	35/55/70ns	0.5 $\mu$ A(LL)	20/15/10mA
LY62L256(I)	-40 ~ 85°C	2.7 ~ 3.6V	35/55/70ns	0.5 $\mu$ A(LL)	20/15/10mA

### FUNCTIONAL BLOCK DIAGRAM



### PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A14	Address Inputs
DQ0 - DQ7	Data Inputs/Outputs
CE#	Chip Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
Vcc	Power Supply
Vss	Ground

**PIN CONFIGURATION**

**ABSOLUTE MAXIMUM RATINGS\***

PARAMETER	SYMBOL	RATING	UNIT
Voltage on Vcc relative to Vss	V <sub>T1</sub>	-0.5 to 4.6	V
Voltage on any other pin relative to Vss	V <sub>T2</sub>	-0.5 to V <sub>CC</sub> +0.5	V
Operating Temperature	T <sub>A</sub>	0 to 70(C grade)	°C
		-20 to 80(E grade)	
		-40 to 85(I grade)	
Storage Temperature	T <sub>STG</sub>	-65 to 150	°C
Power Dissipation	P <sub>D</sub>	1	W
DC Output Current	I <sub>OUT</sub>	50	mA

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

**TRUTH TABLE**

MODE	CE#	OE#	WE#	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	High-Z	I <sub>SB</sub> , I <sub>SB1</sub>
Output Disable	L	H	H	High-Z	I <sub>CC</sub> , I <sub>CC1</sub>
Read	L	L	H	D <sub>OUT</sub>	I <sub>CC</sub> , I <sub>CC1</sub>
Write	L	X	L	D <sub>IN</sub>	I <sub>CC</sub> , I <sub>CC1</sub>

Note: H = V<sub>IH</sub>, L = V<sub>IL</sub>, X = Don't care.

**DC ELECTRICAL CHARACTERISTICS**

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP. <sup>5</sup>	MAX.	UNIT	
Supply Voltage	V <sub>CC</sub>		2.7	3.3	3.6	V	
Input High Voltage	V <sub>IH</sub> <sup>1</sup>		2.0	-	V <sub>CC</sub> +0.5	V	
Input Low Voltage	V <sub>IL</sub> <sup>2</sup>		- 0.5	-	0.6	V	
Input Leakage Current	I <sub>LI</sub>	V <sub>CC</sub> ≥ V <sub>IN</sub> ≥ V <sub>SS</sub>	- 1	-	1	μA	
Output Leakage Current	I <sub>LO</sub>	V <sub>CC</sub> ≥ V <sub>OUT</sub> ≥ V <sub>SS</sub> , Output Disabled	- 1	-	1	μA	
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -1mA	2.4	3.0	-	V	
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2mA	-	-	0.4	V	
Average Operating Power supply Current	I <sub>CC</sub>	Cycle time = Min. CE# = V <sub>IL</sub> , I <sub>I/O</sub> = 0mA Other pins at V <sub>IL</sub> or V <sub>IH</sub>	-35	-	20	40	mA
			-55	-	15	30	mA
			-70	-	10	20	mA
Average Operating Power supply Current	I <sub>CC1</sub>	Cycle time = 1μs CE# ≤ 0.2V and I <sub>I/O</sub> = 0mA other pins at 0.2V or V <sub>CC</sub> -0.2V	-	3	6	mA	
Standby Power Supply Current	I <sub>SB</sub>	CE# = V <sub>IH</sub> , others at V <sub>IL</sub> or V <sub>IH</sub>	-	1	3	mA	
	I <sub>SB1</sub>	CE# ≥ V <sub>CC</sub> - 0.2V Others at 0.2V or V <sub>CC</sub> - 0.2V	-LL	0.5	20 <sup>4</sup>	μA	

Notes:

- V<sub>IH</sub>(max) = V<sub>CC</sub> + 3.0V for pulse width less than 10ns.
- V<sub>IL</sub>(min) = V<sub>SS</sub> - 3.0V for pulse width less than 10ns.
- Over/Undershoot specifications are characterized, not 100% tested.
- 10μA for special request
- Typical values are included for reference only and are not guaranteed or tested.  
Typical values are measured at V<sub>CC</sub> = V<sub>CC</sub>(TYP.) and T<sub>A</sub> = 25°C

**CAPACITANCE (T<sub>A</sub> = 25°C, f = 1.0MHz)**

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C <sub>IN</sub>	-	6	pF
Input/Output Capacitance	C <sub>I/O</sub>	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

**AC TEST CONDITIONS**

Input Pulse Levels	0.2V to V <sub>CC</sub> - 0.2V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	C <sub>L</sub> = 30pF + 1TTL, I <sub>OH</sub> /I <sub>OL</sub> = -1mA/2mA



### AC ELECTRICAL CHARACTERISTICS

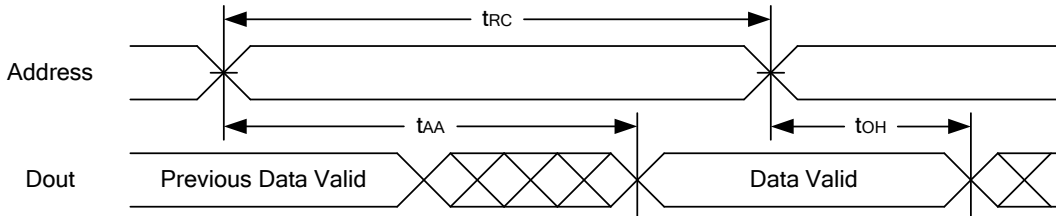
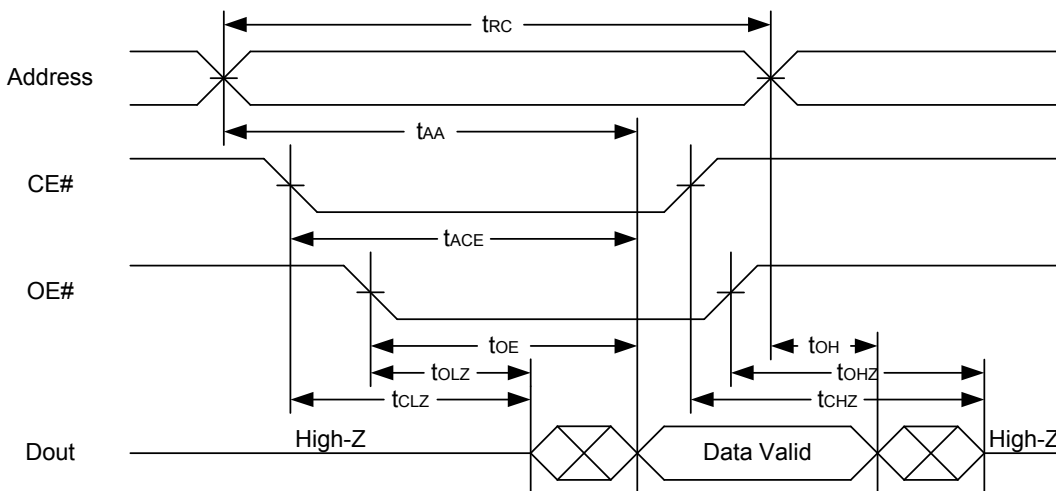
#### (1) READ CYCLE

PARAMETER	SYM.	LY62L256-35		LY62L256-55		LY62L256-70		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t <sub>RC</sub>	35	-	55	-	70	-	ns
Address Access Time	t <sub>AA</sub>	-	35	-	55	-	70	ns
Chip Enable Access Time	t <sub>ACE</sub>	-	35	-	55	-	70	ns
Output Enable Access Time	t <sub>OE</sub>	-	25	-	30	-	35	ns
Chip Enable to Output in Low-Z	t <sub>CLZ</sub> *	10	-	10	-	10	-	ns
Output Enable to Output in Low-Z	t <sub>OLZ</sub> *	5	-	5	-	5	-	ns
Chip Disable to Output in High-Z	t <sub>CHZ</sub> *	-	15	-	20	-	25	ns
Output Disable to Output in High-Z	t <sub>OHZ</sub> *	-	15	-	20	-	25	ns
Output Hold from Address Change	t <sub>OH</sub>	10	-	10	-	10	-	ns

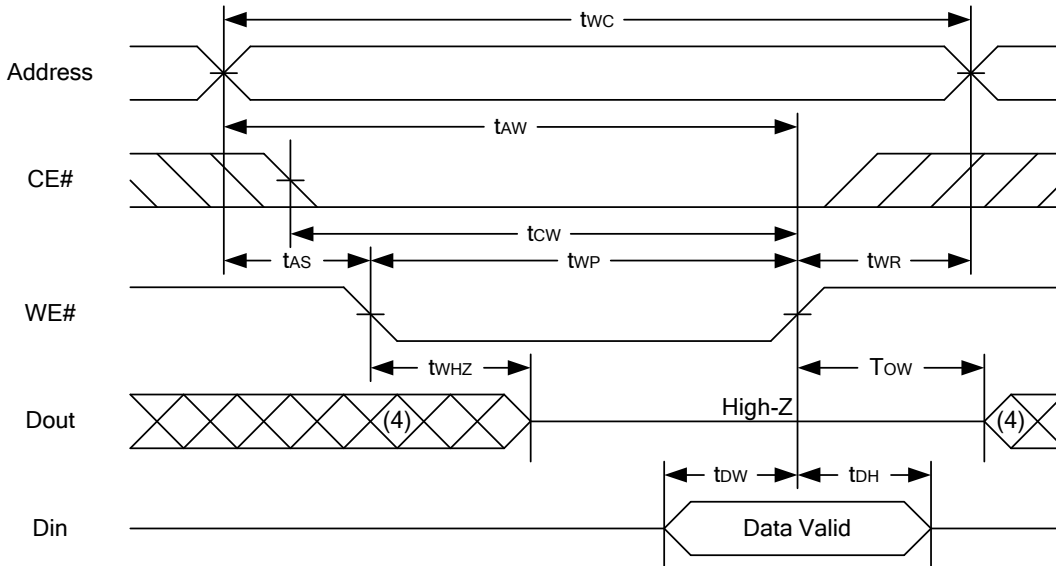
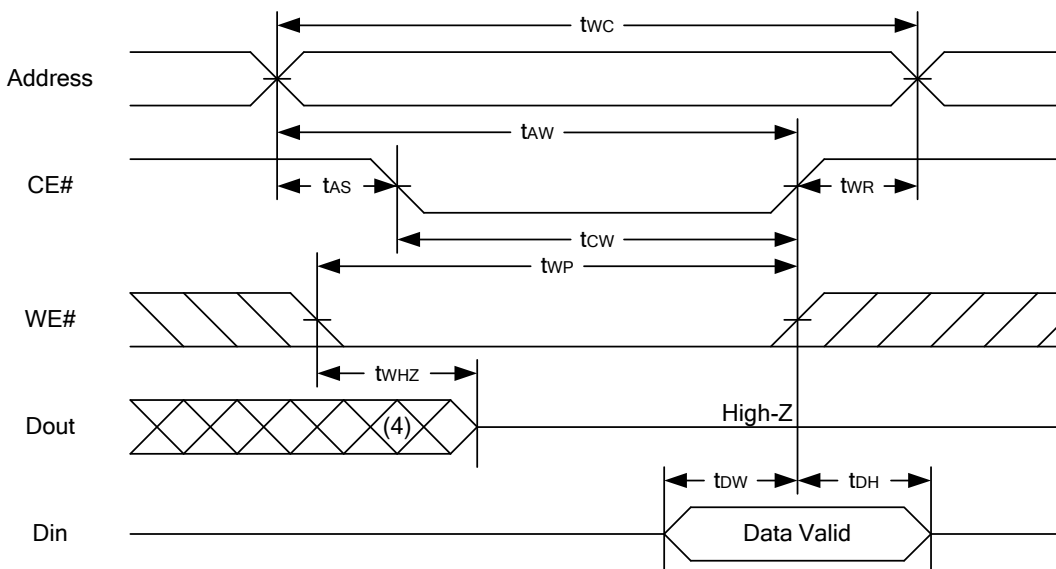
#### (2) WRITE CYCLE

PARAMETER	SYM.	LY62L256-35		LY62L256-55		LY62L256-70		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t <sub>WC</sub>	35	-	55	-	70	-	ns
Address Valid to End of Write	t <sub>AW</sub>	30	-	50	-	60	-	ns
Chip Enable to End of Write	t <sub>CW</sub>	30	-	50	-	60	-	ns
Address Set-up Time	t <sub>AS</sub>	0	-	0	-	0	-	ns
Write Pulse Width	t <sub>WP</sub>	25	-	45	-	55	-	ns
Write Recovery Time	t <sub>WR</sub>	0	-	0	-	0	-	ns
Data to Write Time Overlap	t <sub>DW</sub>	20	-	25	-	30	-	ns
Data Hold from End of Write Time	t <sub>DH</sub>	0	-	0	-	0	-	ns
Output Active from End of Write	t <sub>OW</sub> *	5	-	5	-	5	-	ns
Write to Output in High-Z	t <sub>WHZ</sub> *	-	15	-	20	-	25	ns

\*These parameters are guaranteed by device characterization, but not production tested.

**TIMING WAVEFORMS**
**READ CYCLE 1 (Address Controlled) (1,2)**

**READ CYCLE 2 (CE# and OE# Controlled) (1,3,4,5)**

**Notes :**

1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low.
3. Address must be valid prior to or coincident with CE# = low; otherwise tAA is the limiting parameter.
4. tCLZ, tOLZ, tCHZ and tOHZ are specified with CL = 5pF. Transition is measured ±500mV from steady state.
5. At any given temperature and voltage condition, tCHZ is less than tCLZ, tOHZ is less than tOLZ.

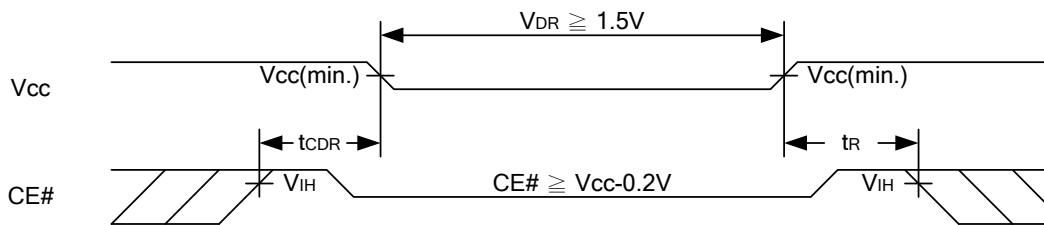
**WRITE CYCLE 1 (WE# Controlled) (1,2,3,5,6)**

**WRITE CYCLE 2 (CE# Controlled) (1,2,5,6)**

**Notes :**

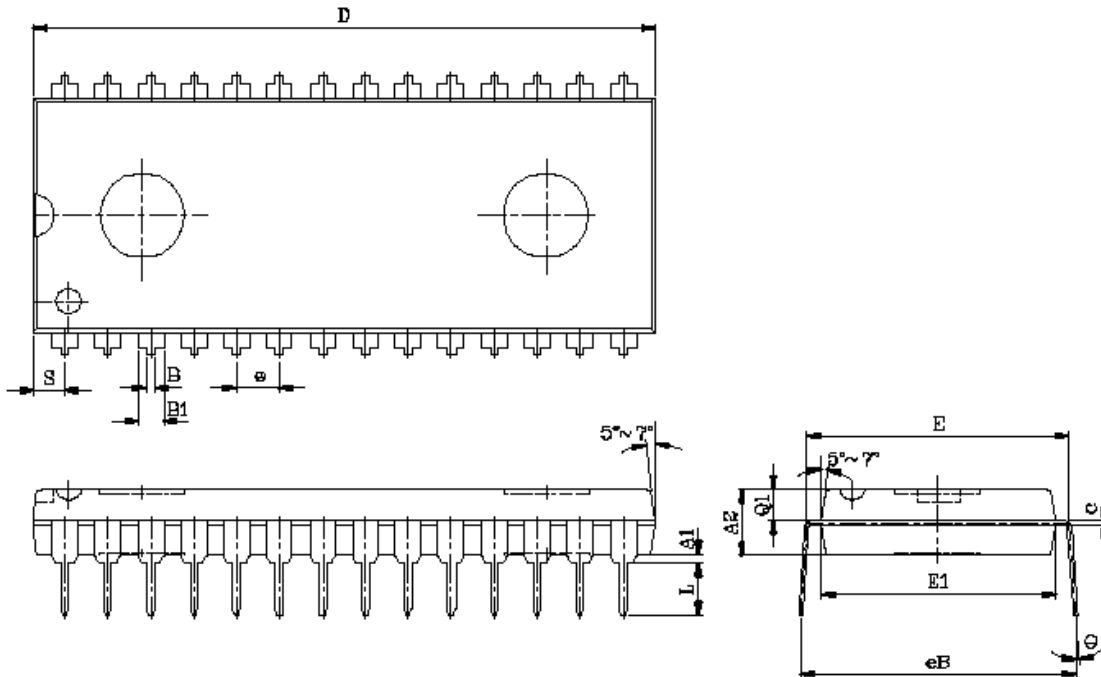
1. WE#, CE# must be high during all address transitions.
2. A write occurs during the overlap of a low CE#, low WE#.
3. During a WE# controlled write cycle with OE# low,  $t_{wp}$  must be greater than  $t_{whz} + t_{dw}$  to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the CE# low transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
6.  $t_{ow}$  and  $t_{whz}$  are specified with  $C_L = 5pF$ . Transition is measured  $\pm 500mV$  from steady state.

**DATA RETENTION CHARACTERISTICS**

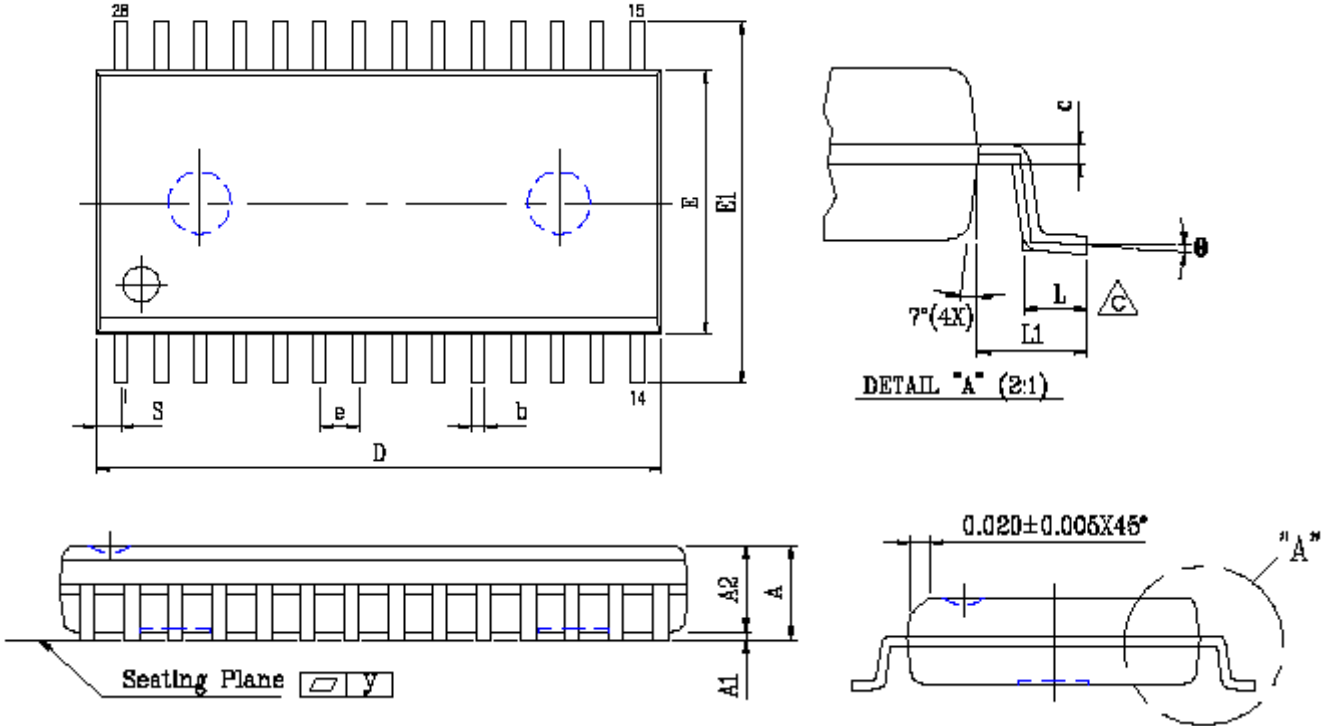
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
V <sub>CC</sub> for Data Retention	V <sub>DR</sub>	CE# ≥ V <sub>CC</sub> - 0.2V	1.5	-	3.6	V
Data Retention Current	I <sub>DR</sub>	V <sub>CC</sub> = 1.5V CE# ≥ V <sub>CC</sub> - 0.2V Others at 0.2V or V <sub>CC</sub> -0.2V	-	0.5	10	μA
Chip Disable to Data Retention Time	t <sub>CDR</sub>	See Data Retention Waveforms (below)	0	-	-	ns
Recovery Time	t <sub>R</sub>		t <sub>RC*</sub>	-	-	ns

 t<sub>RC\*</sub> = Read Cycle Time

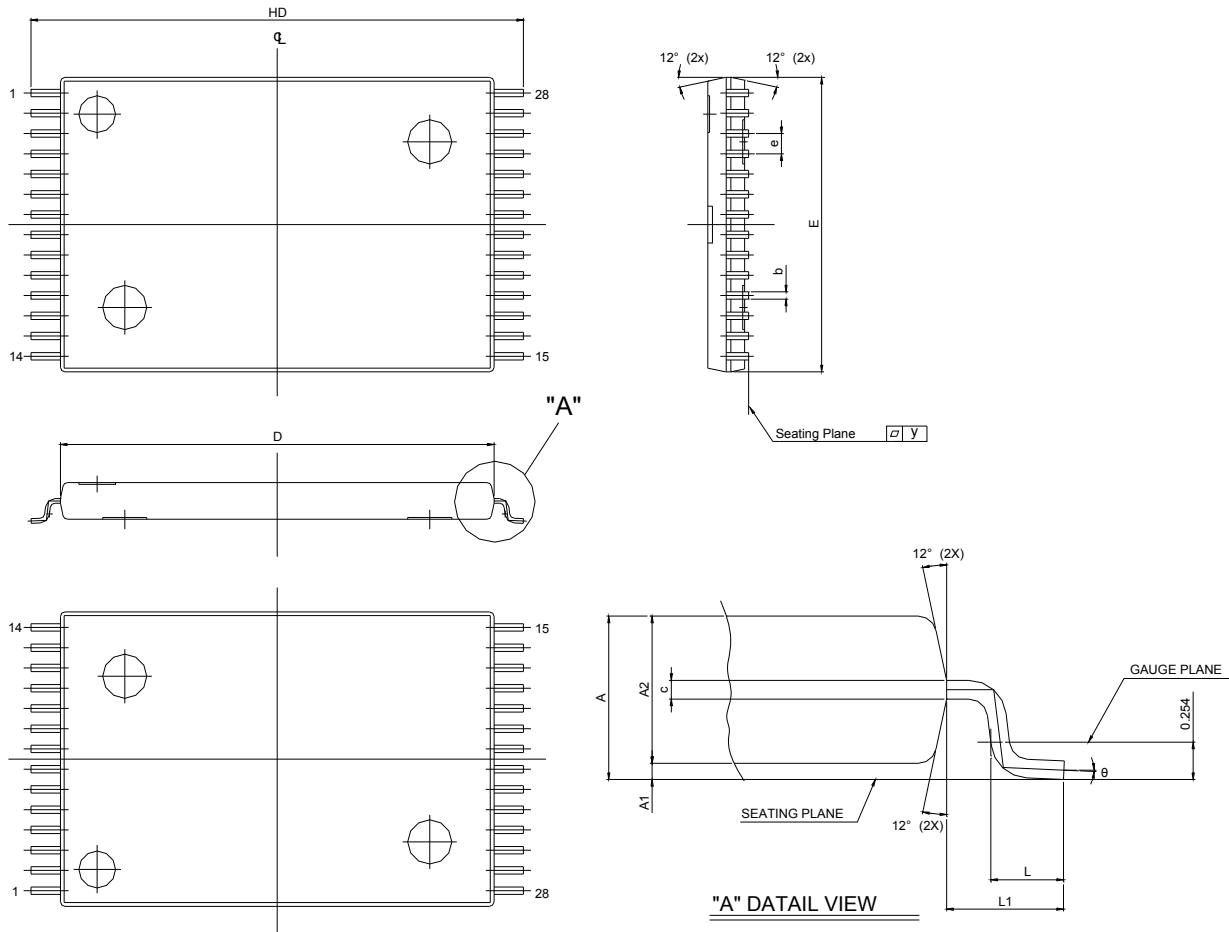
**DATA RETENTION WAVEFORM**


**PACKAGE OUTLINE DIMENSION**
**28 pin 600 mil PDIP Package Outline Dimension**


SYM.	UNIT	INCH.(BASE)	MM(REF)
A1		0.010 (MIN)	0.254 (MIN)
A2		0.150±0.005	3.810±0.127
B		0.020 (MAX)	0.508(MAX)
B1		0.055 (MAX)	1.397(MAX)
c		0.012 (MAX)	0.304 (MAX)
D		1.430 (MAX)	36.322 (MAX)
E		0.6 (TYP)	15.24 (TYP)
E1		0.52 (MAX)	13.208 (MAX)
e		0.100 (TYP)	2.540(TYP)
eB		0.625 (MAX)	15.87 (MAX)
L		0.180(MAX)	4.572(MAX)
S		0.06 (MAX)	1.524 (MAX)
Q1		0.08(MAX)	2.032(MAX)
Θ		15°(MAX)	15°(MAX)

**28 pin 330 mil SOP Package Outline Dimension**


SYM.	UNIT	INCH(BASE)	MM(REF)
A		0.120 (MAX)	3.048 (MAX)
A1		0.002(MIN)	0.05(MIN)
A2		0.098±0.005	2.489±0.127
b		0.016 (TYP)	0.406(TYP)
c		0.010 (TYP)	0.254(TYP)
D		0.728 (MAX)	18.491 (MAX)
E		0.340 (MAX)	8.636 (MAX)
E1		0.465±0.012	11.811±0.305
e		0.050 (TYP)	1.270(TYP)
L		0.05 (MAX)	1.270 (MAX)
L1		0.067±0.008	1.702 ±0.203
S		0.047 (MAX)	1.194 (MAX)
y		0.003(MAX)	0.076(MAX)
θ		0°~10°	0°~10°

**28 pin 8x13.4mm STSOP Package Outline Dimension**


SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.00	1.10	1.20	0.040	0.043	0.047
A1	0.05	-	0.15	0.002	-	0.006
A2	0.91	1.00	1.05	0.036	0.039	0.041
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.10	0.15	0.20	0.004	0.006	0.008
HD	13.20	13.40	13.60	0.520	0.528	0.535
D	11.70	11.80	11.90	0.461	0.465	0.469
E	7.90	8.00	8.10	0.311	0.315	0.319
e	-	0.55	-	-	0.0216	-
L	0.30	0.50	0.70	0.012	0.020	0.028
L1	0.675	-	-	0.027	-	-
Y	0.00	-	0.076	0.000	-	0.003
$\theta$	0°	3°	5°	0°	3°	5°



#### ORDERING INFORMATION

LY62L256 U V - WW XX Y Z

Z : Packing Type

Blank : Tube or Tray

T : Tape Reel

Y : Temperature Range

Blank : (Commercial) 0°C ~ 70°C

E : (Extended) -20°C ~ +80°C

I : (Industrial) -40°C ~ +85°C

XX : Power Type

LL : Ultra Low Power

WW : Access Time(Speed)

V : Lead Information

L : Green Package

U : Package Type

P : 28-pin 600 mil P-DIP

S : 28-pin 330 mil SOP

R : 28-pin 8 mm x 13.4 mm STSOP

THIS PAGE IS LEFT BLANK INTENTIONALLY.