



REVISION HISTORY

<u>Revision</u>	<u>Description</u>	<u>Issue Date</u>
Rev. 1.0	Initial Issue	Apr.19.2006
Rev. 2.0	Revised $I_{SB(max)}$: 0.5mA => 1.25mA	May.11.2006
Rev. 2.1	Adding 44-pin TSOP-II	Jul.5.2006
Rev. 2.2	Adding 48-ball BGA	Dec.20.2006
Rev. 2.3	Revised I_{DR} Deleted L Spec. Added SL Spec. Revised Test Condition of $I_{CC}/I_{SB1}/I_{DR}$ Revised V_{TERM} to V_{T1} and V_{T2}	Mar.3.2008
Rev. 2.4	Added I_{SB1}/I_{DR} values when $T_A = 25^{\circ}C$ and $T_A = 40^{\circ}C$ Revised FEATURES & ORDERING INFORMATION Lead free and green package available to Green package available Added packing type in ORDERING INFORMATION Deleted T_{SOLDER} in ABSOLUTE MAXIMUM RATINGS	Mar.30.2009
Rev. 2.5	Revised PACKAGE OUTLINE DIMENSION in page 13	May.6.2010
Rev. 2.6	Revised ORDERING INFORMATION in page 14	Aug.30.2010
Rev. 2.7	Corrected ORDERING INFORMATION Typo.	May.20.2016
Rev. 2.8	Deleted WRITE CYCLE Notes : 1.WE#, CE# must be high or CE2 must be low during all address transitions in page 9	Jun.29.2016



FEATURES

- Fast access time : 45/55/70ns
- Low power consumption:
Operating current : 40/30/20mA (TYP.)
Standby current : 2μA (TYP.) LL-version
1μA (TYP.) SL-version
- Single 2.7V ~ 3.6V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data byte control : LB# (DQ0 ~ DQ7)
UB# (DQ8 ~ DQ15)
- Data retention voltage : 1.5V (MIN.)
- **Green package available**
- Package : 44-pin 400 mil TSOP II
48-pin 12mm x 20mm TSOP I
48-ball 6mm x 8mm TFBGA

GENERAL DESCRIPTION

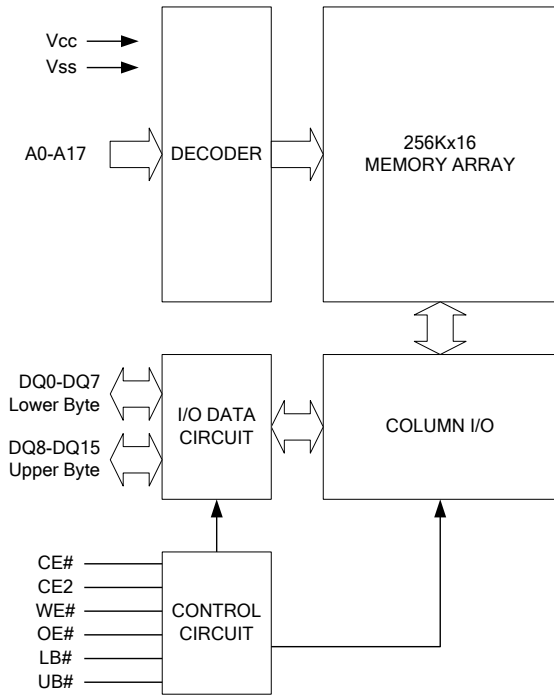
The LY62L25716 is a 4,194,304-bit low power CMOS static random access memory organized as 262,144 words by 16 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

The LY62L25716 is well designed for low power application, and particularly well suited for battery back-up nonvolatile memory application.

The LY62L25716 operates from a single power supply of 2.7V ~ 3.6V and all inputs and outputs are fully TTL compatible

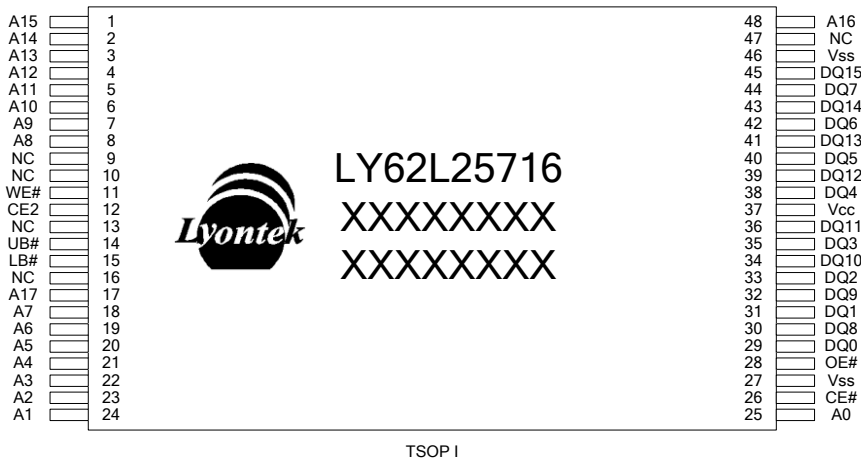
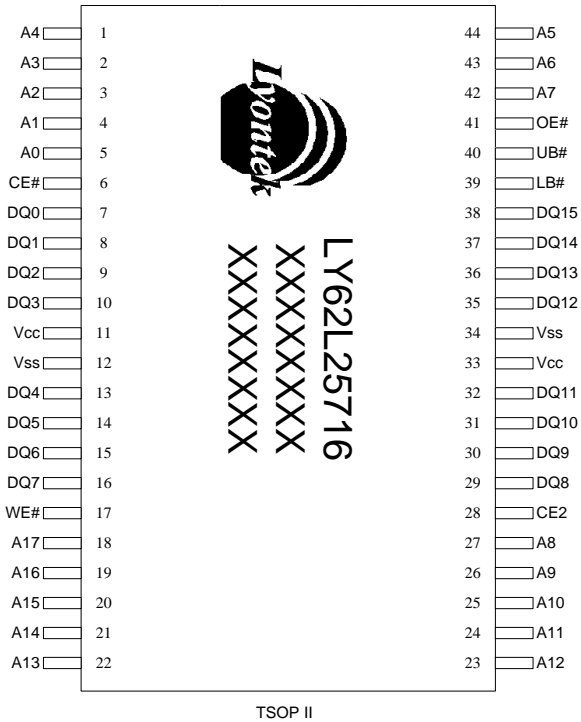
PRODUCT FAMILY

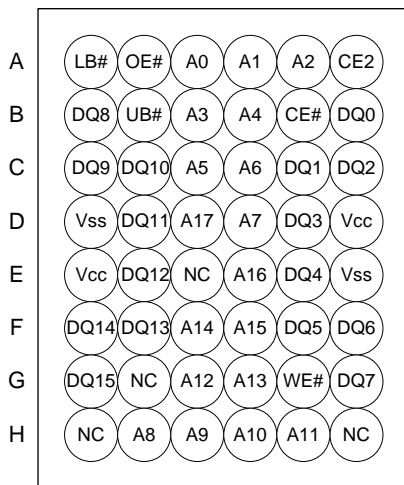
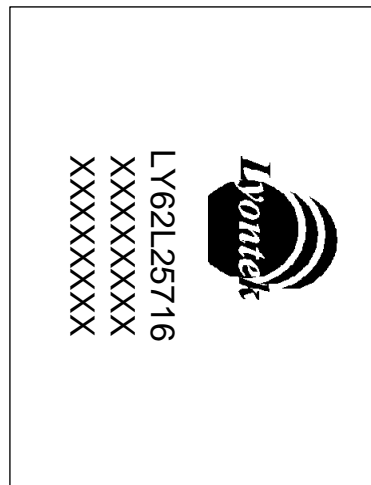
Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation	
				Standby(I _{SB1} ,TYP.)	Operating(I _{CC} ,TYP.)
LY62L25716	0 ~ 70°C	2.7 ~ 3.6V	45/55/70ns	2μA(LL)/1μA(SL)	40/30/20mA
LY62L25716(E)	-20 ~ 80°C	2.7 ~ 3.6V	45/55/70ns	2μA(LL)/1μA(SL)	40/30/20mA
LY62L25716(I)	-40 ~ 85°C	2.7 ~ 3.6V	45/55/70ns	2μA(LL)/1μA(SL)	40/30/20mA

FUNCTIONAL BLOCK DIAGRAM

PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A17	Address Inputs
DQ0 – DQ15	Data Inputs/Outputs
CE#, CE2	Chip Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
LB#	Lower Byte Control
UB#	Upper Byte Control
Vcc	Power Supply
Vss	Ground

PIN CONFIGURATION




 1 2 3 4 5 6
 TFBGA(See through with Top View)


TFBGA(Top View)

ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on Vcc relative to Vss	V _{T1}	-0.5 to 4.6	V
Voltage on any other pin relative to Vss	V _{T2}	-0.5 to Vcc+0.5	V
Operating Temperature	T _A	0 to 70(C grade)	°C
		-20 to 80(E grade)	
		-40 to 85(I grade)	
Storage Temperature	T _{STG}	-65 to 150	°C
Power Dissipation	P _D	1	W
DC Output Current	I _{OUT}	50	mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE#	CE2	OE#	WE#	LB#	UB#	I/O OPERATION		SUPPLY CURRENT
							DQ0-DQ7	DQ8-DQ15	
Standby	H	X	X	X	X	X	High - Z	High - Z	I _{SB} , I _{SB1}
	X	L	X	X	X	X	High - Z	High - Z	
	X	X	X	X	H	H	High - Z	High - Z	
Output Disable	L	H	H	H	L	X	High - Z	High - Z	I _{CC} , I _{CC1}
	L	H	H	H	X	L	High - Z	High - Z	
Read	L	H	L	H	L	H	D _{OUT}	High - Z	I _{CC} , I _{CC1}
	L	H	L	H	H	L	High - Z	D _{OUT}	
	L	H	L	H	L	L	D _{OUT}	D _{OUT}	
Write	L	H	X	L	L	H	D _{IN}	High - Z	I _{CC} , I _{CC1}
	L	H	X	L	H	L	High - Z	D _{IN}	
	L	H	X	L	L	L	D _{IN}	D _{IN}	

Note: H = V_{IH}, L = V_{IL}, X = Don't care.

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP. ⁴	MAX.	UNIT		
Supply Voltage	V _{CC}		2.7	3.0	3.6	V		
Input High Voltage	V _{IH} ¹		2.2	-	V _{CC} +0.3	V		
Input Low Voltage	V _{IL} ²		- 0.2	-	0.6	V		
Input Leakage Current	I _{LI}	V _{CC} ≥ V _{IN} ≥ V _{SS}	- 1	-	1	μA		
Output Leakage Current	I _{LO}	V _{CC} ≥ V _{OUT} ≥ V _{SS} , Output Disabled	- 1	-	1	μA		
Output High Voltage	V _{OH}	I _{OH} = -1mA	2.2	2.7	-	V		
Output Low Voltage	V _{OL}	I _{OL} = 2mA	-	-	0.4	V		
Average Operating Power supply Current	I _{CC}	Cycle time = Min. CE# = V _{IL} and CE2 = V _{IH} , I _{I/O} = 0mA Other pins at V _{IL} or V _{IH}	- 45	-	40	50	mA	
			- 55	-	30	40	mA	
			- 70	-	20	30	mA	
	I _{CC1}	Cycle time = 1μs CE# ≤ 0.2V and CE2 ≥ V _{CC} -0.2V,, I _{I/O} = 0mA Other pins at 0.2V or V _{CC} -0.2V	-	4	5	mA		
Standby Power Supply Current	I _{SB}	CE# = V _{IH} or CE2 = V _{IL} , other pins at V _{IL} or V _{IH}	-	0.3	1.25	mA		
	I _{SB1}	CE# ≥ V _{CC} -0.2V or CE2 ≤ 0.2V Others at 0.2V or V _{CC} - 0.2V	LL	-	2	15	μA	
			LLE/LLI	-	2	20	μA	
			SL ⁺⁵	25°C	-	1	3	μA
			SLE ⁺⁵	40°C	-	1	3	μA
			SLI ⁺⁵		-	1	3	μA
			SL		-	1	10	μA
SLE/SLI		-	1	12	μA			

Notes:

- V_{IH}(max) = V_{CC} + 3.0V for pulse width less than 10ns.
- V_{IL}(min) = V_{SS} - 3.0V for pulse width less than 10ns.
- Over/Undershoot specifications are characterized, not 100% tested.
- Typical values are included for reference only and are not guaranteed or tested.
Typical values are measured at V_{CC} = V_{CC}(TYP.) and T_A = 25°C
- This parameter is measured at V_{CC} = 3.0V

CAPACITANCE (T_A = 25°C, f = 1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C _{IN}	-	6	pF
Input/Output Capacitance	C _{I/O}	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0.2V to V _{CC} - 0.2V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	C _L = 30pF + 1TTL, I _{OH} /I _{OL} = -1mA/2mA

AC ELECTRICAL CHARACTERISTICS
(1) READ CYCLE

PARAMETER	SYM.	LY62L25716-45		LY62L25716-55		LY62L25716-70		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t _{RC}	45	-	55	-	70	-	ns
Address Access Time	t _{AA}	-	45	-	55	-	70	ns
Chip Enable Access Time	t _{ACE}	-	45	-	55	-	70	ns
Output Enable Access Time	t _{OE}	-	25	-	30	-	35	ns
Chip Enable to Output in Low-Z	t _{CLZ} *	10	-	10	-	10	-	ns
Output Enable to Output in Low-Z	t _{OLZ} *	5	-	5	-	5	-	ns
Chip Disable to Output in High-Z	t _{CHZ} *	-	15	-	20	-	25	ns
Output Disable to Output in High-Z	t _{OHZ} *	-	15	-	20	-	25	ns
Output Hold from Address Change	t _{OH}	10	-	10	-	10	-	ns
LB#, UB# Access Time	t _{BA}	-	45	-	55	-	70	ns
LB#, UB# to High-Z Output	t _{BHZ} *	-	20	-	25	-	30	ns
LB#, UB# to Low-Z Output	t _{BLZ} *	10	-	10	-	10	-	ns

(2) WRITE CYCLE

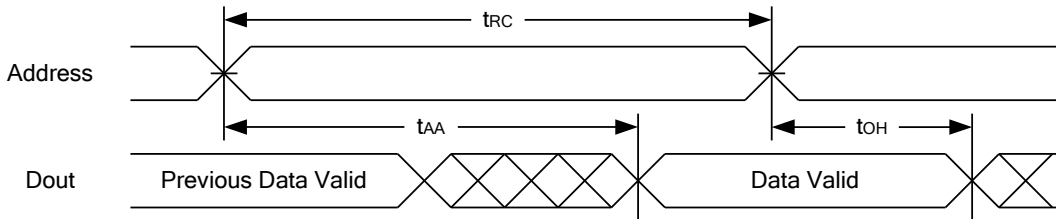
PARAMETER	SYM.	LY62L25716-45		LY62L25716-55		LY62L25716-70		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t _{WC}	45	-	55	-	70	-	ns
Address Valid to End of Write	t _{AW}	40	-	50	-	60	-	ns
Chip Enable to End of Write	t _{CW}	40	-	50	-	60	-	ns
Address Set-up Time	t _{AS}	0	-	0	-	0	-	ns
Write Pulse Width	t _{WP}	35	-	45	-	55	-	ns
Write Recovery Time	t _{WR}	0	-	0	-	0	-	ns
Data to Write Time Overlap	t _{DW}	20	-	25	-	30	-	ns
Data Hold from End of Write Time	t _{DH}	0	-	0	-	0	-	ns
Output Active from End of Write	t _{OW} *	5	-	5	-	5	-	ns
Write to Output in High-Z	t _{WHZ} *	-	15	-	20	-	25	ns
LB#, UB# Valid to End of Write	t _{BW}	35	-	45	-	60	-	ns

*These parameters are guaranteed by device characterization, but not production tested.

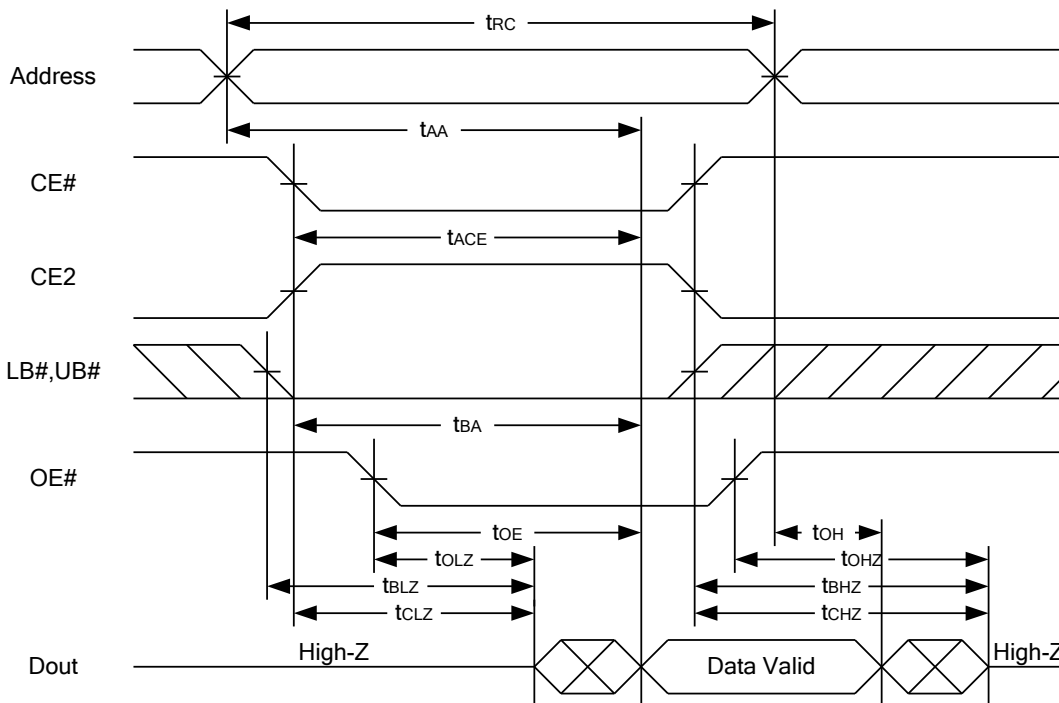


TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)



READ CYCLE 2 (CE# and CE2 and OE# Controlled) (1,3,4,5)

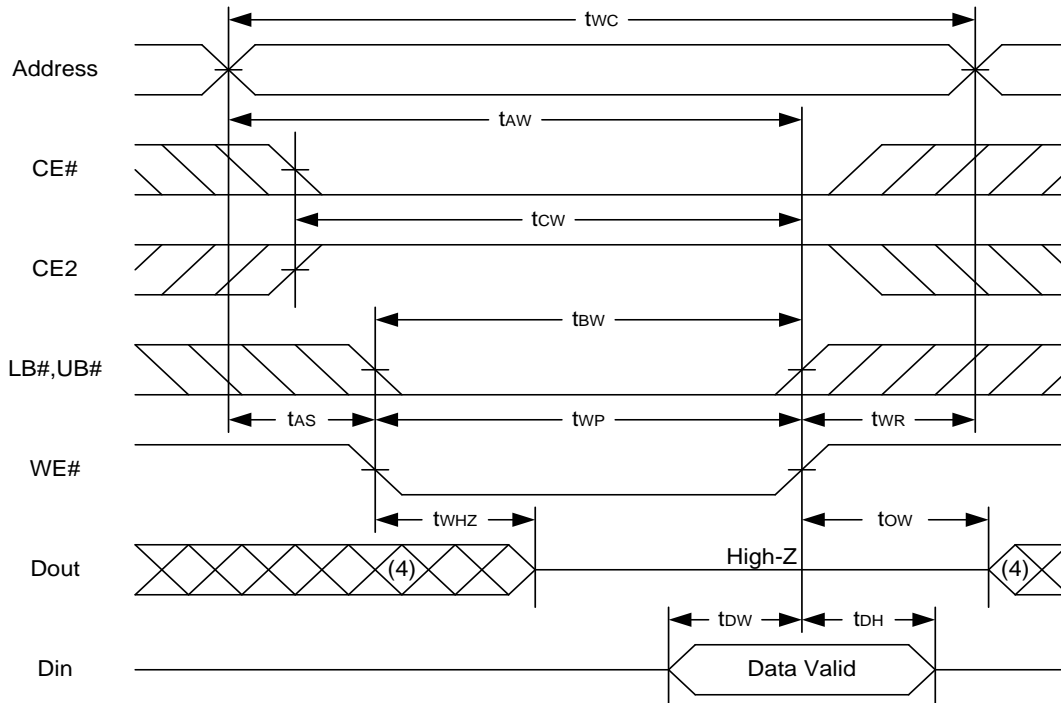


Notes :

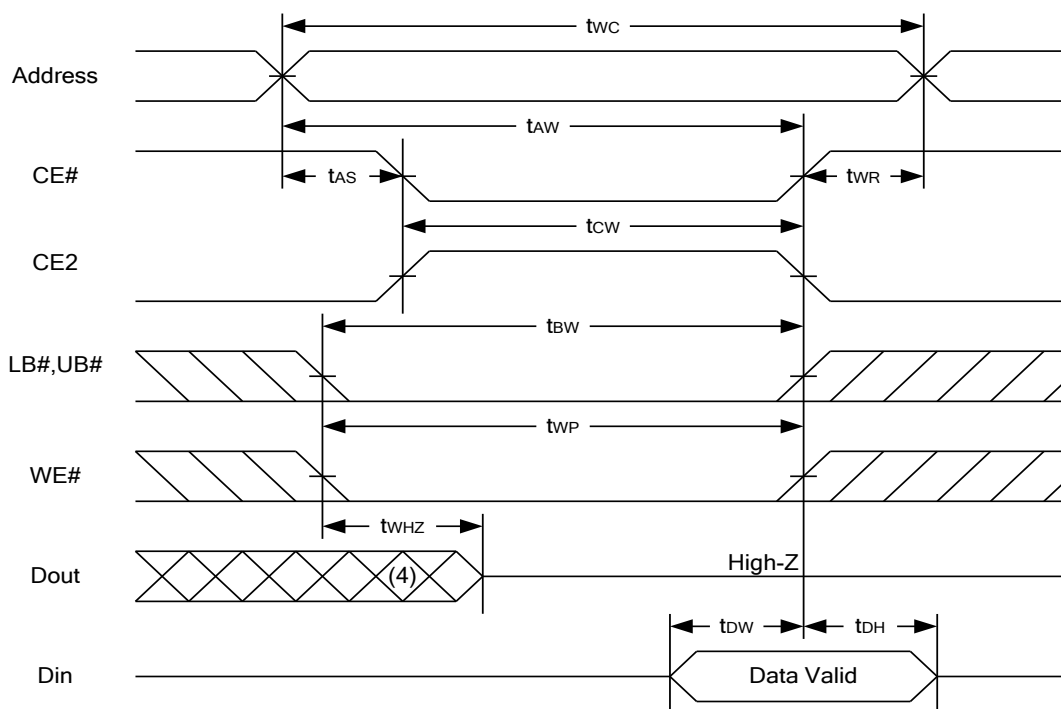
1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low, CE2 = high, LB# or UB# = low.
3. Address must be valid prior to or coincident with CE# = low, CE2 = high, LB# or UB# = low transition; otherwise t_{AA} is the limiting parameter.
4. t_{CLZ} , t_{BLZ} , t_{OLZ} , t_{CHZ} , t_{BHZ} and t_{OHZ} are specified with $C_L = 5pF$. Transition is measured $\pm 500mV$ from steady state.
5. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{BHZ} is less than t_{BLZ} , t_{OHZ} is less than t_{OLZ} .



WRITE CYCLE 1 (WE# Controlled) (1,2,4,5)

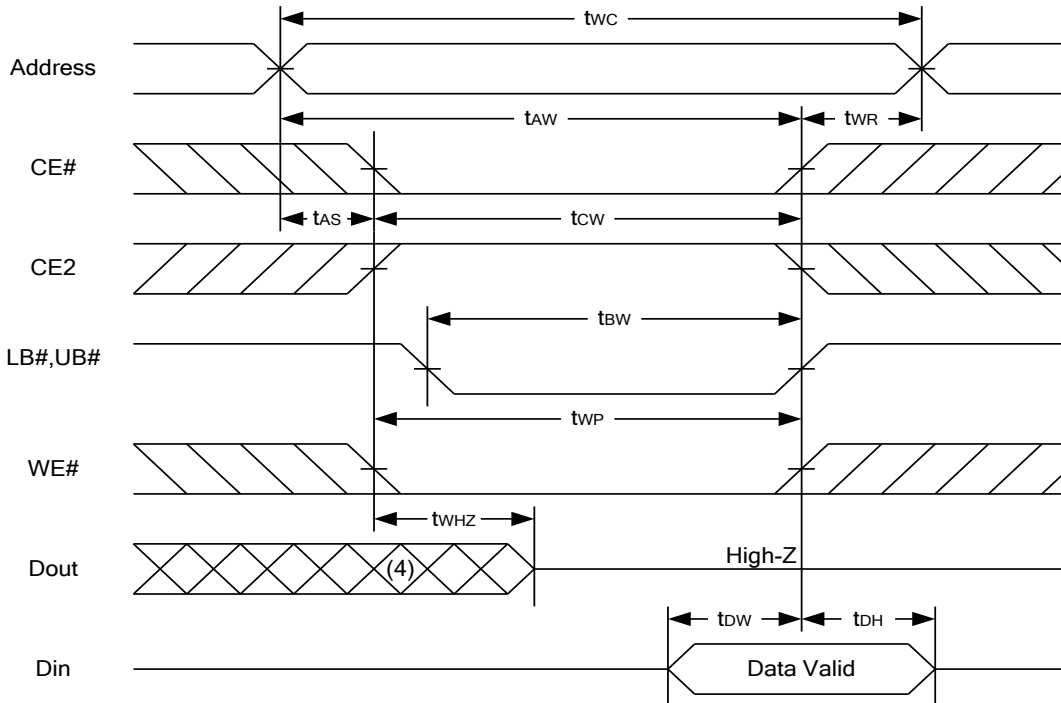


WRITE CYCLE 2 (CE# and CE2 Controlled) (1,4,5)





WRITE CYCLE 3 (LB#,UB# Controlled) (1,4,5)



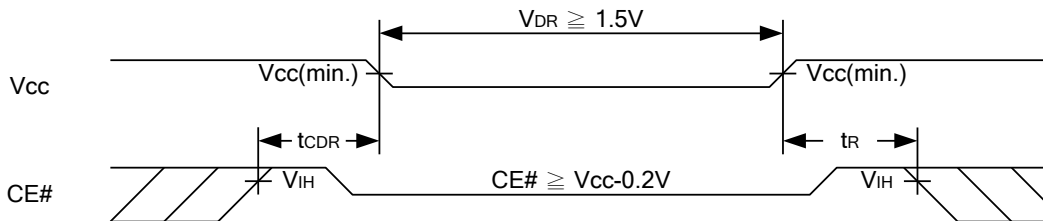
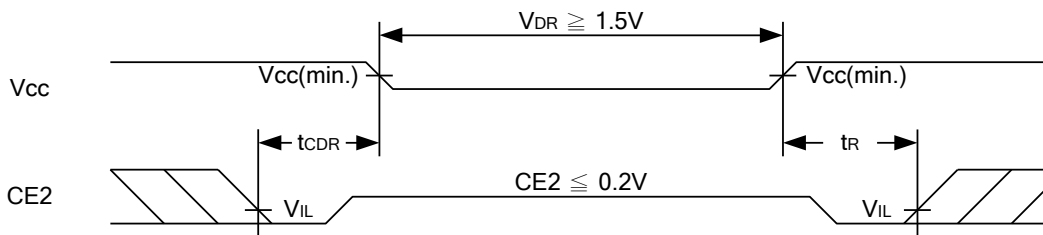
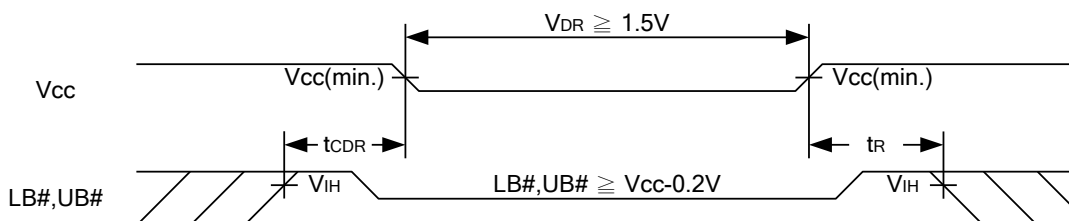
Notes :

1. A write occurs during the overlap of a low CE#, high CE2, low WE#, LB# or UB# = low.
2. During a WE# controlled write cycle with OE# low, t_{WP} must be greater than $t_{WHZ} + t_{DQ}$ to allow the drivers to turn off and data to be placed on the bus.
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the CE#, LB#, UB# low transition and CE2 high transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
5. t_{ow} and t_{whz} are specified with $C_L = 5pF$. Transition is measured $\pm 500mV$ from steady state.

DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT		
V _{CC} for Data Retention	V _{DR}	CE# ≥ V _{CC} - 0.2V or CE2 ≤ 0.2V	1.5	-	3.6	V		
Data Retention Current	I _{DR}	V _{CC} = 1.5V CE# ≥ V _{CC} - 0.2V or CE2 ≤ 0.2V Other pins at 0.2V or V _{CC} -0.2V	LL	-	1.0	12	μA	
			LLE/LLI	-	1.0	16	μA	
			SL	25°C	-	0.5	2.5	μA
			SLE	40°C	-	0.5	2.5	μA
			SLI		-	0.5	2.5	μA
			SL	-	0.5	8	μA	
SLE/SLI	-	0.5	10	μA				
Chip Disable to Data Retention Time	t _{CDR}	See Data Retention Waveforms (below)	0	-	-	ns		
Recovery Time	t _R		t _{RC} *	-	-	ns		

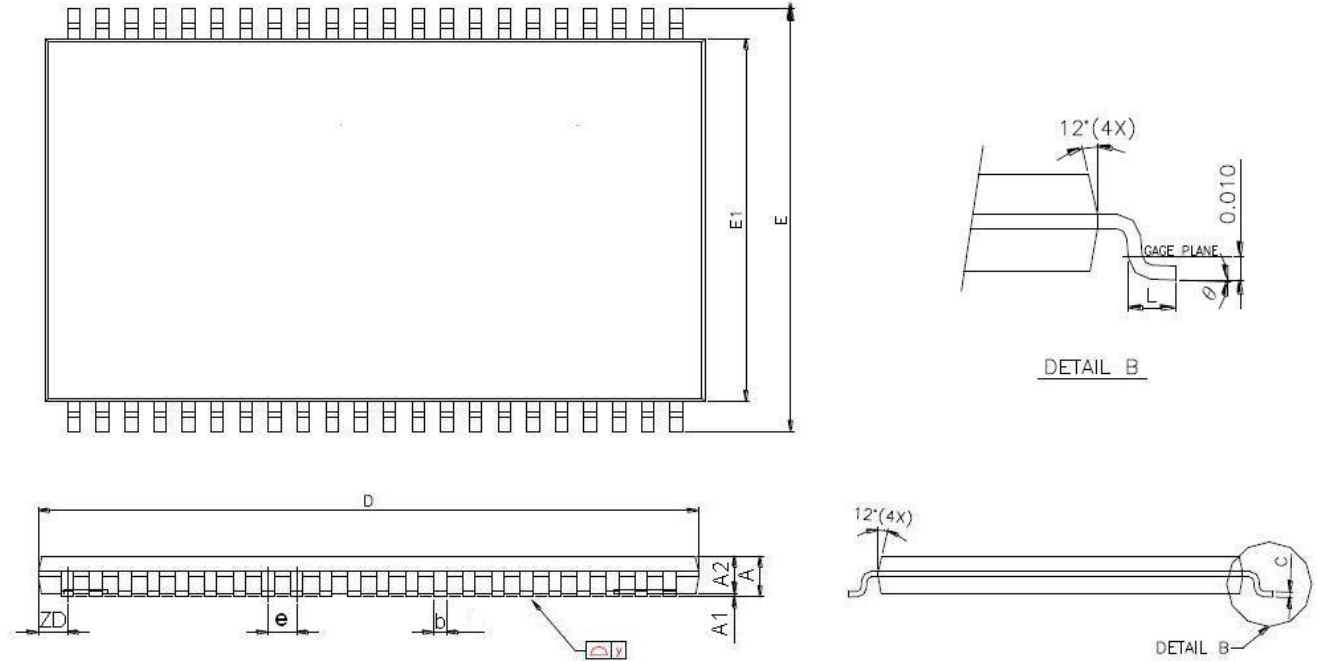
 t_{RC}* = Read Cycle Time

DATA RETENTION WAVEFORM
Low V_{CC} Data Retention Waveform (1) (CE# controlled)

Low V_{CC} Data Retention Waveform (2) (CE2 controlled)

Low V_{CC} Data Retention Waveform (3) (LB#, UB# controlled)




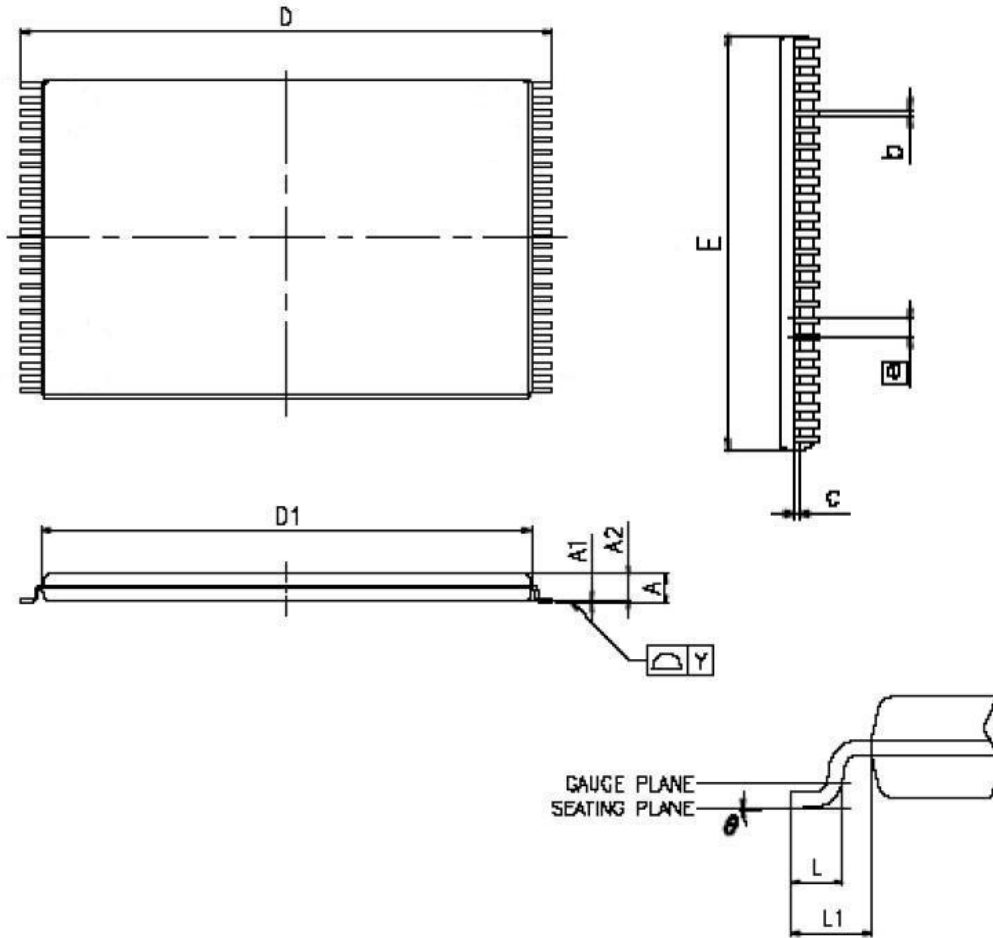
PACKAGE OUTLINE DIMENSION

44-pin 400mil TSOP II Package Outline Dimension



SYMBOLS	DIMENSIONS IN MILLMETERS			DIMENSIONS IN MILS		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	-	-	1.20	-	-	47.2
A1	0.05	0.10	0.15	2.0	3.9	5.9
A2	0.95	1.00	1.05	37.4	39.4	41.3
b	0.30	-	0.45	11.8	-	17.7
c	0.12	-	0.21	4.7	-	8.3
D	18.212	18.415	18.618	717	725	733
E	11.506	11.760	12.014	453	463	473
E1	9.957	10.160	10.363	392	400	408
e	-	0.800	-	-	31.5	-
L	0.40	0.50	0.60	15.7	19.7	23.6
ZD	-	0.805	-	-	31.7	-
y	-	-	0.076	-	-	3
Θ	0°	3°	6°	0°	3°	6°

48-pin 12mm x 20mm TSOP I Package Outline Dimension



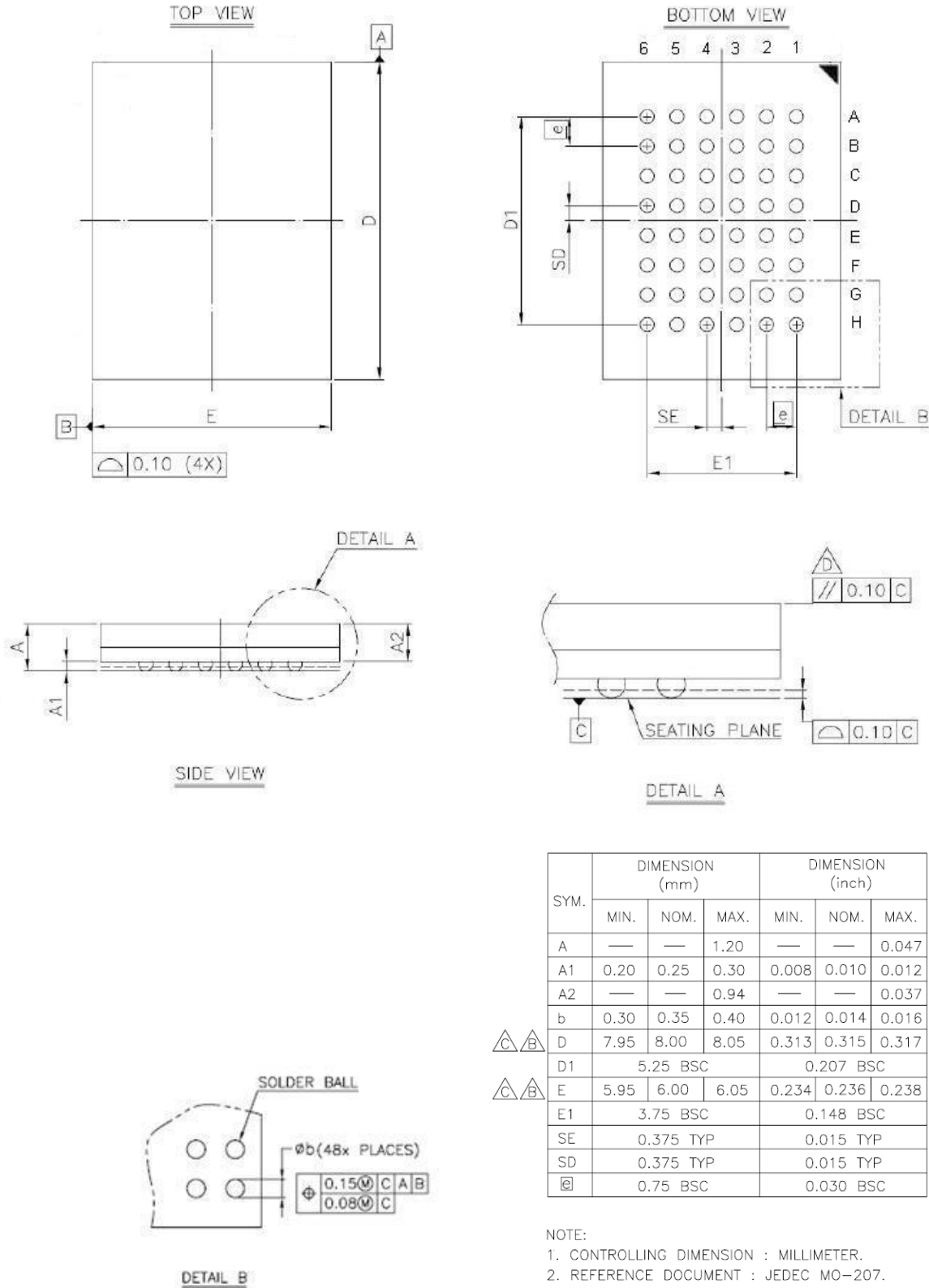
VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX
A	-	-	1.20
A1	0.05	-	0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
c	0.10	-	0.21
D	19.80	20.00	20.20
D1	18.30	18.40	18.50
E	11.90	12.00	12.10
⓪	0.50 BASIC		
L	0.50	0.60	0.70
L1	-	0.80	-
Y	-	-	0.10
⊘	⊘	-	5°

NOTES:

- 1 JEDEC OUTLINE : MO-142 DD
2. PROFILE TOLERANCE ZONES FOR D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION ON E IS 0.15mm PER SIDE AND ON D1 IS 0.25mm PER SIDE.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

48-ball 6mm x 8mm TFBGA Package Outline Dimension





ORDERING INFORMATION

Package Type	Access Time (Speed)(ns)	Power Type	Temperature Range(°C)	Packing Type	Lyontek Item No.
44Pin(400mil) TSOP II	45	Special Ultra Low Power	0°C~70°C	Tray	LY62L25716ML-45SL
				Tape Reel	LY62L25716ML-45SLT
			-20°C~80°C	Tray	LY62L25716ML-45SLE
				Tape Reel	LY62L25716ML-45SLET
			-40°C~85°C	Tray	LY62L25716ML-45SLI
				Tape Reel	LY62L25716ML-45SLIT
		Ultra Low Power	0°C~70°C	Tray	LY62L25716ML-45LL
				Tape Reel	LY62L25716ML-45LLT
			-20°C~80°C	Tray	LY62L25716ML-45LLE
				Tape Reel	LY62L25716ML-45LLET
			-40°C~85°C	Tray	LY62L25716ML-45LLI
				Tape Reel	LY62L25716ML-45LLIT
	55	Special Ultra Low Power	0°C~70°C	Tray	LY62L25716ML-55SL
				Tape Reel	LY62L25716ML-55SLT
			-20°C~80°C	Tray	LY62L25716ML-55SLE
				Tape Reel	LY62L25716ML-55SLET
			-40°C~85°C	Tray	LY62L25716ML-55SLI
				Tape Reel	LY62L25716ML-55SLIT
		Ultra Low Power	0°C~70°C	Tray	LY62L25716ML-55LL
				Tape Reel	LY62L25716ML-55LLT
			-20°C~80°C	Tray	LY62L25716ML-55LLE
				Tape Reel	LY62L25716ML-55LLET
			-40°C~85°C	Tray	LY62L25716ML-55LLI
				Tape Reel	LY62L25716ML-55LLIT
70	Special Ultra Low Power	0°C~70°C	Tray	LY62L25716ML-70SL	
			Tape Reel	LY62L25716ML-70SLT	
		-20°C~80°C	Tray	LY62L25716ML-70SLE	
			Tape Reel	LY62L25716ML-70SLET	
		-40°C~85°C	Tray	LY62L25716ML-70SLI	
			Tape Reel	LY62L25716ML-70SLIT	
	Ultra Low Power	0°C~70°C	Tray	LY62L25716ML-70LL	
			Tape Reel	LY62L25716ML-70LLT	
		-20°C~80°C	Tray	LY62L25716ML-70LLE	
			Tape Reel	LY62L25716ML-70LLET	
		-40°C~85°C	Tray	LY62L25716ML-70LLI	
			Tape Reel	LY62L25716ML-70LLIT	



ORDERING INFORMATION

Package Type	Access Time (Speed)(ns)	Power Type	Temperature Range(°C)	Packing Type	Lyontek Item No.
48-Pin 12mmx20mm TSOP I	45	Special Ultra Low Power	0°C~70°C	Tray	LY62L25716LL-45SL
				Tape Reel	LY62L25716LL-45SLT
			-20°C~80°C	Tray	LY62L25716LL-45SLE
				Tape Reel	LY62L25716LL-45SLET
			-40°C~85°C	Tray	LY62L25716LL-45SLI
				Tape Reel	LY62L25716LL-45SLIT
		Ultra Low Power	0°C~70°C	Tray	LY62L25716LL-45LL
				Tape Reel	LY62L25716LL-45LLT
			-20°C~80°C	Tray	LY62L25716LL-45LLE
				Tape Reel	LY62L25716LL-45LLET
			-40°C~85°C	Tray	LY62L25716LL-45LLI
				Tape Reel	LY62L25716LL-45LLIT
	55	Special Ultra Low Power	0°C~70°C	Tray	LY62L25716LL-55SL
				Tape Reel	LY62L25716LL-55SLT
			-20°C~80°C	Tray	LY62L25716LL-55SLE
				Tape Reel	LY62L25716LL-55SLET
			-40°C~85°C	Tray	LY62L25716LL-55SLI
				Tape Reel	LY62L25716LL-55SLIT
		Ultra Low Power	0°C~70°C	Tray	LY62L25716LL-55LL
				Tape Reel	LY62L25716LL-55LLT
			-20°C~80°C	Tray	LY62L25716LL-55LLE
				Tape Reel	LY62L25716LL-55LLET
			-40°C~85°C	Tray	LY62L25716LL-55LLI
				Tape Reel	LY62L25716LL-55LLIT
70	Special Ultra Low Power	0°C~70°C	Tray	LY62L25716LL-70SL	
			Tape Reel	LY62L25716LL-70SLT	
		-20°C~80°C	Tray	LY62L25716LL-70SLE	
			Tape Reel	LY62L25716LL-70SLET	
		-40°C~85°C	Tray	LY62L25716LL-70SLI	
			Tape Reel	LY62L25716LL-70SLIT	
	Ultra Low Power	0°C~70°C	Tray	LY62L25716LL-70LL	
			Tape Reel	LY62L25716LL-70LLT	
		-20°C~80°C	Tray	LY62L25716LL-70LLE	
			Tape Reel	LY62L25716LL-70LLET	
		-40°C~85°C	Tray	LY62L25716LL-70LLI	
			Tape Reel	LY62L25716LL-70LLIT	



ORDERING INFORMATION

Package Type	Access Time (Speed)(ns)	Power Type	Temperature Range(°C)	Packing Type	Lyontek Item No.
48-ball (6mmx8mm) TFBGA	45	Special Ultra Low Power	0°C~70°C	Tray	LY62L25716GL-45SL
				Tape Reel	LY62L25716GL-45SLT
			-20°C~80°C	Tray	LY62L25716GL-45SLE
				Tape Reel	LY62L25716GL-45SLET
			-40°C~85°C	Tray	LY62L25716GL-45SLI
				Tape Reel	LY62L25716GL-45SLIT
		Ultra Low Power	0°C~70°C	Tray	LY62L25716GL-45LL
				Tape Reel	LY62L25716GL-45LLT
			-20°C~80°C	Tray	LY62L25716GL-45LLE
				Tape Reel	LY62L25716GL-45LLET
			-40°C~85°C	Tray	LY62L25716GL-45LLI
				Tape Reel	LY62L25716GL-45LLIT
	55	Special Ultra Low Power	0°C~70°C	Tray	LY62L25716GL-55SL
				Tape Reel	LY62L25716GL-55SLT
			-20°C~80°C	Tray	LY62L25716GL-55SLE
				Tape Reel	LY62L25716GL-55SLET
			-40°C~85°C	Tray	LY62L25716GL-55SLI
				Tape Reel	LY62L25716GL-55SLIT
		Ultra Low Power	0°C~70°C	Tray	LY62L25716GL-55LL
				Tape Reel	LY62L25716GL-55LLT
			-20°C~80°C	Tray	LY62L25716GL-55LLE
				Tape Reel	LY62L25716GL-55LLET
			-40°C~85°C	Tray	LY62L25716GL-55LLI
				Tape Reel	LY62L25716GL-55LLIT
70	Special Ultra Low Power	0°C~70°C	Tray	LY62L25716GL-70SL	
			Tape Reel	LY62L25716GL-70SLT	
		-20°C~80°C	Tray	LY62L25716GL-70SLE	
			Tape Reel	LY62L25716GL-70SLET	
		-40°C~85°C	Tray	LY62L25716GL-70SLI	
			Tape Reel	LY62L25716GL-70SLIT	
	Ultra Low Power	0°C~70°C	Tray	LY62L25716GL-70LL	
			Tape Reel	LY62L25716GL-70LLT	
		-20°C~80°C	Tray	LY62L25716GL-70LLE	
			Tape Reel	LY62L25716GL-70LLET	
		-40°C~85°C	Tray	LY62L25716GL-70LLI	
			Tape Reel	LY62L25716GL-70LLIT	



Lyontek Inc.

LY62L25716

Rev. 2.8

256K X 16 BIT LOW POWER CMOS SRAM

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