



REVISION HISTORY

<u>Revision</u>	<u>Description</u>	<u>Issue Date</u>
Rev. 1.0	Initial Issue	Apr.06.2016
Rev. 1.1	Deleted WRITE CYCLE Notes : 1. WE#,CE#, LB#, UB# must be high or CE2 must be low during all address transitions. in page 8	Jun.28.2016
Rev. 1.2	Revised I_{CC} / I_{CC1} / $I_{SB1}(MAX.)$ / $I_{DR}(MAX.)$ in <u>DC ELECTRICAL CHARACTERISTICS & DATA RETENTION CHARACTERISTICS & PRODUCT FAMILY & FEATURES</u>	Apr.07.2017
Rev. 1.3	Added <u>TRUTH TABLE</u> Notes: 2. The BYTE# pin has to be tied to V_{CC} to use the device as a 4M x 16 SRAM, and to be tied to V_{SS} as a 8M x 8 SRAM. In the 8M x 8 configuration, Pin 45 is A-1, and both UB# and LB# are tied to V_{SS} , while DQ8 to DQ14 pins are not used.	May.22.2017
Rev. 1.4	Revised typo in <u>TIMING WAVEFORMS</u> of WRITE CYCLE in page 7 & 8	Jul.30.2020

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FEATURES

- Fast access time : 55ns
- Low power consumption:
Operating current : 12mA (TYP.)
Standby current : 12μA(TYP.)
- Single 2.7V ~ 3.6V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data byte control :
 - (i) BYTE# fixed to V_{CC}
LB# controlled DQ0 ~ DQ7
UB# controlled DQ8 ~ DQ15
 - (ii) BYTE# fixed to V_{SS}
DQ15 used as address pin, while
DQ8~DQ14 pins not used
- Data retention voltage : 1.2V (MIN.)
- **Green package available**
- Package : 48-pin 12mm x 20mm TSOP I

PRODUCT FAMILY

Product Family	Operating Temperature	V_{CC} Range	Speed	Power Dissipation	
				Standby(I_{SB1} , TYP.)	Operating(I_{CC} , TYP.)
LY62L409816A	0 ~ 70°C	2.7 ~ 3.6V	55ns	12μA	12mA
LY62L409816A(I)	-40 ~ 85°C	2.7 ~ 3.6V	55ns	12μA	12mA

GENERAL DESCRIPTION

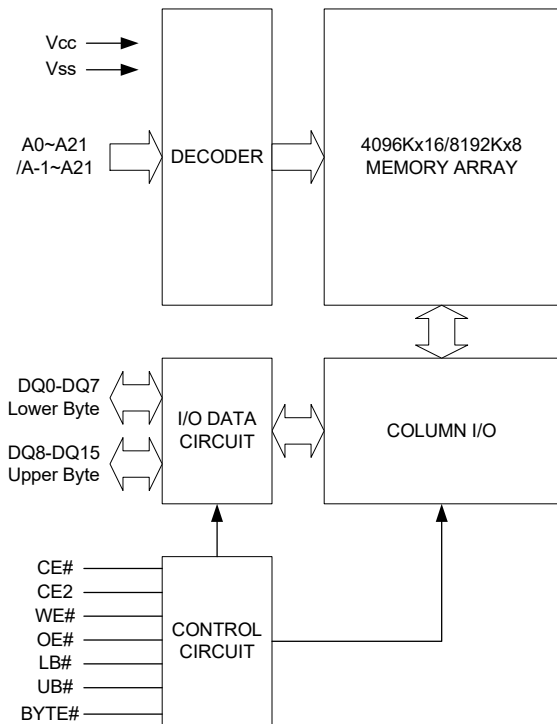
The LY62L409816A is a 67,108,864-bit low power CMOS static random access memory organized as 4,194,304 words by 16 bits or 8,388,608 words by 8 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

The LY62L409816A is well designed for low power application, and particularly well suited for battery back-up nonvolatile memory application.

The LY62L409816A operates from a single power supply of 2.7V ~ 3.6V and all inputs and outputs are fully TTL compatible



FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A21	Address Inputs(word mode)
A-1 - A21	Address Inputs(byte mode)
DQ0 - DQ15	Data Inputs/Outputs
CE#, CE2	Chip Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
LB#	Lower Byte Control
UB#	Upper Byte Control
BYTE#	Byte Enable
Vcc	Power Supply
Vss	Ground

PIN CONFIGURATION



TSOP I



ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on V _{CC} relative to V _{SS}	V _{T1}	-0.5 to 4.6	V
Voltage on any other pin relative to V _{SS}	V _{T2}	-0.5 to V _{CC} +0.5	V
Operating Temperature	T _A	0 to 70(C grade)	°C
		-40 to 85(I grade)	
Storage Temperature	T _{STG}	-65 to 150	°C
Power Dissipation	P _D	1	W
DC Output Current	I _{OUT}	50	mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE#	CE2	BYTE #	OE#	WE#	LB#	UB#	I/O OPERATION			SUPPLY CURRENT
								DQ0-DQ7	DQ8-DQ14	DQ15	
Standby	H	X	X	X	X	X	X	High-Z	High-Z	High-Z	I _{SB1}
	X	L	X	X	X	X	X	High-Z	High-Z	High-Z	
	X	X	H	X	X	H	H	High-Z	High-Z	High-Z	
Output Disable	L	H	H	H	H	L	X	High-Z	High-Z	High-Z	I _{CC} , I _{CC1}
	L	H	H	H	H	X	L	High-Z	High-Z	High-Z	
	L	H	L	H	H	L	L	High-Z	High-Z	A-1	
Read	L	H	H	L	H	L	H	D _{OUT}	High-Z	High-Z	I _{CC} , I _{CC1}
	L	H	H	L	H	H	L	High-Z	D _{OUT}	D _{OUT}	
	L	H	H	L	H	L	L	D _{OUT}	D _{OUT}	D _{OUT}	
Write	L	H	H	X	L	L	H	D _{IN}	High-Z	High-Z	I _{CC} , I _{CC1}
	L	H	H	X	L	H	L	High-Z	D _{IN}	D _{IN}	
	L	H	H	X	L	L	L	D _{IN}	D _{IN}	D _{IN}	
Byte# Read	L	H	L	L	H	L	L	D _{OUT}	High-Z	A-1	I _{CC} , I _{CC1}
Byte # Write	L	H	L	X	L	L	L	D _{IN}	High-Z	A-1	I _{CC} , I _{CC1}

Notes:

- H = V_{IH}, L = V_{IL}, X = Don't care.
- The BYTE# pin has to be tied to V_{CC} to use the device as a 4M x 16 SRAM, and to be tied to V_{SS} as a 8M x 8 SRAM. In the 8M x 8 configuration, Pin 45 is A-1, and both UB# and LB# are tied to V_{SS}, while DQ8 to DQ14 pins are not used.



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP. ^{*4}	MAX.	UNIT	
Supply Voltage	V _{CC}		2.7	3.0	3.6	V	
Input High Voltage	V _{IH} ^{*1}		2.2	-	V _{CC} +0.3	V	
Input Low Voltage	V _{IL} ^{*2}		- 0.2	-	0.6	V	
Input Leakage Current	I _{LI}	V _{CC} ≥ V _{IN} ≥ V _{SS}	- 1	-	1	μA	
Output Leakage Current	I _{LO}	V _{CC} ≥ V _{OUT} ≥ V _{SS} Output Disabled	- 1	-	1	μA	
Output High Voltage	V _{OH}	I _{OH} = -1mA	2.2	2.7	-	V	
Output Low Voltage	V _{OL}	I _{OL} = 2mA	-	-	0.4	V	
Average Operating Power supply Current	I _{CC}	Cycle time = MIN. CE# ≤ 0.2V and CE2 ≥ V _{CC} -0.2V I _{I/O} = 0mA Other pins at 0.2V or V _{CC} -0.2V	-	12	20	mA	
	I _{CC1}	Cycle time = 1μs CE# ≤ 0.2V and CE2 ≥ V _{CC} -0.2V I _{I/O} = 0mA Other pins at 0.2V or V _{CC} -0.2V	-	3	5	mA	
Standby Power Supply Current	I _{SB1}	CE# ≥ V _{CC} -0.2V or CE2 ≤ 0.2V Other pins at 0.2V or V _{CC} -0.2V	-SL ^{*5} 25°C	-	12	32	μA
			-SLI ^{*5} 40°C	-	12	36	μA
			-SL (70°C)	-	-	100	μA
			-SLI (85°C)	-	-	160	μA

Notes:

- V_{IH}(max) = V_{CC} + 2.0V for pulse width less than 6ns.
- V_{IL}(min) = V_{SS} - 2.0V for pulse width less than 6ns.
- Over/Undershoot specifications are characterized on engineering evaluation stage, not for mass production test.
- Typical values, measured at V_{CC} = V_{CC}(TYP.) and T_A = 25°C, are included for reference only and are not guaranteed or tested.
- This parameter is measured at V_{CC}=3.0V.

CAPACITANCE (T_A = 25°C, f = 1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Input Capacitance	C _{IN}	-	15	pF
Input/Output Capacitance	C _{I/O}	-	20	pF

Note : These parameters are guaranteed by device characterization, but not production tested.



AC TEST CONDITIONS

Input Pulse Levels	0.2V to $V_{CC} - 0.2V$
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	$C_L = 30pF + 1TTL, I_{OH}/I_{OL} = -1mA/2mA$

AC ELECTRICAL CHARACTERISTICS

(1) READ CYCLE

PARAMETER	SYM.	LY62L409816A-55		UNIT
		MIN.	MAX.	
Read Cycle Time	t_{RC}	55	-	ns
Address Access Time	t_{AA}	-	55	ns
Chip Enable Access Time	t_{ACE}	-	55	ns
Output Enable Access Time	t_{OE}	-	30	ns
Chip Enable to Output in Low-Z	t_{CLZ}^*	10	-	ns
Output Enable to Output in Low-Z	t_{OLZ}^*	5	-	ns
Chip Disable to Output in High-Z	t_{CHZ}^*	-	20	ns
Output Disable to Output in High-Z	t_{OHZ}^*	-	20	ns
Output Hold from Address Change	t_{OH}	10	-	ns
LB#, UB# Access Time	t_{BA}	-	55	ns
LB#, UB# to High-Z Output	t_{BHZ}^*	-	20	ns
LB#, UB# to Low-Z Output	t_{BLZ}^*	10	-	ns

(2) WRITE CYCLE

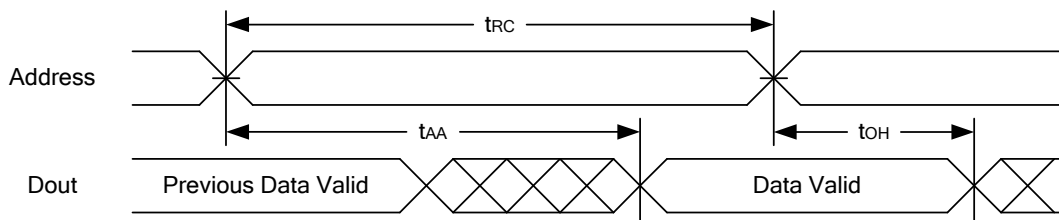
PARAMETER	SYM.	LY62L409816A-55		UNIT
		MIN.	MAX.	
Write Cycle Time	t_{WC}	55	-	ns
Address Valid to End of Write	t_{AW}	50	-	ns
Chip Enable to End of Write	t_{CW}	50	-	ns
Address Set-up Time	t_{AS}	0	-	ns
Write Pulse Width	t_{WP}	45	-	ns
Write Recovery Time	t_{WR}	0	-	ns
Data to Write Time Overlap	t_{DW}	25	-	ns
Data Hold from End of Write Time	t_{DH}	0	-	ns
Output Active from End of Write	t_{OW}^*	5	-	ns
Write to Output in High-Z	t_{WHZ}^*	-	20	ns
LB#, UB# Valid to End of Write	t_{BW}	50	-	ns

*These parameters are guaranteed by device characterization, but not production tested.

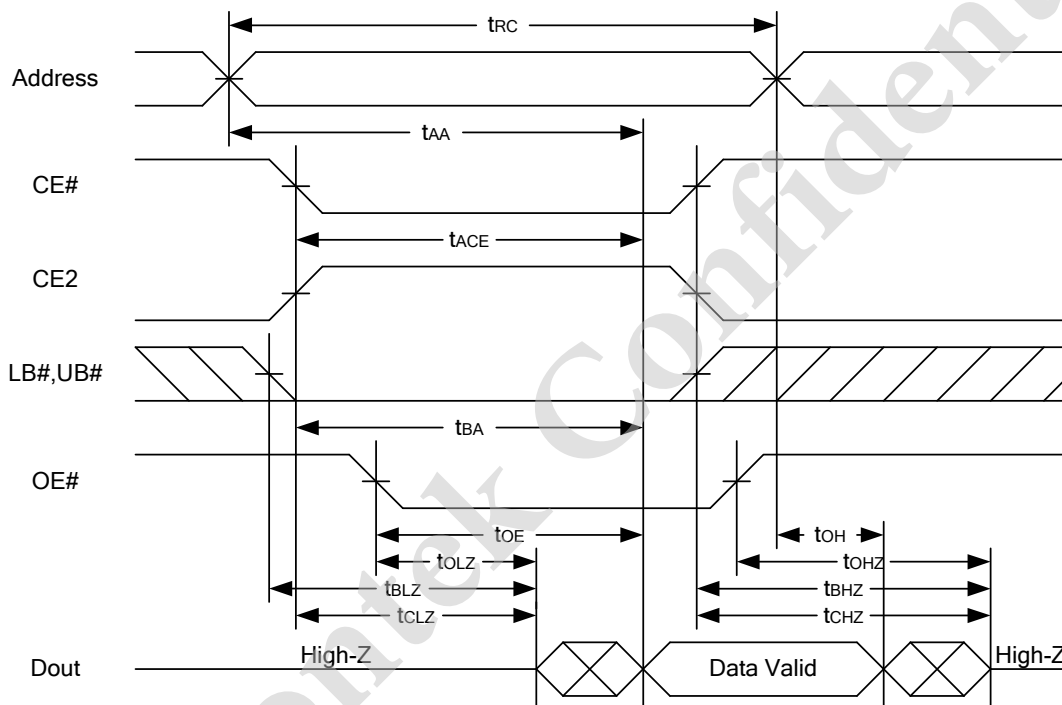


TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)



READ CYCLE 2 (CE# and CE2 and OE# Controlled) (1,3,4,5)

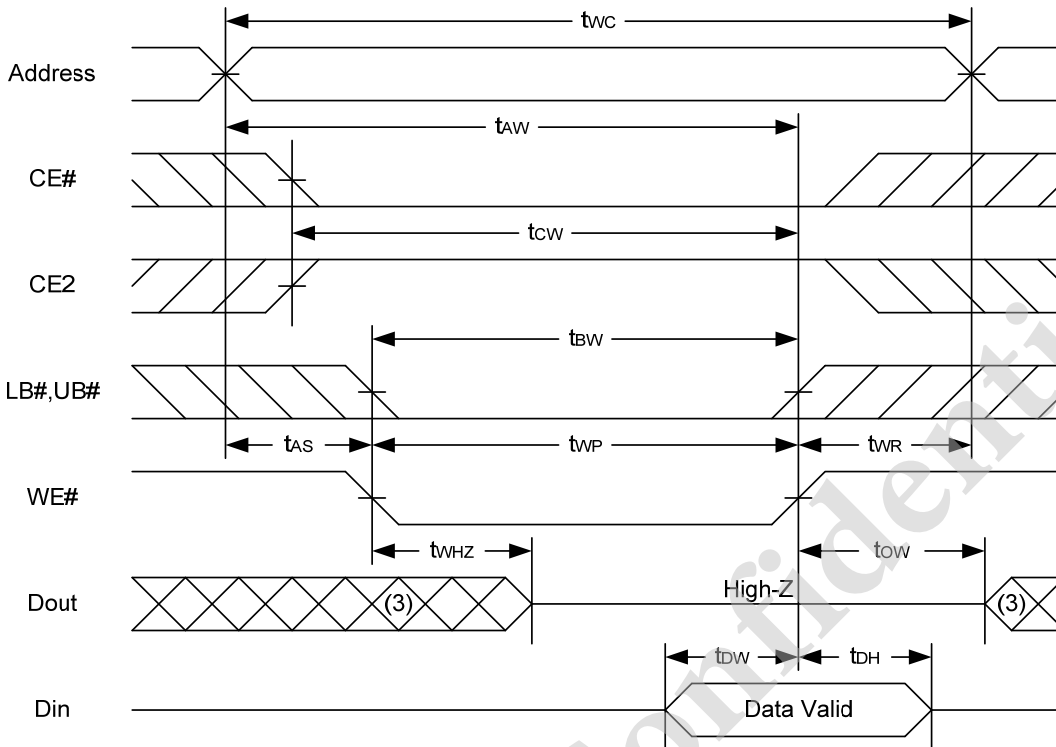


Notes :

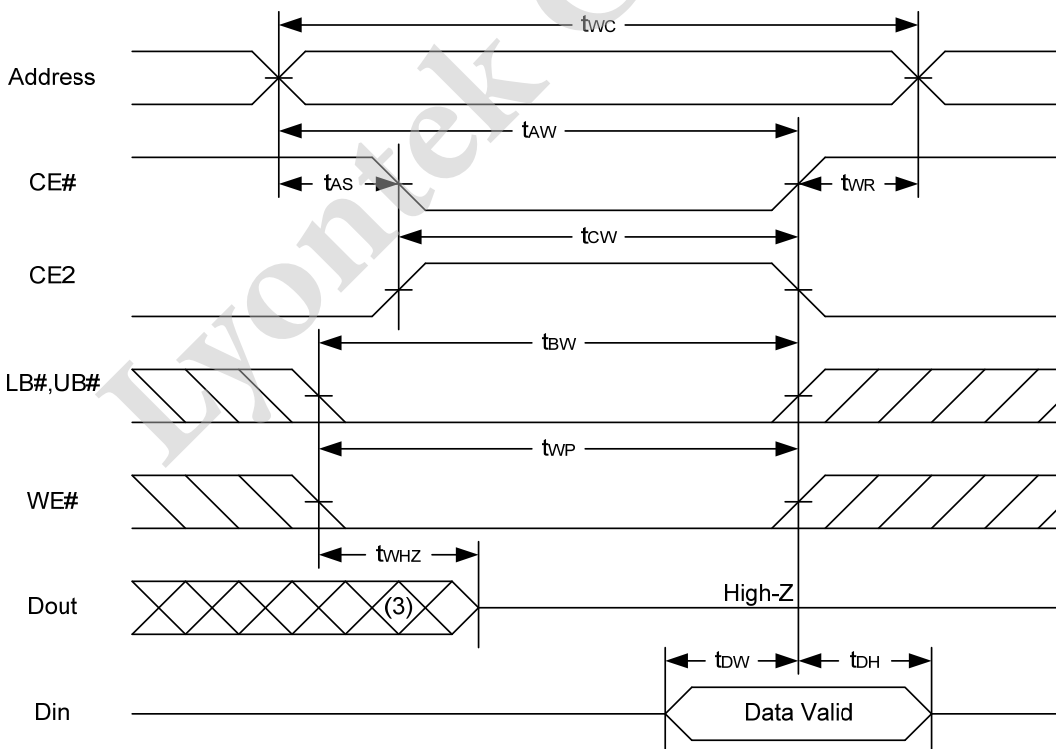
1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low, CE2 = high, LB# or UB# = low.
3. Address must be valid prior to or coincident with CE# = low, CE2 = high, LB# or UB# = low transition; otherwise t_{AA} is the limiting parameter.
4. t_{CLZ} , t_{BLZ} , t_{OLZ} , t_{CHZ} , t_{BHZ} and t_{OHZ} are specified with $C_L = 5pF$. Transition is measured $\pm 500mV$ from steady state.
5. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{BHZ} is less than t_{BLZ} , t_{OHZ} is less than t_{OLZ} .



WRITE CYCLE 1 (WE# Controlled) (1,2,4,5)



WRITE CYCLE 2 (CE# and CE2 Controlled) (1,4,5)



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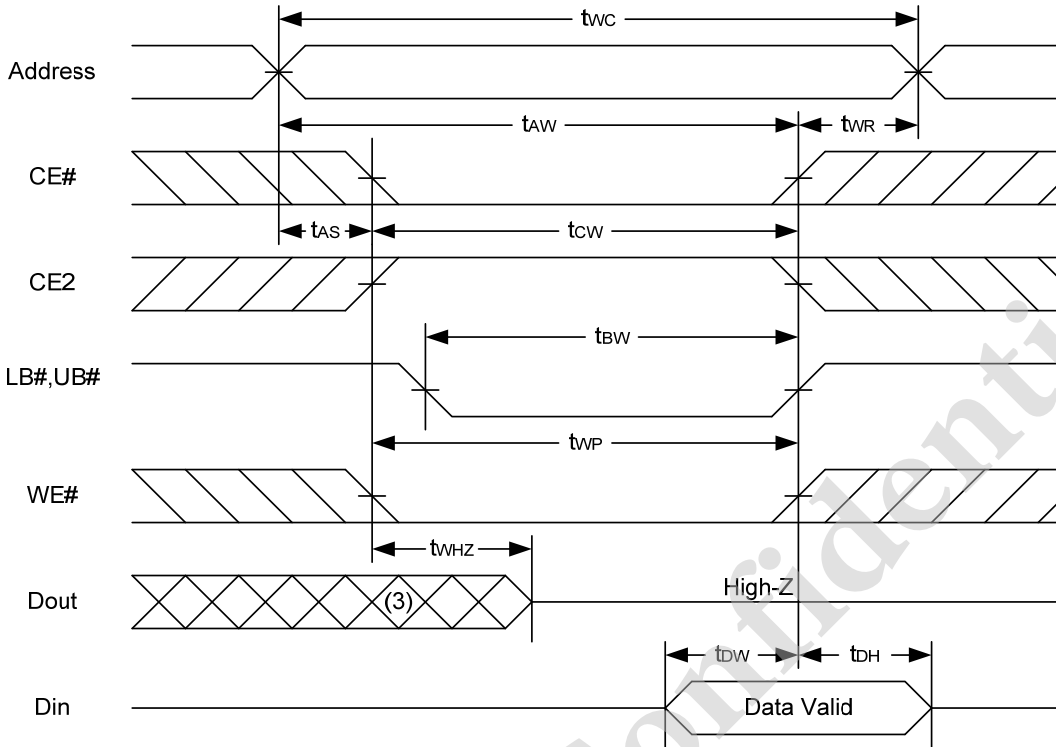
2F, No.17, Industry E. Rd. II, Science-Based Industrial Park, Hsinchu 300, Taiwan.

TEL: 886-3-6668838

FAX: 886-3-6668836



WRITE CYCLE 3 (LB#,UB# Controlled) (1,4,5)



Notes :

1. A write occurs during the overlap of a low CE#, high CE2, low WE#, LB# or UB# = low.
2. During a WE# controlled write cycle with OE# low, t_{WP} must be greater than $t_{wHZ} + t_{DW}$ to allow the drivers to turn off and data to be placed on the bus.
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the CE#, LB#, UB# low transition and CE2 high transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
5. t_{ow} and t_{wHZ} are specified with $C_L = 5pF$. Transition is measured $\pm 500mV$ from steady state.



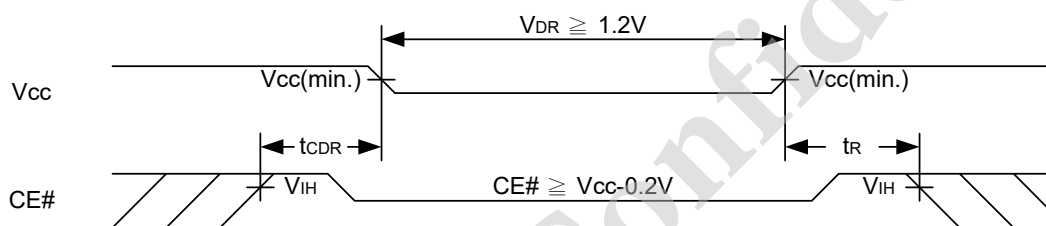
DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT		
V _{CC} for Data Retention	V _{DR}	CE# ≥ V _{CC} - 0.2V or CE2 ≤ 0.2V	1.2	-	3.6	V		
Data Retention Current	I _{DR}	V _{CC} = 1.2V CE# ≥ V _{CC} - 0.2V or CE2 ≤ 0.2V Other pins at 0.2V or V _{CC} - 0.2V	-SL	25°C	-	10	32	μA
			-SLI	40°C	-	10	36	μA
			-SL		-	-	100	μA
			-SLI		-	-	160	μA
Chip Disable to Data Retention Time	t _{CDR}	See Data Retention Waveforms (below)	0	-	-	ns		
Recovery Time	t _R		t _{RC} *	-	-	ns		

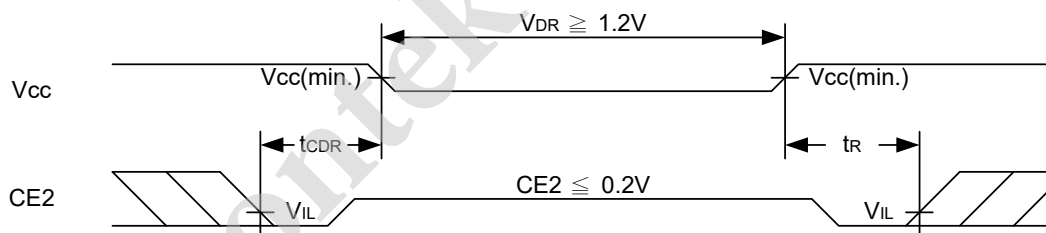
t_{RC}* = Read Cycle Time

DATA RETENTION WAVEFORM

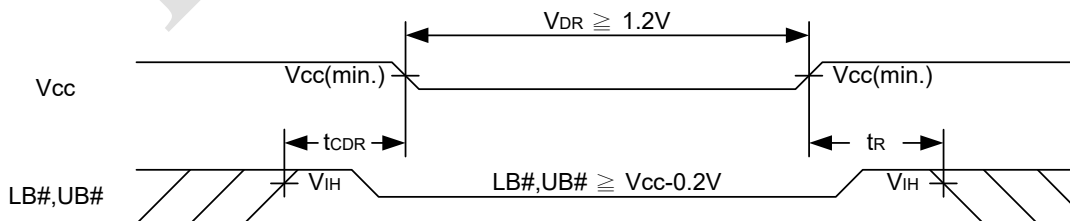
Low V_{CC} Data Retention Waveform (1) (CE# controlled)



Low V_{CC} Data Retention Waveform (2) (CE2 controlled)



Low V_{CC} Data Retention Waveform (3) (LB#, UB# controlled)



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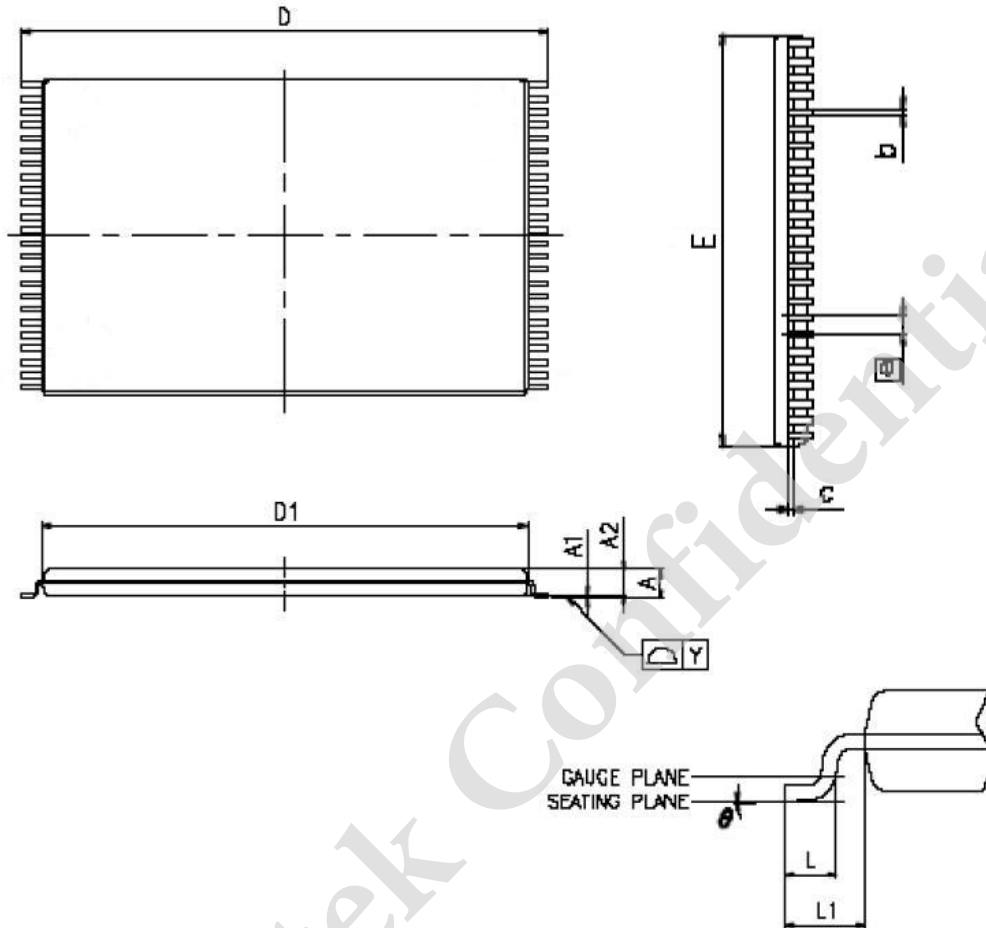
2F, No.17, Industry E. Rd. II, Science-Based Industrial Park, Hsinchu 300, Taiwan.

TEL: 886-3-6668838

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PACKAGE OUTLINE DIMENSION

48-pin 12mm x 20mm TSOP I Package Outline Dimension



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX
A	-	-	1.20
A1	0.05	-	0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
c	0.10	-	0.21
D	19.80	20.00	20.20
D1	18.30	18.40	18.50
E	11.90	12.00	12.10
\ominus	0.50 BASIC		
L	0.50	0.60	0.70
L1	-	0.80	-
Y	-	-	0.10
θ	0°	-	5°

NOTES:

- 1 JEDEC OUTLINE : MO-142 DD
2. PROFILE TOLERANCE ZONES FOR D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION ON E IS 0.15mm PER SIDE AND ON D1 IS 0.25mm PER SIDE.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.



ORDERING INFORMATION

Package Type	Access Time (Speed)(ns)	Power Type	Temperature Range(°C)	Packing Type	Lyontek Item No.
48-pin (12mm x 20mm) TSOP I	55	Special Ultra Low Power	0°C~70°C	Tray	LY62L409816ALL-55SL
				Tape Reel	LY62L409816ALL-55SLT
			-40°C~85°C	Tray	LY62L409816ALL-55SLI
				Tape Reel	LY62L409816ALL-55SLIT

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