



#### REVISION HISTORY

| <u>Revision</u> | <u>Description</u>  | <u>Issue Date</u> |
|-----------------|---|-------------------|
| Rev. 1.0        | Initial Issue   | Nov.1.2007        |
| Rev. 1.1        | Added I <sub>SB</sub> Spec.   | Feb.1.2008        |
| Rev. 1.2        | Revised <b>ORDERING INFORMATION</b>   | Feb.13.2008       |
| Rev. 1.3        | Added SL Spec.  | Jul.2.2008        |
| Rev. 1.4        | Added I <sub>SB1</sub> /I <sub>DR</sub> values when T <sub>A</sub> = 25°C and T <sub>A</sub> = 40°C<br>Revised <b>FEATURES &amp; ORDERING INFORMATION</b> <b>Lead</b><br><b>free and green package available</b> to <b>Green package available</b><br>Added packing type in <b>ORDERING INFORMATION</b><br>Deleted T <sub>SOLDER</sub> in <b>ABSOLUTE MAXIMUM RATINGS</b> | Mar.30.2009       |
| Rev. 1.5        | Revised <b>ORDERING INFORMATION</b> in page 11  | Aug.30.2010       |
| Rev. 1.6        | Deleted E grade   | Apr.12.2011       |
| Rev. 1.7        | Added -45ns Spec.   | Oct.1.2015        |
| Rev. 1.8        | Deleted <b>WRITE CYCLE</b> Notes :<br>1.WE#,CE#, LB#, UB# must be high during all address transitions.in page 8   | Jun.29.2016       |
| Rev. 1.9        | Deleted -45ns Spec.   | Nov.14.2016       |

### FEATURES

- Fast access time : 55/70ns
- Low power consumption:  
 Operating current : 30/20mA (TYP.)  
 Standby current : 5 $\mu$ A (TYP.) LL-version  
                           1.5 $\mu$ A (TYP.) SL-version
- Single 2.7V ~ 3.6V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data byte control : LB# (DQ0 ~ DQ7)  
                           UB# (DQ8 ~ DQ15)
- Data retention voltage : 1.2V (MIN.)
- **Green package available**
- Package : 44-pin 400mil TSOP II  
                   48-ball 6mm x 8mm TFBGA

### GENERAL DESCRIPTION

The LY62L51216 is a 8,388,608-bit low power CMOS static random access memory organized as 524,288 words by 16 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

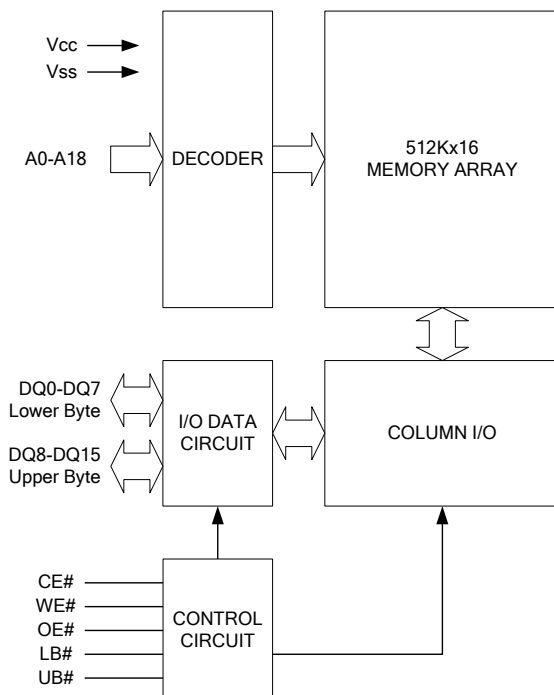
The LY62L51216 is well designed for low power application, and particularly well suited for battery back-up nonvolatile memory application.

The LY62L51216 operates from a single power supply of 2.7V ~ 3.6V and all inputs and outputs are fully TTL compatible

### PRODUCT FAMILY

| Product Family | Operating Temperature | V <sub>cc</sub> Range | Speed   | Power Dissipation               |                                  |
|----------------|-----------------------|-----------------------|---------|---------------------------------|----------------------------------|
|                |                       |                       |         | Standby(I <sub>SB1</sub> ,TYP.) | Operating(I <sub>cc</sub> ,TYP.) |
| LY62L51216     | 0 ~ 70°C              | 2.7 ~ 3.6V            | 55/70ns | 5 $\mu$ A(LL)/1.5 $\mu$ A(SL)   | 30/20mA                          |
| LY62L51216(I)  | -40 ~ 85°C            | 2.7 ~ 3.6V            | 55/70ns | 5 $\mu$ A(LL)/1.5 $\mu$ A(SL)   | 30/20mA                          |

### FUNCTIONAL BLOCK DIAGRAM

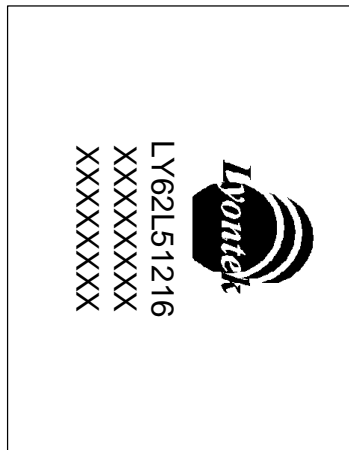
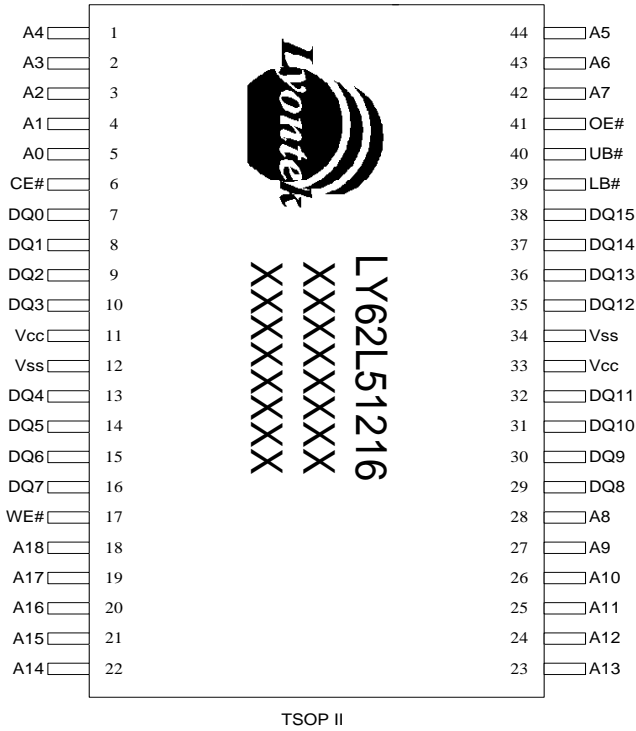


### PIN DESCRIPTION

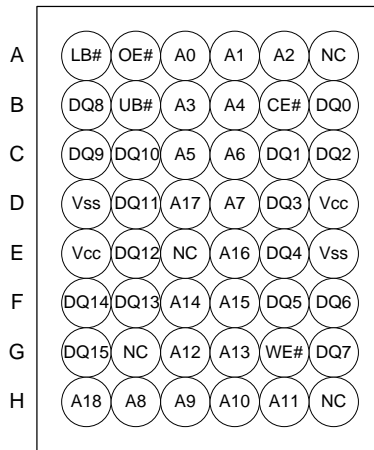
| SYMBOL          | DESCRIPTION         |
|-----------------|---------------------|
| A0 - A18        | Address Inputs      |
| DQ0 - DQ15      | Data Inputs/Outputs |
| CE#             | Chip Enable Input   |
| WE#             | Write Enable Input  |
| OE#             | Output Enable Input |
| LB#             | Lower Byte Control  |
| UB#             | Upper Byte Control  |
| V <sub>cc</sub> | Power Supply        |
| V <sub>ss</sub> | Ground              |



**PIN CONFIGURATION**



TFPGA(Top View)



TFPGA (See through with Top View)



### ABSOLUTE MAXIMUM RATINGS\*

| PARAMETER  | SYMBOL           | RATING                       | UNIT |
|--|------------------|------------------------------|------|
| Voltage on V <sub>CC</sub> relative to V <sub>SS</sub> | V <sub>T1</sub>  | -0.5 to 4.6                  | V    |
| Voltage on any other pin relative to V <sub>SS</sub>   | V <sub>T2</sub>  | -0.5 to V <sub>CC</sub> +0.5 | V    |
| Operating Temperature                                  | T <sub>A</sub>   | 0 to 70(C grade)             | °C   |
|  |                  | -40 to 85(I grade)           |      |
| Storage Temperature                                    | T <sub>STG</sub> | -65 to 150                   | °C   |
| Power Dissipation                                      | P <sub>D</sub>   | 1                            | W    |
| DC Output Current                                      | I <sub>OUT</sub> | 50                           | mA   |

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

### TRUTH TABLE

| MODE           | CE# | OE# | WE# | LB# | UB# | I/O OPERATION    |                  | SUPPLY CURRENT                     |
|----------------|-----|-----|-----|-----|-----|------------------|------------------|------------------------------------|
|                |     |     |     |     |     | DQ0-DQ7          | DQ8-DQ15         |                                    |
| Standby        | H   | X   | X   | X   | X   | High – Z         | High – Z         | I <sub>SB</sub> , I <sub>SB1</sub> |
|                | X   | X   | X   | H   | H   | High – Z         | High – Z         |                                    |
| Output Disable | L   | H   | H   | L   | X   | High – Z         | High – Z         | I <sub>CC</sub> , I <sub>CC1</sub> |
|                | L   | H   | H   | X   | L   | High – Z         | High – Z         |                                    |
| Read           | L   | L   | H   | L   | H   | D <sub>OUT</sub> | High – Z         | I <sub>CC</sub> , I <sub>CC1</sub> |
|                | L   | L   | H   | H   | L   | High – Z         | D <sub>OUT</sub> |                                    |
|                | L   | L   | H   | L   | L   | D <sub>OUT</sub> | D <sub>OUT</sub> |                                    |
| Write          | L   | X   | L   | L   | H   | D <sub>IN</sub>  | High – Z         | I <sub>CC</sub> , I <sub>CC1</sub> |
|                | L   | X   | L   | H   | L   | High – Z         | D <sub>IN</sub>  |                                    |
|                | L   | X   | L   | L   | L   | D <sub>IN</sub>  | D <sub>IN</sub>  |                                    |

Note: H = V<sub>IH</sub>, L = V<sub>IL</sub>, X = Don't care.



### DC ELECTRICAL CHARACTERISTICS

| PARAMETER                              | SYMBOL             | TEST CONDITION   | MIN.  | TYP.*4 | MAX.                 | UNIT |    |    |
|--|--------------------|--|-------|--------|----------------------|------|----|----|
| Supply Voltage                         | V <sub>CC</sub>    |  | 2.7   | 3.0    | 3.6                  | V    |    |    |
| Input High Voltage                     | V <sub>IH</sub> *1 |  | 2.2   | -      | V <sub>CC</sub> +0.3 | V    |    |    |
| Input Low Voltage                      | V <sub>IL</sub> *2 |  | - 0.2 | -      | 0.6                  | V    |    |    |
| Input Leakage Current                  | I <sub>LI</sub>    | V <sub>CC</sub> ≥ V <sub>IN</sub> ≥ V <sub>SS</sub>  | - 1   | -      | 1                    | μA   |    |    |
| Output Leakage Current                 | I <sub>LO</sub>    | V <sub>CC</sub> ≥ V <sub>OUT</sub> ≥ V <sub>SS</sub> ,<br>Output Disabled  | - 1   | -      | 1                    | μA   |    |    |
| Output High Voltage                    | V <sub>OH</sub>    | I <sub>OH</sub> = -1mA   | 2.2   | 2.7    | -                    | V    |    |    |
| Output Low Voltage                     | V <sub>OL</sub>    | I <sub>OL</sub> = 2mA  | -     | -      | 0.4                  | V    |    |    |
| Average Operating Power supply Current | I <sub>CC</sub>    | Cycle time = Min.<br>CE# = V <sub>IL</sub> ,<br>I <sub>I/O</sub> = 0mA<br>Other pins at V <sub>IL</sub> or V <sub>IH</sub> | - 55  | -      | 30                   | 40   | mA |    |
|  |                    |  | - 70  | -      | 20                   | 30   | mA |    |
|  | I <sub>CC1</sub>   | Cycle time = 1μs<br>CE# = 0.2V , I <sub>I/O</sub> = 0mA<br>Other pins at 0.2V or V <sub>CC</sub> - 0.2V                    | -     | 4      | 8                    | mA   |    |    |
| Standby Power Supply Current           | I <sub>SB</sub>    | CE# = V <sub>IH</sub> . Other pins at V <sub>IL</sub> or V <sub>IH</sub>   | -     | 0.15   | 1                    | mA   |    |    |
|  | I <sub>SB1</sub>   | CE# ≥ V <sub>CC</sub> - 0.2V<br>Others at 0.2V or V <sub>CC</sub> - 0.2V   | LL    | -      | 5                    | 30   | μA |    |
|  |                    |  | LLI   | -      | 5                    | 50   | μA |    |
|  |                    |  | SL*5  | 25°C   | -                    | 1.5  | 5  | μA |
|  |                    |  | SLI*5 | 40°C   | -                    | 1.5  | 5  | μA |
|  |                    |  | SL    |        | -                    | 1.5  | 15 | μA |
| SLI                                    |                    | -  | 1.5   | 20     | μA                   |      |    |    |

Notes:

- V<sub>IH</sub>(max) = V<sub>CC</sub> + 3.0V for pulse width less than 10ns.
- V<sub>IL</sub>(min) = V<sub>SS</sub> - 3.0V for pulse width less than 10ns.
- Over/Undershoot specifications are characterized, not 100% tested.
- Typical values are included for reference only and are not guaranteed or tested.  
Typical values are measured at V<sub>CC</sub> = V<sub>CC</sub>(TYP.) and T<sub>A</sub> = 25°C
- This parameter is measured at V<sub>CC</sub> = 3.0V

### CAPACITANCE (T<sub>A</sub> = 25°C, f = 1.0MHz)

| PARAMETER                | SYMBOL           | MIN. | MAX | UNIT |
|--------------------------|------------------|------|-----|------|
| Input Capacitance        | C <sub>IN</sub>  | -    | 6   | pF   |
| Input/Output Capacitance | C <sub>I/O</sub> | -    | 8   | pF   |

Note : These parameters are guaranteed by device characterization, but not production tested.

### AC TEST CONDITIONS

|  |   |
|--|---|
| Input Pulse Levels                       | 0.2V to V <sub>CC</sub> - 0.2V  |
| Input Rise and Fall Times                | 3ns   |
| Input and Output Timing Reference Levels | 1.5V  |
| Output Load                              | C <sub>L</sub> = 30pF + 1TTL, I <sub>OH</sub> /I <sub>OL</sub> = -1mA/2mA |

**AC ELECTRICAL CHARACTERISTICS**
**(1) READ CYCLE**

| PARAMETER                          | SYM.               | LY62L51216-55 |      | LY62L51216-70 |      | UNIT |
|------------------------------------|--------------------|---------------|------|---------------|------|------|
|                                    |                    | MIN.          | MAX. | MIN.          | MAX. |      |
| Read Cycle Time                    | t <sub>RC</sub>    | 55            | -    | 70            | -    | ns   |
| Address Access Time                | t <sub>AA</sub>    | -             | 55   | -             | 70   | ns   |
| Chip Enable Access Time            | t <sub>ACE</sub>   | -             | 55   | -             | 70   | ns   |
| Output Enable Access Time          | t <sub>OE</sub>    | -             | 30   | -             | 35   | ns   |
| Chip Enable to Output in Low-Z     | t <sub>CLZ</sub> * | 10            | -    | 10            | -    | ns   |
| Output Enable to Output in Low-Z   | t <sub>OLZ</sub> * | 5             | -    | 5             | -    | ns   |
| Chip Disable to Output in High-Z   | t <sub>CHZ</sub> * | -             | 20   | -             | 25   | ns   |
| Output Disable to Output in High-Z | t <sub>OHZ</sub> * | -             | 20   | -             | 25   | ns   |
| Output Hold from Address Change    | t <sub>OH</sub>    | 10            | -    | 10            | -    | ns   |
| LB#, UB# Access Time               | t <sub>BA</sub>    | -             | 55   | -             | 70   | ns   |
| LB#, UB# to High-Z Output          | t <sub>BHZ</sub> * | -             | 25   | -             | 30   | ns   |
| LB#, UB# to Low-Z Output           | t <sub>BLZ</sub> * | 10            | -    | 10            | -    | ns   |

**(2) WRITE CYCLE**

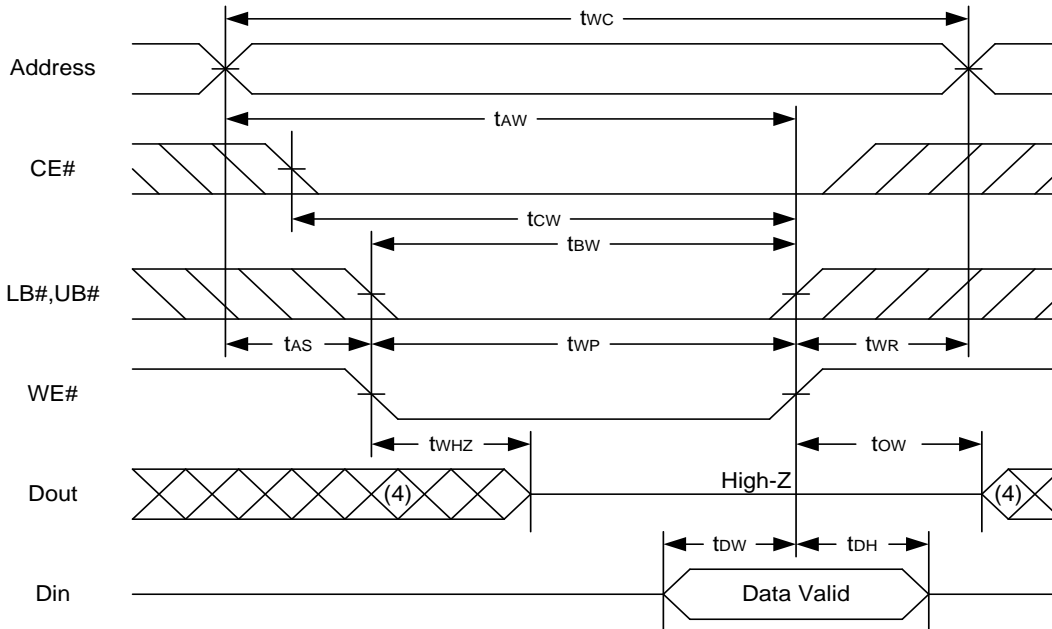
| PARAMETER                        | SYM.               | LY62L51216-55 |      | LY62L51216-70 |      | UNIT |
|----------------------------------|--------------------|---------------|------|---------------|------|------|
|                                  |                    | MIN.          | MAX. | MIN.          | MAX. |      |
| Write Cycle Time                 | t <sub>WC</sub>    | 55            | -    | 70            | -    | ns   |
| Address Valid to End of Write    | t <sub>AW</sub>    | 50            | -    | 60            | -    | ns   |
| Chip Enable to End of Write      | t <sub>CW</sub>    | 50            | -    | 60            | -    | ns   |
| Address Set-up Time              | t <sub>AS</sub>    | 0             | -    | 0             | -    | ns   |
| Write Pulse Width                | t <sub>WP</sub>    | 45            | -    | 55            | -    | ns   |
| Write Recovery Time              | t <sub>WR</sub>    | 0             | -    | 0             | -    | ns   |
| Data to Write Time Overlap       | t <sub>DW</sub>    | 25            | -    | 30            | -    | ns   |
| Data Hold from End of Write Time | t <sub>DH</sub>    | 0             | -    | 0             | -    | ns   |
| Output Active from End of Write  | t <sub>OW</sub> *  | 5             | -    | 5             | -    | ns   |
| Write to Output in High-Z        | t <sub>WHZ</sub> * | -             | 20   | -             | 25   | ns   |
| LB#, UB# Valid to End of Write   | t <sub>BW</sub>    | 45            | -    | 60            | -    | ns   |

\*These parameters are guaranteed by device characterization, but not production tested.

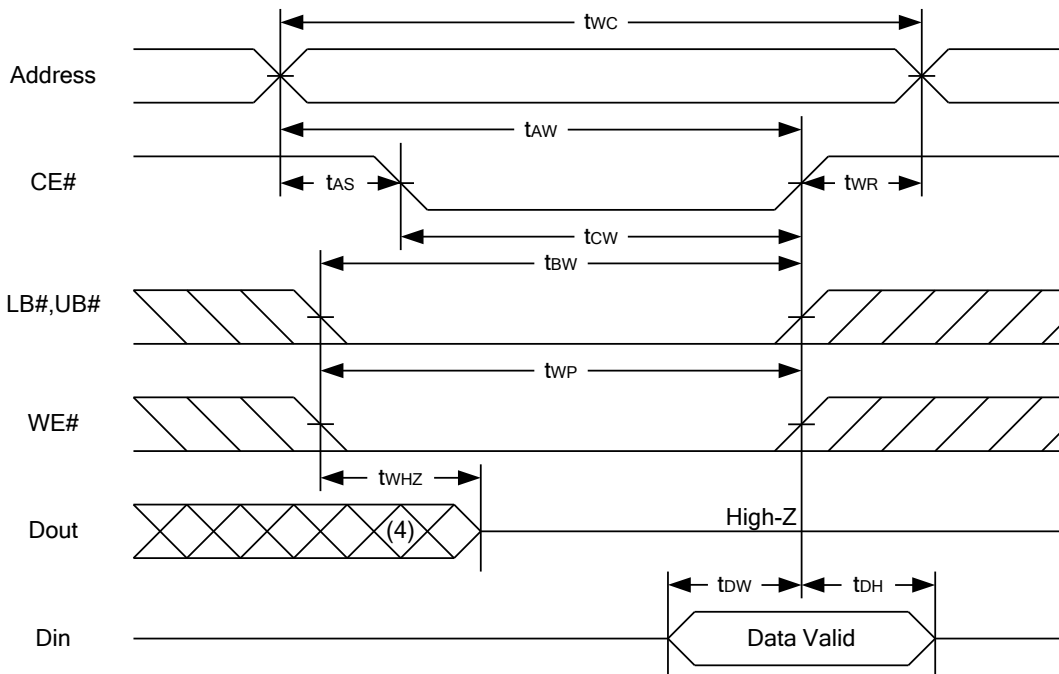




#### WRITE CYCLE 1 (WE# Controlled) (1,2,4,5)



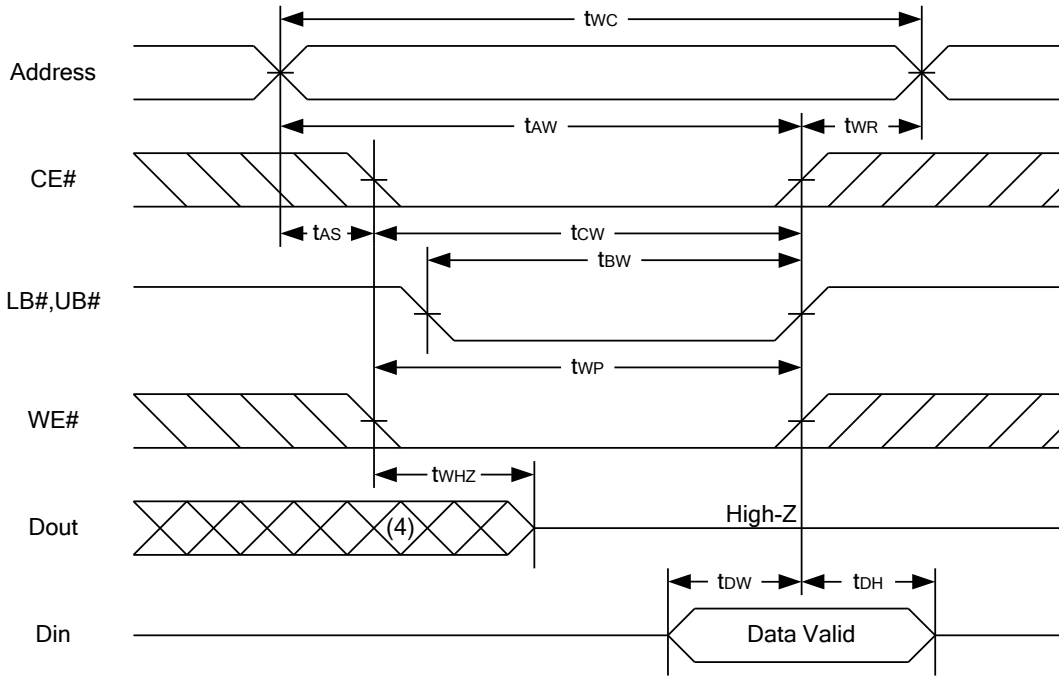
#### WRITE CYCLE 2 (CE# Controlled) (1,4,5)







#### WRITE CYCLE 3 (LB#,UB# Controlled) (1,4,5)



Notes :

1. A write occurs during the overlap of a low CE#, low WE#, LB# or UB# = low.
2. During a WE# controlled write cycle with OE# low, tWP must be greater than tWHZ + tDW to allow the drivers to turn off and data to be placed on the bus.
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the CE#, LB#, UB# low transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
5. tOW and tWHZ are specified with CL = 5pF. Transition is measured ±500mV from steady state.



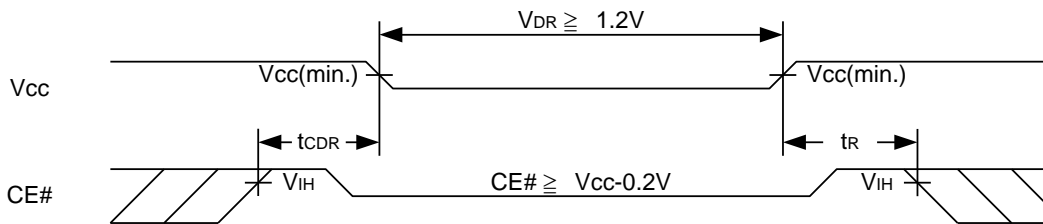
**DATA RETENTION CHARACTERISTICS**

| PARAMETER                           | SYMBOL           | TEST CONDITION  | MIN.              | TYP. | MAX. | UNIT |    |
|-------------------------------------|------------------|---|-------------------|------|------|------|----|
| V <sub>CC</sub> for Data Retention  | V <sub>DR</sub>  | CE# ≥ V <sub>CC</sub> - 0.2V  | 1.2               | -    | 3.6  | V    |    |
| Data Retention Current              | I <sub>DR</sub>  | V <sub>CC</sub> = 1.2V<br>CE# ≥ V <sub>CC</sub> - 0.2V<br>Other pins at 0.2V or V <sub>CC</sub> -0.2V | LL                | -    | 2    | 25   | μA |
|                                     |                  |   | LLI               | -    | 2    | 40   | μA |
|                                     |                  |   | SL 25°C           | -    | 1    | 3    | μA |
|                                     |                  |   | SLI 40°C          | -    | 1    | 3    | μA |
|                                     |                  |   | SL                | -    | 1    | 15   | μA |
|                                     |                  |   | SLI               | -    | 1    | 20   | μA |
| Chip Disable to Data Retention Time | t <sub>CDR</sub> | See Data Retention Waveforms (below)  | 0                 | -    | -    | ns   |    |
| Recovery Time                       | t <sub>R</sub>   |   | t <sub>RC</sub> * | -    | -    | ns   |    |

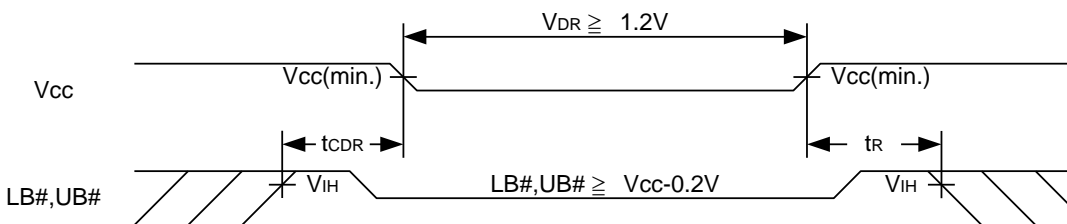
t<sub>RC</sub>\* = Read Cycle Time

**DATA RETENTION WAVEFORM**

**Low V<sub>CC</sub> Data Retention Waveform (1) (CE# controlled)**



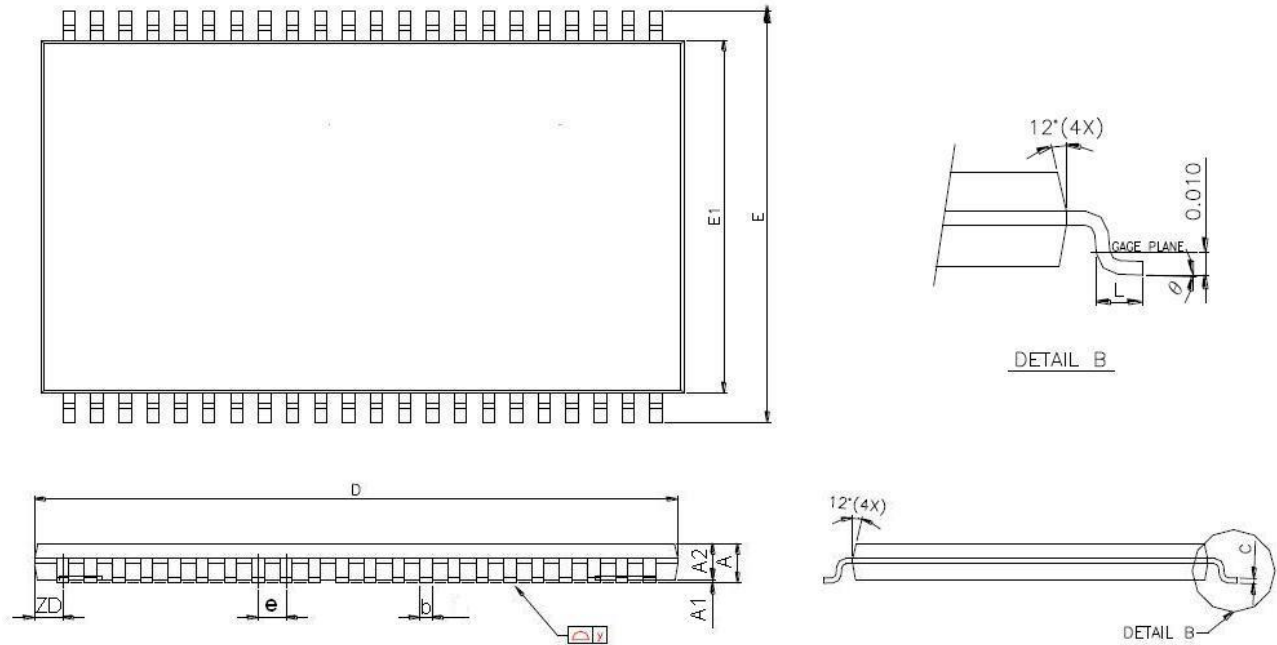
**Low V<sub>CC</sub> Data Retention Waveform (2) (LB#, UB# controlled)**





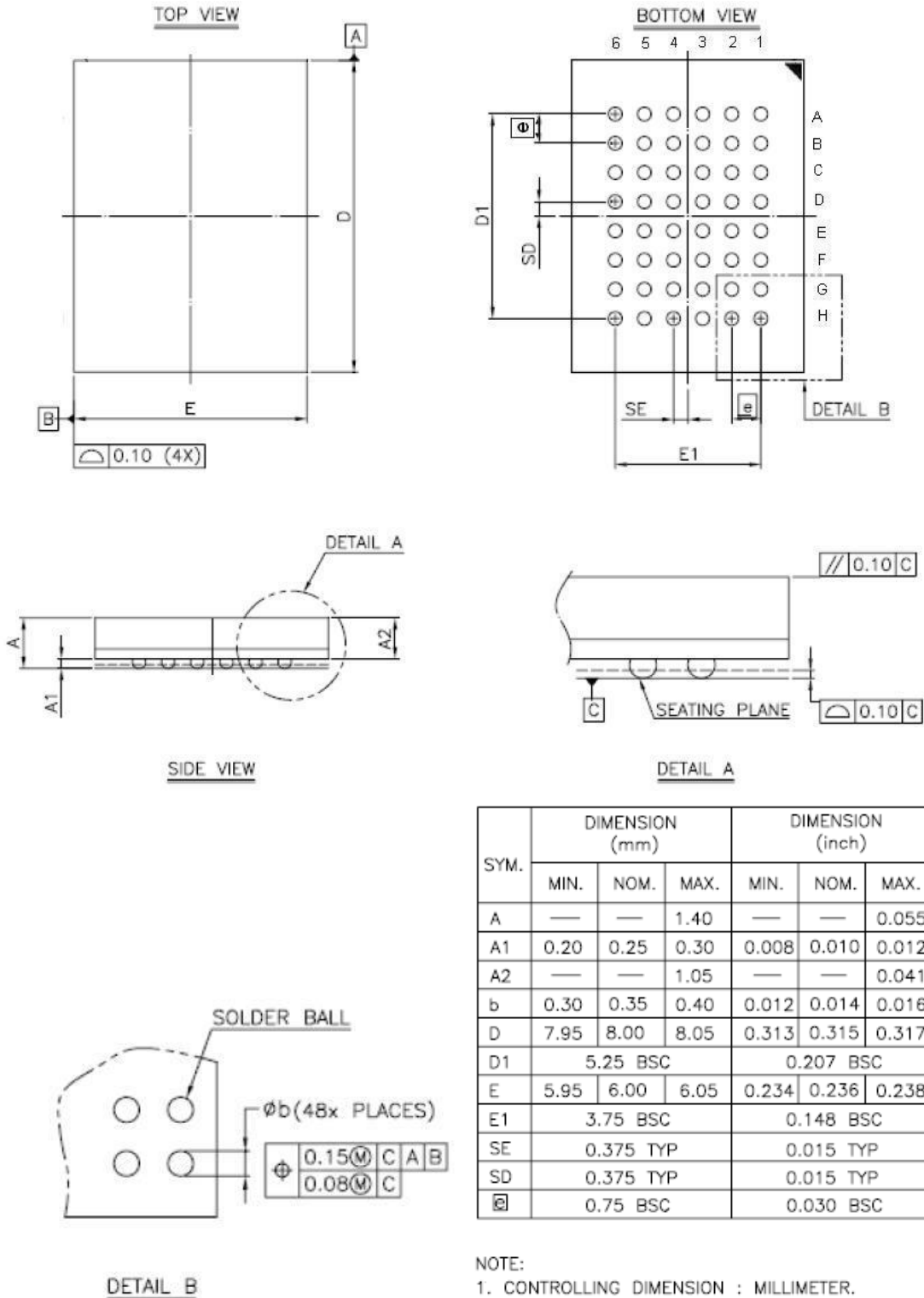
### PACKAGE OUTLINE DIMENSION

#### 44-pin 400mil TSOP II Package Outline Dimension



| SYMBOLS | DIMENSIONS IN MILLMETERS |        |        | DIMENSIONS IN MILS |      |      |
|---------|--------------------------|--------|--------|--------------------|------|------|
|         | MIN.                     | NOM.   | MAX.   | MIN.               | NOM. | MAX. |
| A       | -                        | -      | 1.20   | -                  | -    | 47.2 |
| A1      | 0.05                     | 0.10   | 0.15   | 2.0                | 3.9  | 5.9  |
| A2      | 0.95                     | 1.00   | 1.05   | 37.4               | 39.4 | 41.3 |
| b       | 0.30                     | -      | 0.45   | 11.8               | -    | 17.7 |
| c       | 0.12                     | -      | 0.21   | 4.7                | -    | 8.3  |
| D       | 18.212                   | 18.415 | 18.618 | 717                | 725  | 733  |
| E       | 11.506                   | 11.760 | 12.014 | 453                | 463  | 473  |
| E1      | 9.957                    | 10.160 | 10.363 | 392                | 400  | 408  |
| e       | -                        | 0.800  | -      | -                  | 31.5 | -    |
| L       | 0.40                     | 0.50   | 0.60   | 15.7               | 19.7 | 23.6 |
| ZD      | -                        | 0.805  | -      | -                  | 31.7 | -    |
| y       | -                        | -      | 0.076  | -                  | -    | 3    |
| θ       | 0°                       | 3°     | 6°     | 0°                 | 3°   | 6°   |

#### 48-ball 6mm x 8mm TFBGA Package Outline Dimension



NOTE:  
 1. CONTROLLING DIMENSION : MILLIMETER.  
 2. REFERENCE DOCUMENT : JEDEC MO-207.



#### ORDERING INFORMATION

| Package Type               | Access Time (Speed/ns) | Power Type              | Temperature Range(°C) | Packing Type        | Lyontek Item No.   |
|----------------------------|------------------------|-------------------------|-----------------------|---------------------|--------------------|
| 44-pin (400mil)<br>TSOP II | 55                     | Special Ultra Low Power | 0°C ~70°C             | Tray                | LY62L51216ML-55SL  |
|                            |                        |                         |                       | Tape Reel           | LY62L51216ML-55SLT |
|                            |                        |                         | -40°C ~85°C           | Tray                | LY62L51216ML-55SLI |
|                            |                        |                         | Tape Reel             | LY62L51216ML-55SLIT |                    |
|                            |                        | Ultra Low Power         | 0°C ~70°C             | Tray                | LY62L51216ML-55LL  |
|                            |                        |                         | -40°C ~85°C           | Tray                | LY62L51216ML-55LLI |
|                            | 70                     | Special Ultra Low Power | 0°C ~70°C             | Tray                | LY62L51216ML-70SL  |
|                            |                        |                         |                       | Tape Reel           | LY62L51216ML-70SLT |
|                            |                        |                         | -40°C ~85°C           | Tray                | LY62L51216ML-70SLI |
|                            |                        |                         | Tape Reel             | LY62L51216ML-70SLIT |                    |
|                            |                        | Ultra Low Power         | 0°C ~70°C             | Tray                | LY62L51216ML-70LL  |
|                            |                        |                         | -40°C ~85°C           | Tray                | LY62L51216ML-70LLI |
|                            | Tape Reel              | LY62L51216ML-70LLIT     |                       |                     |                    |



#### ORDERING INFORMATION

| Package Type                    | Access Time<br>(Speed/ns) | Power Type                 | Temperature<br>Range(°C) | Packing<br>Type | Lyontek Item No.    |
|---------------------------------|---------------------------|----------------------------|--------------------------|-----------------|---------------------|
| 48-ball<br>(6mm x 8mm)<br>TFBGA | 55                        | Special Ultra<br>Low Power | 0°C ~70°C                | Tray            | LY62L51216GL-55SL   |
|                                 |                           |                            |                          | Tape Reel       | LY62L51216GL-55SLT  |
|                                 |                           |                            | -40°C ~85°C              | Tray            | LY62L51216GL-55SLI  |
|                                 |                           |                            |                          | Tape Reel       | LY62L51216GL-55SLIT |
|                                 |                           | Ultra Low<br>Power         | 0°C ~70°C                | Tray            | LY62L51216GL-55LL   |
|                                 |                           |                            |                          | Tape Reel       | LY62L51216GL-55LLT  |
|                                 | 70                        | Special Ultra<br>Low Power | 0°C ~70°C                | Tray            | LY62L51216GL-70SL   |
|                                 |                           |                            |                          | Tape Reel       | LY62L51216GL-70SLT  |
|                                 |                           |                            | -40°C ~85°C              | Tray            | LY62L51216GL-70SLI  |
|                                 |                           |                            |                          | Tape Reel       | LY62L51216GL-70SLIT |
|                                 |                           | Ultra Low<br>Power         | 0°C ~70°C                | Tray            | LY62L51216GL-70LL   |
|                                 |                           |                            |                          | Tape Reel       | LY62L51216GL-70LLT  |
|                                 | -40°C ~85°C               | Tray                       | LY62L51216GL-70LLI       |                 |                     |
|                                 |                           | Tape Reel                  | LY62L51216GL-70LLIT      |                 |                     |



**Lyontek Inc.**

**LY62L51216**

Rev. 1.9

**512K X 16 BIT LOW POWER CMOS SRAM**

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