



REVISION HISTORY

<u>Revision</u>	<u>Description</u>	<u>Issue Date</u>
Rev. 1.0	Initial Issue	Oct.28.2008
Rev. 1.1	Revised FEATURES & ORDERING INFORMATION Lead free and green package available to Green package available Added packing type in ORDERING INFORMATION Deleted T _{SOLDER} in ABSOLUTE MAXIMUM RATINGS Revised PACKAGE OUTLINE DIMENSION in page 11 Revised V _{DR} to 1.5V	May.6.2010
Rev. 1.2	Revised ORDERING INFORMATION in page 12	Aug.30.2010
Rev. 1.3	Added SL Grade Deleted E Grade Revised I _{SB1} /I _{DR}	Aug.9.2011
Rev. 1.4	Corrected ORDERING INFORMATION Typo.	May.20.2016
Rev. 1.5	Deleted WRITE CYCLE Notes : 1. WE#,CE#, LB#, UB# must be high during all address transitions. in page 8	Jun.29.2016
Rev. 1.6	Revised PIN DESCRIPTION & GENERAL DESCRIPTION in page 1	Feb.15.2017

FEATURES

- Fast access time : 55/70ns
- Low power consumption:
Operating current : 20/18mA (TYP.)
Standby current : 1 μ A (TYP.)
- Single 2.7V ~ 5.5V power supply
- All outputs TTL compatible
- Fully static operation
- Tri-state output
- Data byte control : LB# (DQ0 ~ DQ7)
UB# (DQ8 ~ DQ15)
- Data retention voltage : 1.5V (MIN.)
- **Green package available**
- Package : 44-pin 400 mil TSOP II
48-ball 6mm x 8mm TFBGA

GENERAL DESCRIPTION

The LY62W12816 is a 2,097,152-bit low power CMOS static random access memory organized as 131,072 words by 16 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

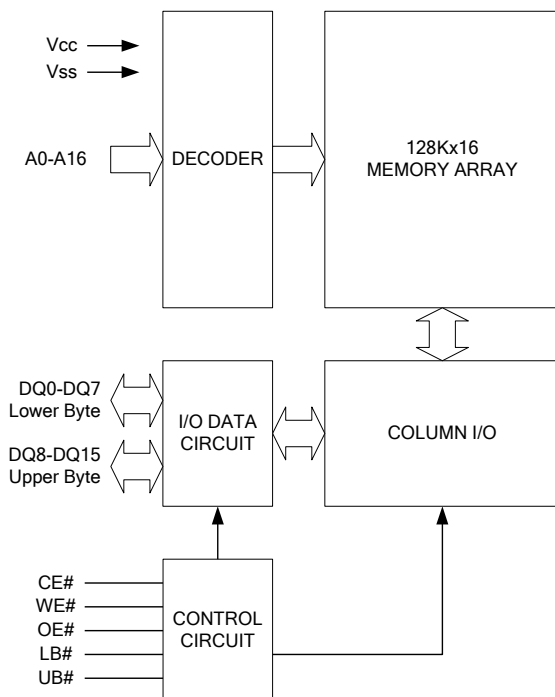
The LY62W12816 is well designed for low power application, and particularly well suited for battery back-up nonvolatile memory application.

The LY62W12816 operates from a single power supply of 2.7V ~ 5.5V and all outputs are fully TTL compatible.

PRODUCT FAMILY

Product Family	Operating Temperature	V _{CC} Range	Speed	Power Dissipation	
				Standby(I _{SB1} , TYP.)	Operating(I _{CC} , TYP.)
LY62W12816	0 ~ 70°C	2.7 ~ 5.5V	55/70ns	1 μ A	20/18mA
LY62W12816(I)	-40 ~ 85°C	2.7 ~ 5.5V	55/70ns	1 μ A	20/18mA

FUNCTIONAL BLOCK DIAGRAM

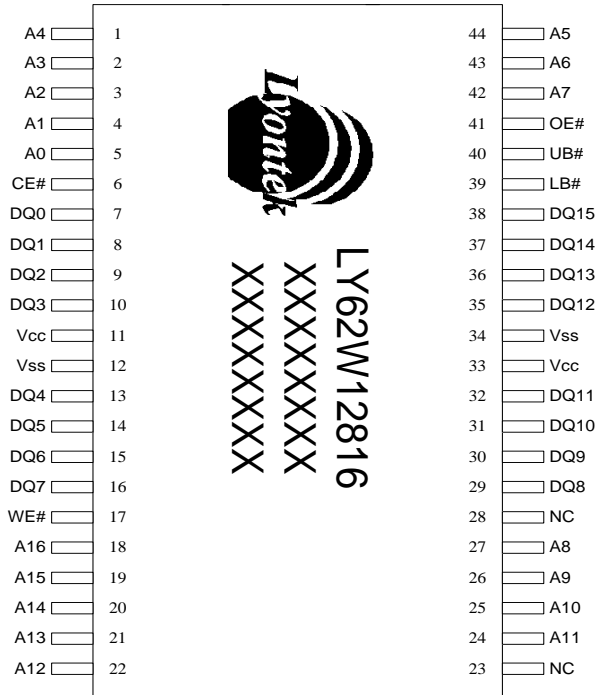


PIN DESCRIPTION

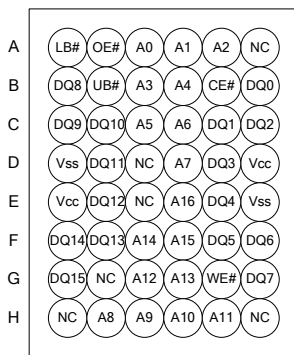
SYMBOL	DESCRIPTION
A0 - A16	Address Inputs
DQ0 - DQ15	Data Inputs/Outputs
CE#	Chip Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
LB#	Lower Byte Control
UB#	Upper Byte Control
V _{CC}	Power Supply
V _{SS}	Ground
NC	No Connection



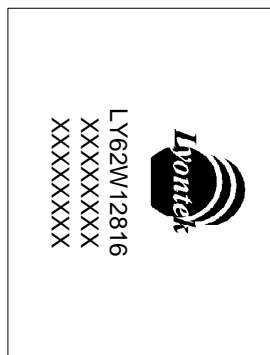
PIN CONFIGURATION



TSOP II



TFBGA(See through with Top View)



TFBGA(Top View)



ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on V _{CC} relative to V _{SS}	V _{T1}	-0.5 to 6.5	V
Voltage on any other pin relative to V _{SS}	V _{T2}	-0.5 to V _{CC} +0.5	V
Operating Temperature	T _A	0 to 70(C grade)	°C
		-40 to 85(I grade)	
Storage Temperature	T _{STG}	-65 to 150	°C
Power Dissipation	P _D	1	W
DC Output Current	I _{OUT}	50	mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE#	OE#	WE#	LB#	UB#	I/O OPERATION		SUPPLY CURRENT
						DQ0 - DQ7	DQ8 - DQ15	
Standby	H	X	X	X	X	High-Z	High-Z	I _{SB1}
	X	X	X	H	H	High-Z	High-Z	
Output Disable	L	H	H	L	X	High-Z	High-Z	I _{CC} , I _{CC1}
	L	H	H	X	L	High-Z	High-Z	
Read	L	L	H	L	H	D _{OUT}	High-Z	I _{CC} , I _{CC1}
	L	L	H	H	L	High-Z	D _{OUT}	
	L	L	H	L	L	D _{OUT}	D _{OUT}	
Write	L	X	L	L	H	D _{IN}	High-Z	I _{CC} , I _{CC1}
	L	X	L	H	L	High-Z	D _{IN}	
	L	X	L	L	L	D _{IN}	D _{IN}	

Note: H = V_{IH}, L = V_{IL}, X = Don't care.



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP. ^{*4}	MAX.	UNIT		
Supply Voltage	V _{CC}		2.7	3.0	5.5	V		
Input High Voltage	V _{IH} ^{*1}		0.7*V _{CC}	-	V _{CC} +0.3	V		
Input Low Voltage	V _{IL} ^{*2}		-0.2	-	0.6	V		
Input Leakage Current	I _{LI}	V _{CC} ≥ V _{IN} ≥ V _{SS}	-1	-	1	μA		
Output Leakage Current	I _{LO}	V _{CC} ≥ V _{OUT} ≥ V _{SS} , Output Disabled	-1	-	1	μA		
Output High Voltage	V _{OH}	I _{OH} = -1mA	2.4	2.7	-	V		
Output Low Voltage	V _{OL}	I _{OL} = 2mA	-	-	0.4	V		
Average Operating Power supply Current	I _{CC}	Cycle time = MIN. CE# = V _{IL} , I _{I/O} = 0mA Other pins at V _{IL} or V _{IH}	-55	-	20	60	mA	
			-70	-	18	50	mA	
	I _{CC1}	Cycle time = 1μs CE# = 0.2V, I _{I/O} = 0mA Other pins at 0.2V or V _{CC} - 0.2V	-	4	10	mA		
Standby Power Supply Current	I _{SB1}	CE# ≥ V _{CC} - 0.2V Others at 0.2V or V _{CC} - 0.2V	LL/LLI	-	1	50	μA	
			SL ^{*5}	25°C	-	1	5	μA
			SLI ^{*5}	40°C	-	1	5	μA
			SL	-	1	20	μA	
			SLI	-	1	25	μA	

Notes:

- V_{IH}(max) = V_{CC} + 3.0V for pulse width less than 10ns.
- V_{IL}(min) = V_{SS} - 3.0V for pulse width less than 10ns.
- Over/Undershoot specifications are characterized, not 100% tested.
- Typical values are included for reference only and are not guaranteed or tested.
Typical values are measured at V_{CC} = V_{CC}(TYP.) and T_A = 25°C
- This parameter is measured at V_{CC} = 3.0V

CAPACITANCE (T_A = 25°C, f = 1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Input Capacitance	C _{IN}	-	6	pF
Input/Output Capacitance	C _{I/O}	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0.2V to V _{CC} - 0.2V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	C _L = 30pF + 1TTL, I _{OH} /I _{OL} = -2mA/4mA



AC ELECTRICAL CHARACTERISTICS

(1) READ CYCLE

PARAMETER	SYM.	LY62W12816-55		LY62W12816-70		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t _{RC}	55	-	70	-	ns
Address Access Time	t _{AA}	-	55	-	70	ns
Chip Enable Access Time	t _{ACE}	-	55	-	70	ns
Output Enable Access Time	t _{OE}	-	30	-	35	ns
Chip Enable to Output in Low-Z	t _{CLZ} *	10	-	10	-	ns
Output Enable to Output in Low-Z	t _{OLZ} *	5	-	5	-	ns
Chip Disable to Output in High-Z	t _{CHZ} *	-	20	-	25	ns
Output Disable to Output in High-Z	t _{OHZ} *	-	20	-	25	ns
Output Hold from Address Change	t _{OH}	10	-	10	-	ns
LB#, UB# Access Time	t _{BA}	-	55	-	70	ns
LB#, UB# to High-Z Output	t _{BHZ} *	-	25	-	30	ns
LB#, UB# to Low-Z Output	t _{BLZ} *	10	-	10	-	ns

(2) WRITE CYCLE

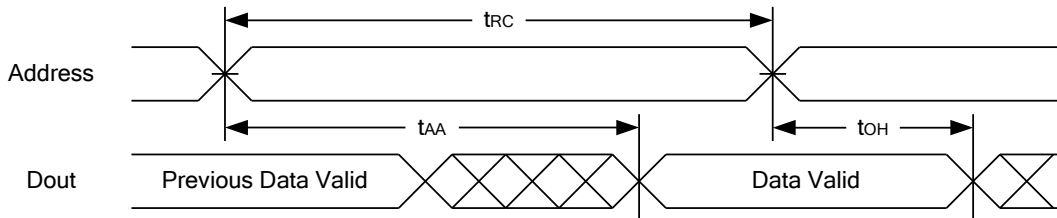
PARAMETER	SYM.	LY62W12816-55		LY62W12816-70		UNIT
		MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t _{WC}	55	-	70	-	ns
Address Valid to End of Write	t _{AW}	50	-	60	-	ns
Chip Enable to End of Write	t _{CW}	50	-	60	-	ns
Address Set-up Time	t _{AS}	0	-	0	-	ns
Write Pulse Width	t _{WP}	45	-	55	-	ns
Write Recovery Time	t _{WR}	0	-	0	-	ns
Data to Write Time Overlap	t _{DW}	25	-	30	-	ns
Data Hold from End of Write Time	t _{DH}	0	-	0	-	ns
Output Active from End of Write	t _{OW} *	5	-	5	-	ns
Write to Output in High-Z	t _{WHZ} *	-	20	-	25	ns
LB#, UB# Valid to End of Write	t _{BW}	50	-	60	-	ns

*These parameters are guaranteed by device characterization, but not production tested.

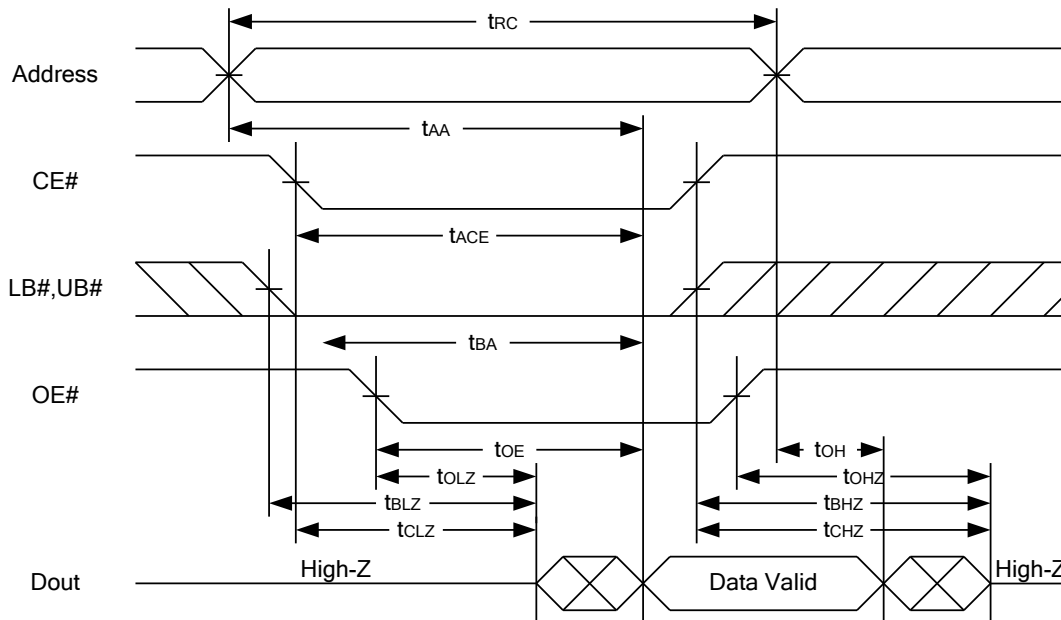


TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)



READ CYCLE 2 (CE# and OE# Controlled) (1,3,4,5)

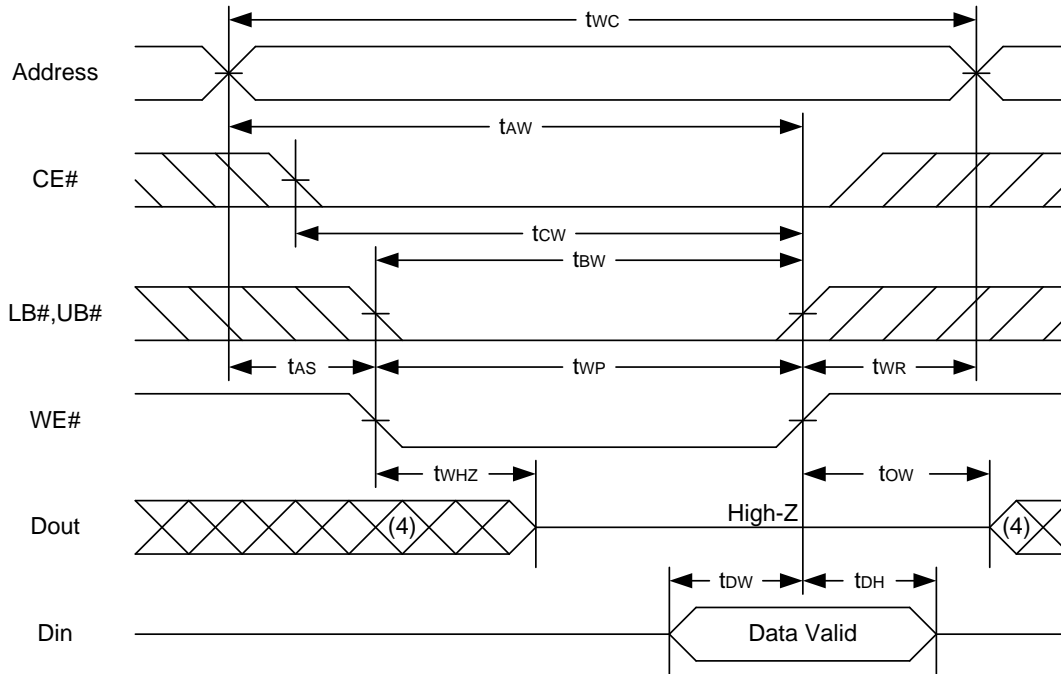


Notes :

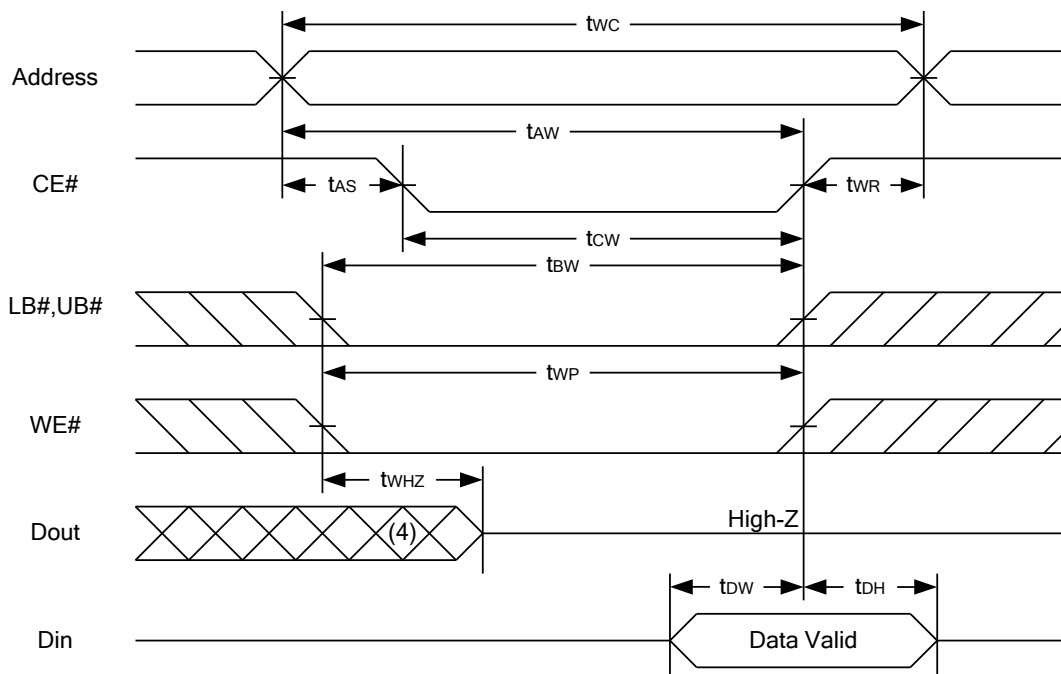
1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low, LB# or UB# = low.
3. Address must be valid prior to or coincident with CE# = low, LB# or UB# = low transition; otherwise t_{AA} is the limiting parameter.
4. t_{CLZ} , t_{BLZ} , t_{OLZ} , t_{CHZ} , t_{BHZ} and t_{OHZ} are specified with $C_L = 5pF$. Transition is measured $\pm 500mV$ from steady state.
5. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{BHZ} is less than t_{BLZ} , t_{OHZ} is less than t_{OLZ} .



WRITE CYCLE 1 (WE# Controlled) (1,2,4,5)

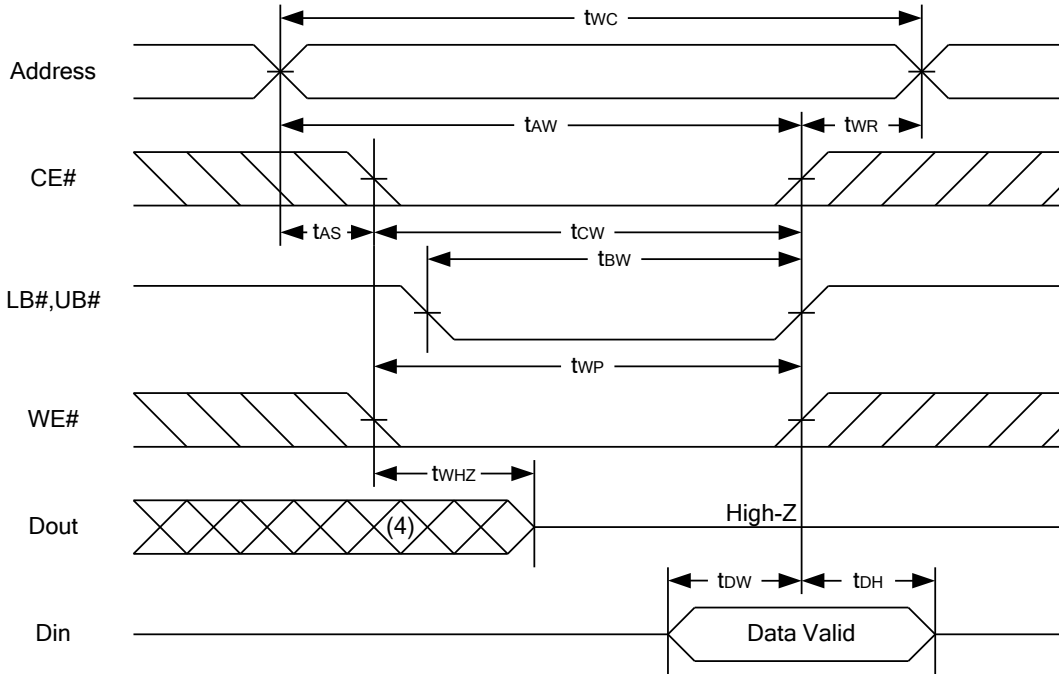


WRITE CYCLE 2 (CE# Controlled) (1,4,5)





WRITE CYCLE 3 (LB#,UB# Controlled) (1,4,5)



Notes :

1. A write occurs during the overlap of a low CE#, low WE#, LB# or UB# = low.
2. During a WE# controlled write cycle with OE# low, t_{WP} must be greater than $t_{WHZ} + t_{DW}$ to allow the drivers to turn off and data to be placed on the bus.
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the CE#, LB#, UB# low transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
5. t_{OW} and t_{WHZ} are specified with $C_L = 5\text{pF}$. Transition is measured $\pm 500\text{mV}$ from steady state.



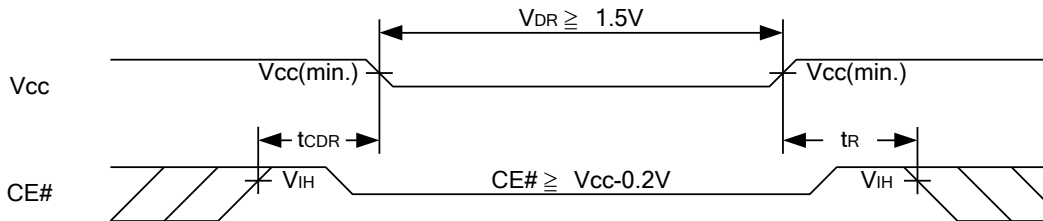
DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
V _{CC} for Data Retention	V _{DR}	CE# ≥ V _{CC} - 0.2V	1.5	-	5.5	V	
Data Retention Current	I _{DR}	V _{CC} = 1.5V, CE# ≥ V _{CC} - 0.2V Others at 0.2V or V _{CC} -0.2V	LL/LLI	-	0.5	20	μA
			SL 25°C	-	0.5	4	μA
			SLI 40°C	-	0.5	4	μA
			SL/SLI	-	0.5	15	μA
Chip Disable to Data Retention Time	t _{CDR}	See Data Retention Waveforms (below)	0	-	-	ns	
Recovery Time	t _R		t _{RC} *	-	-	ns	

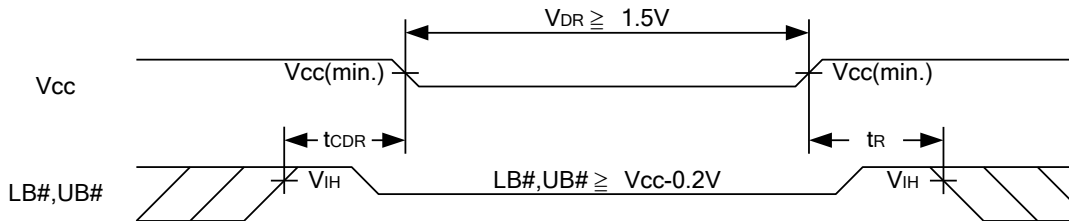
t_{RC}* = Read Cycle Time

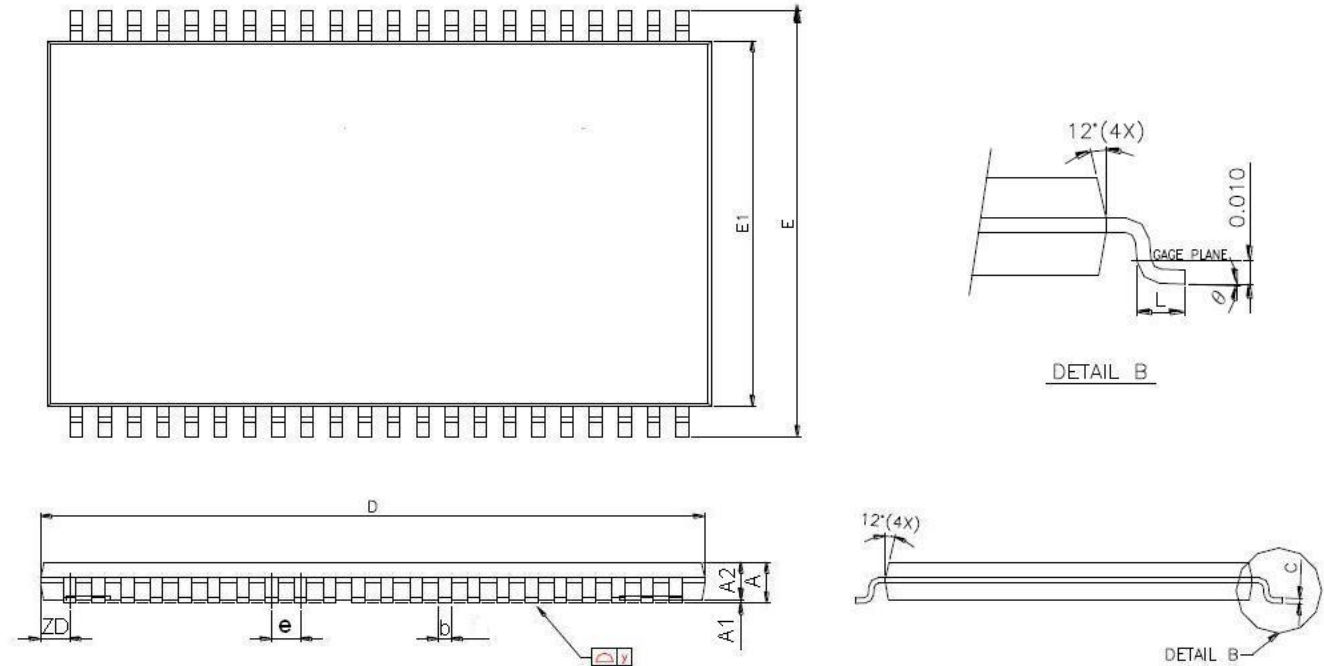
DATA RETENTION WAVEFORM

Low V_{CC} Data Retention Waveform (1) (CE# controlled)



Low V_{CC} Data Retention Waveform (2) (LB#, UB# controlled)

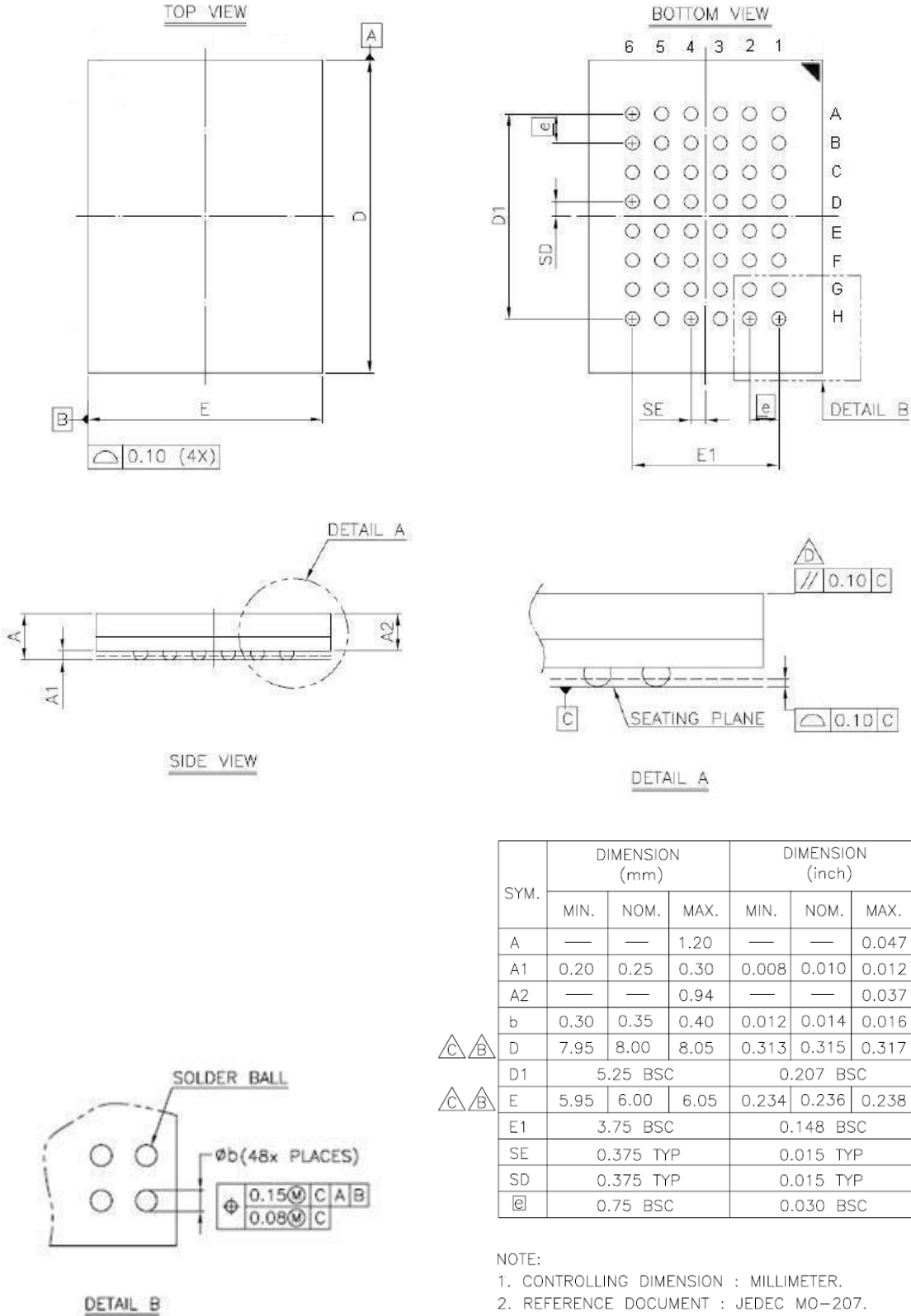


PACKAGE OUTLINE DIMENSION
44-pin 400 mil TSOP II Package Outline Dimension


SYMBOLS	DIMENSIONS IN MILLMETERS			DIMENSIONS IN MILS		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	-	-	1.20	-	-	47.2
A1	0.05	0.10	0.15	2.0	3.9	5.9
A2	0.95	1.00	1.05	37.4	39.4	41.3
b	0.30	-	0.45	11.8	-	17.7
c	0.12	-	0.21	4.7	-	8.3
D	18.212	18.415	18.618	717	725	733
E	11.506	11.760	12.014	453	463	473
E1	9.957	10.160	10.363	392	400	408
e	-	0.800	-	-	31.5	-
L	0.40	0.50	0.60	15.7	19.7	23.6
ZD	-	0.805	-	-	31.7	-
y	-	-	0.076	-	-	3
θ	0°	3°	6°	0°	3°	6°



48-ball 6mm x 8mm TFBGA Package Outline Dimension



NOTE:
 1. CONTROLLING DIMENSION : MILLIMETER.
 2. REFERENCE DOCUMENT : JEDEC MO-207.



ORDERING INFORMATION

Package Type	Access Time (Speed)(ns)	Power Type	Temperature Range(°C)	Packing Type	Lyontek Item No.
44-pin (400mil) TSOP II	55	Special	0°C ~70°C	Tray	LY62W12816ML-55SL
				Tape Reel	LY62W12816ML-55SLT
		Ultra Low Power	-40°C ~85°C	Tray	LY62W12816ML-55SLI
				Tape Reel	LY62W12816ML-55SLIT
		Ultra Low Power	0°C ~70°C	Tray	LY62W12816ML-55LL
				Tape Reel	LY62W12816ML-55LLT
	Ultra Low Power	-40°C ~85°C	Tray	LY62W12816ML-55LLI	
			Tape Reel	LY62W12816ML-55LLIT	
	70	Special	0°C ~70°C	Tray	LY62W12816ML-70SL
				Tape Reel	LY62W12816ML-70SLT
		Ultra Low Power	-40°C ~85°C	Tray	LY62W12816ML-70SLI
				Tape Reel	LY62W12816ML-70SLIT
Ultra Low Power		0°C ~70°C	Tray	LY62W12816ML-70LL	
			Tape Reel	LY62W12816ML-70LLT	
Ultra Low Power	-40°C ~85°C	Tray	LY62W12816ML-70LLI		
		Tape Reel	LY62W12816ML-70LLIT		



ORDERING INFORMATION

Package Type	Access Time (Speed)(ns)	Power Type	Temperature Range(°C)	Packing Type	Lyontek Item No.
48-ball (6mm x 8mm) TFBGA	55	Special Ultra Low Power	0°C ~70°C	Tray	LY62W12816GL-55SL
				Tape Reel	LY62W12816GL-55SLT
			-40°C ~85°C	Tray	LY62W12816GL-55SLI
				Tape Reel	LY62W12816GL-55SLIT
		Ultra Low Power	0°C ~70°C	Tray	LY62W12816GL-55LL
				Tape Reel	LY62W12816GL-55LLT
			-40°C ~85°C	Tray	LY62W12816GL-55LLI
				Tape Reel	LY62W12816GL-55LLIT
	70	Special Ultra Low Power	0°C ~70°C	Tray	LY62W12816GL-70SL
				Tape Reel	LY62W12816GL-70SLT
			-40°C ~85°C	Tray	LY62W12816GL-70SLI
				Tape Reel	LY62W12816GL-70SLIT
		Ultra Low Power	0°C ~70°C	Tray	LY62W12816GL-70LL
				Tape Reel	LY62W12816GL-70LLT
			-40°C ~85°C	Tray	LY62W12816GL-70LLI
				Tape Reel	LY62W12816GL-70LLIT



Lyontek Inc.

LY62W12816

Rev. 1.6

128K X 16 BIT LOW POWER CMOS SRAM

THIS PAGE IS LEFT BLANK INTENTIONALLY.