REVISION HISTORY

Revision	Description	Issue Date
Rev. 1.0	Initial Issue	Oct.14.2007
Rev. 1.1	Added I_{SB} Spec.	Feb.1.2008
Rev. 1.2	Revised I_{CC1}/I_{SB1}/V_{DR}/I_{DR} Spec. Revised typos in Page 1(I_{CC} TYP.)	Mar.2.2009
Rev. 1.3	Revised **FEATURES** & **ORDERING INFORMATION** **Lead free and green package available** to **Green package available** Added packing type in **ORDERING INFORMATION** Deleted T_{SOLDER} in **ABSOLUTE MAXIMUN RATINGS** Revised **PACKAGE OUTLINE DIMENSION** in page 10 Revised V_{IH} to 0.7*Vcc	May.7.2010
Rev. 1.4	Revised **ORDERING INFORMATION** in page 11	Aug.25.2010
Rev. 1.5	Deleted E grade Added SL grade Revised V_{IH} in page 3	Apr.25.2011
Rev. 1.6	Revised **TEST CONDITION** of V_{IH} in page 3	May.13.2011
Rev. 1.7	Revised **PACKAGE OUTLINE DIMENSION** in page 10	Jul.27.2011
Rev. 1.8	Deleted **WRITE CYCLE** Notes : 1.WE#,CE#, LB#, UB# must be high during all address transitions. In page 7	Jun.29.2016

LY62W51216

Rev. 1.8

512K X 16 BIT LOW POWER CMOS SRAM

FEATURES

- Fast access time : 55/70ns
- Low power consumption:
  Operating current : 30/20mA (TYP.)
  Standby current : 6μA (TYP.) LL-version
  3μA (TYP.) SL-version
- Single 2.7V ~ 5.5V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data byte control : LB# (DQ0 ~ DQ7)
  UB# (DQ8 ~ DQ15)
- Data retention voltage : 1.5V (MIN.)
- **Green package available**
- Package : 44-pin 400 mil TSOP-II
  48-ball 6mm x 8mm TFBGA

GENERAL DESCRIPTION

The LY62W51216 is a 8,388,608-bit low power CMOS static random access memory organized as 524,288 words by 16 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

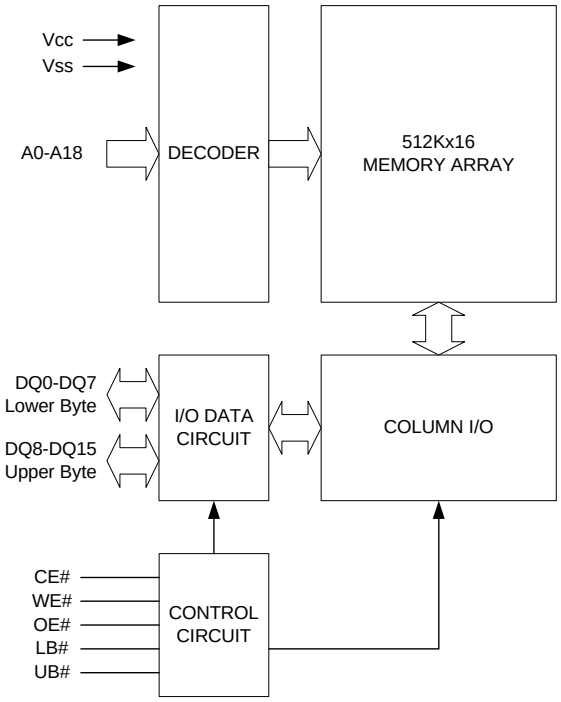
The LY62W51216 is well designed for low power application, and particularly well suited for battery back-up nonvolatile memory application.

The LY62W51216 operates from a single power supply of 2.7V ~ 5.5V and all inputs and outputs are fully TTL compatible

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation	
				Standby(I_{SB1},TYP.)	Operating(Icc,TYP.)
LY62W51216	0 ~ 70℃	2.7 ~ 5.5V	55/70ns	6μA(LL)/3μA(SL)	30/20mA
LY62W51216(I)	-40 ~ 85℃	2.7 ~ 5.5V	55/70ns	6μA(LL)/3μA(SL)	30/20mA

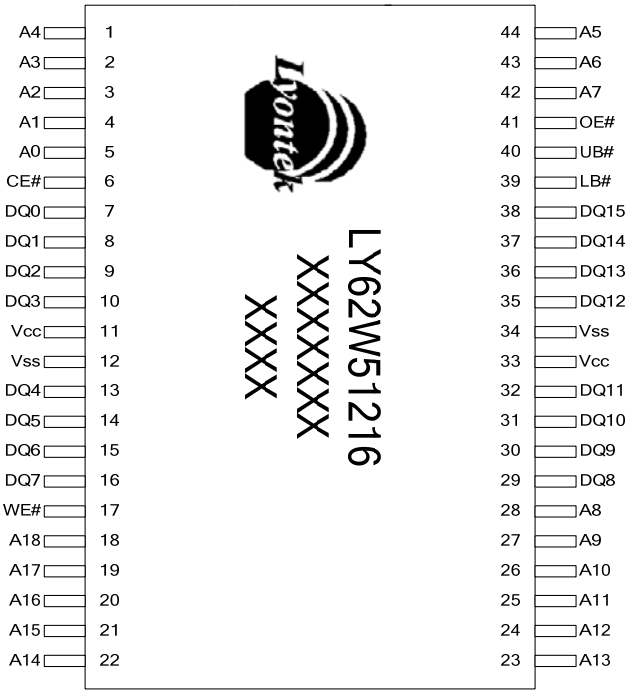
FUNCTIONAL BLOCK DIAGRAM



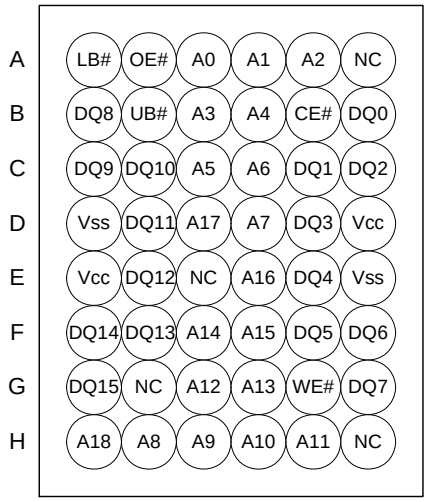
PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A18	Address Inputs
DQ0 – DQ15	Data Inputs/Outputs
CE#	Chip Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
LB#	Lower Byte Control
UB#	Upper Byte Control
V_{CC}	Power Supply
V_{SS}	Ground

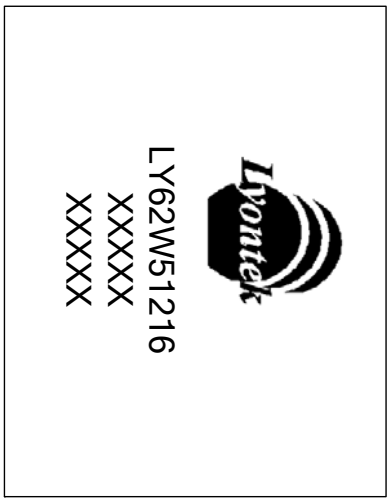
PIN CONFIGURATION



TSOP II



TFBGA



TFBGA(Top View)

ABSOLUTE MAXIMUN RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on V_{CC} relative to V_{SS}	V_{T1}	-0.5 to 6.5	V
Voltage on any other pin relative to V_{SS}	V_{T2}	-0.5 to V_{CC}+0.5	V
Operating Temperature	T_A	0 to 70(C grade) -40 to 85(I grade)	℃
Storage Temperature	T_{STG}	-65 to 150	℃
Power Dissipation	P_D	1	W
DC Output Current	I_{OUT}	50	mA

*Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE#	OE#	WE#	LB#	UB#	I/O OPERATION		SUPPLY CURRENT
						DQ0-DQ7	DQ8-DQ15	
Standby	H	X	X	X	X	High – Z	High – Z	I_{SB},I_{SB1}
	X	X	X	H	H	High – Z	High – Z	
Output Disable	L	H	H	L	X	High – Z	High – Z	I_{CC},I_{CC1}
	L	H	H	X	L	High – Z	High – Z	
Read	L	L	H	L	H	D_{OUT}	High – Z	I_{CC},I_{CC1}
	L	L	H	H	L	High – Z	D_{OUT}	
	L	L	H	L	L	D_{OUT}	D_{OUT}	
Write	L	X	L	L	H	D_{IN}	High – Z	I_{CC},I_{CC1}
	L	X	L	H	L	High – Z	D_{IN}	
	L	X	L	L	L	D_{IN}	D_{IN}	

Note: H = V_{IH}, L = V_{IL}, X = Don't care.

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP. *4	MAX.	UNIT
Supply Voltage	V_{CC}			2.7	3.0	5.5	V
Input High Voltage	V_{IH} *1	V_{CC} = 2.7 ~ 3.6V		2.2	-	V_{CC}+0.5	V
		V_{CC} = 4.5 ~ 5.5V		2.4	-	V_{CC}+0.5	V
Input Low Voltage	V_{IL} *2			- 0.2	-	0.6	V
Input Leakage Current	I_{LI}	$V_{CC} \geqq V_{IN} \geqq V_{SS}$		- 1	-	1	µA
Output Leakage Current	I_{LO}	$V_{CC} \geqq V_{OUT} \geqq V_{SS}$, Output Disabled		- 1	-	1	µA
Output High Voltage	V_{OH}	I_{OH} = -1mA		2.4	2.7	-	V
Output Low Voltage	V_{OL}	I_{OL} = 2mA		-	-	0.4	V
Average Operating Power supply Current	I_{CC}	Cycle time = Min. CE# = V_{IL} , $I_{I/O}$ = 0mA Other pins at V_{IL} or V_{IH}	- 55	-	30	60	mA
			- 70	-	20	50	mA
	I_{CC1}	Cycle time = 1µs CE# = 0.2V , $I_{I/O}$ = 0mA Other pins at 0.2V or V_{CC} - 0.2V		-	4	12	mA
Standby Power Supply Current	I_{SB}	CE# = V_{IH}, Other pins at V_{IL} or V_{IH}		-	0.15	2	mA
	I_{SB1}	CE# $\geqq V_{CC}$ - 0.2V Others at 0.2V or V_{CC} - 0.2V	LL	-	6	30	µA
			LLI	-	6	50	µA
			SL *5 25℃	-	3	10	µA
			SLI *5 40℃	-	3	10	µA
			SL	-	3	20	µA
			SLI	-	3	25	µA

Notes:
1. V_{IH}(max) = V_{CC} + 3.0V for pulse width less than 10ns.
2. V_{IL}(min) = V_{SS} - 3.0V for pulse width less than 10ns.
3. Over/Undershoot specifications are characterized, not 100% tested.
4. Typical values are included for reference only and are not guaranteed or tested.
   Typical values are measured at V_{CC} = V_{CC}(TYP.) and T_A = 25℃
5. This parameter is measured at V_{CC} = 3.0V

CAPACITANCE (T_A = 25℃, f = 1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C_{IN}	-	6	pF
Input/Output Capacitance	$C_{I/O}$	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0.2V to V_{CC} - 0.2V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	C_L = 30pF + 1TTL, I_{OH}/I_{OL} = -1mA/2mA

AC ELECTRICAL CHARACTERISTICS

(1) READ CYCLE

PARAMETER	SYM.	LY62W51216-55		LY62W51216-70		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t_{RC}	55	-	70	-	ns
Address Access Time	t_{AA}	-	55	-	70	ns
Chip Enable Access Time	t_{ACE}	-	55	-	70	ns
Output Enable Access Time	t_{OE}	-	30	-	35	ns
Chip Enable to Output in Low-Z	t_{CLZ}*	10	-	10	-	ns
Output Enable to Output in Low-Z	t_{OLZ}*	5	-	5	-	ns
Chip Disable to Output in High-Z	t_{CHZ}*	-	20	-	25	ns
Output Disable to Output in High-Z	t_{OHZ}*	-	20	-	25	ns
Output Hold from Address Change	t_{OH}	10	-	10	-	ns
LB#, UB# Access Time	t_{BA}	-	55	-	70	ns
LB#, UB# to High-Z Output	t_{BHZ}*	-	25	-	30	ns
LB#, UB# to Low-Z Output	t_{BLZ}*	10	-	10	-	ns

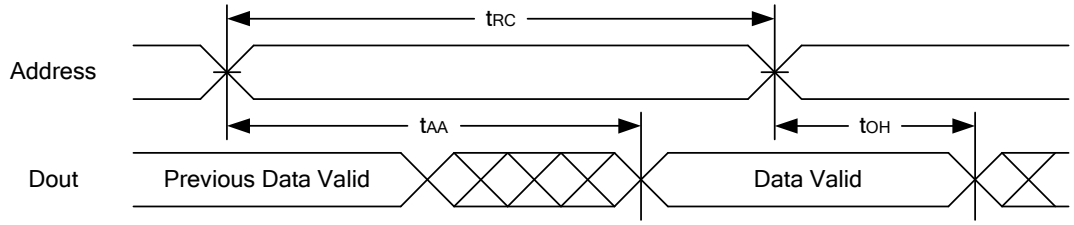
(2) WRITE CYCLE

PARAMETER	SYM.	LY62W51216-55		LY62W51216-70		UNIT
		MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t_{WC}	55	-	70	-	ns
Address Valid to End of Write	t_{AW}	50	-	60	-	ns
Chip Enable to End of Write	t_{CW}	50	-	60	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	ns
Write Pulse Width	t_{WP}	45	-	55	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	ns
Data to Write Time Overlap	t_{DW}	25	-	30	-	ns
Data Hold from End of Write Time	t_{DH}	0	-	0	-	ns
Output Active from End of Write	t_{OW}*	5	-	5	-	ns
Write to Output in High-Z	t_{WHZ}*	-	20	-	25	ns
LB#, UB# Valid to End of Write	t_{BW}	45	-	60	-	ns

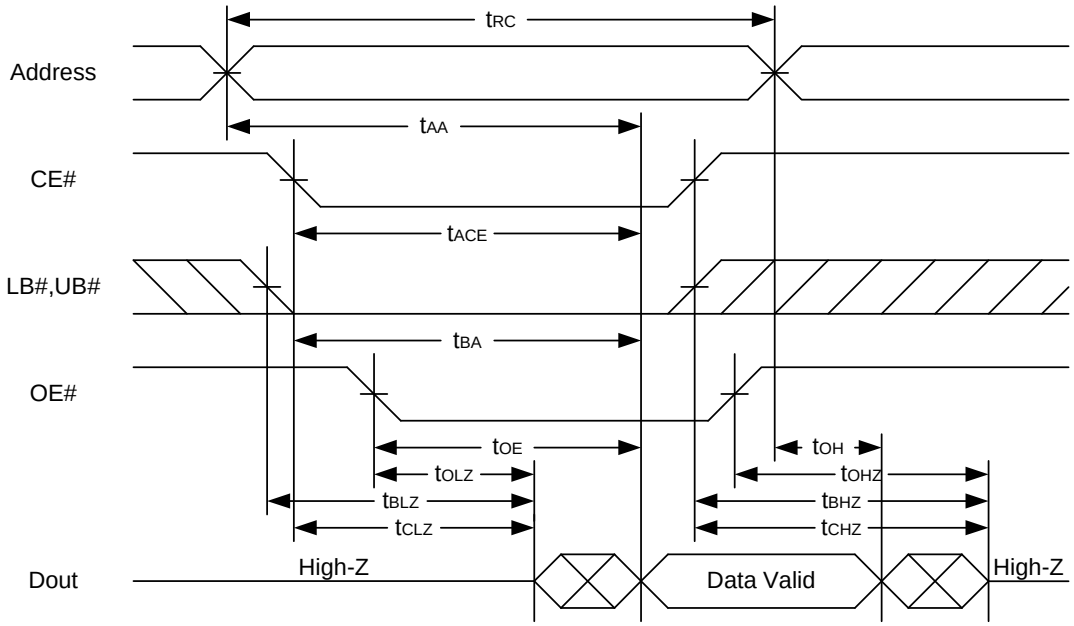
*These parameters are guaranteed by device characterization, but not production tested.

TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)

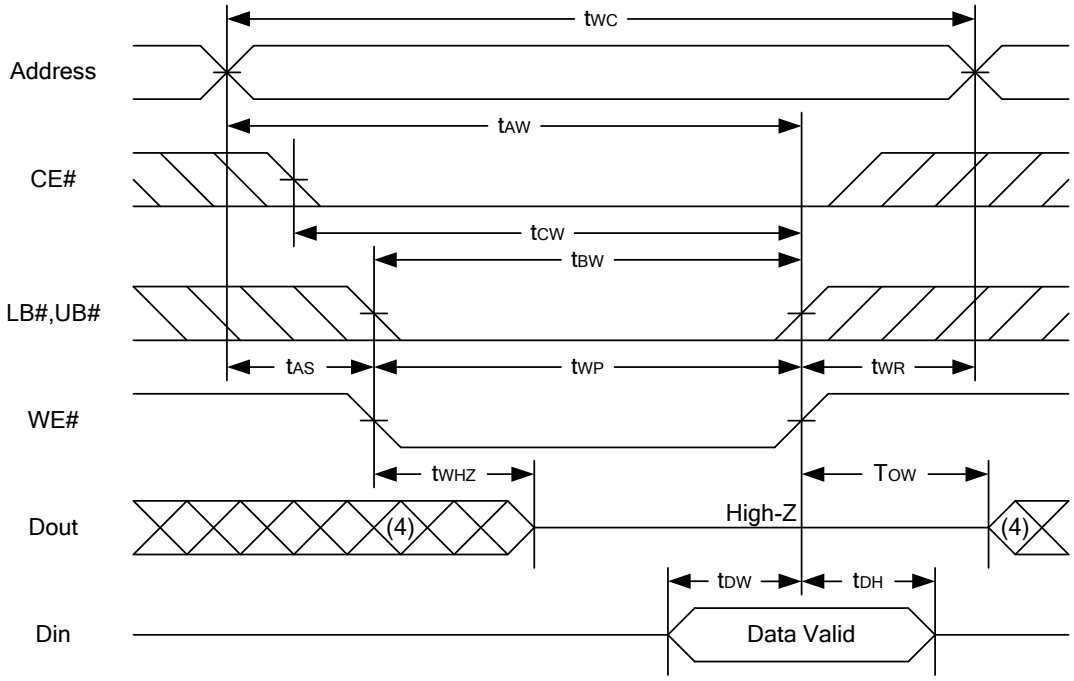


READ CYCLE 2 (CE# and OE# Controlled) (1,3,4,5)

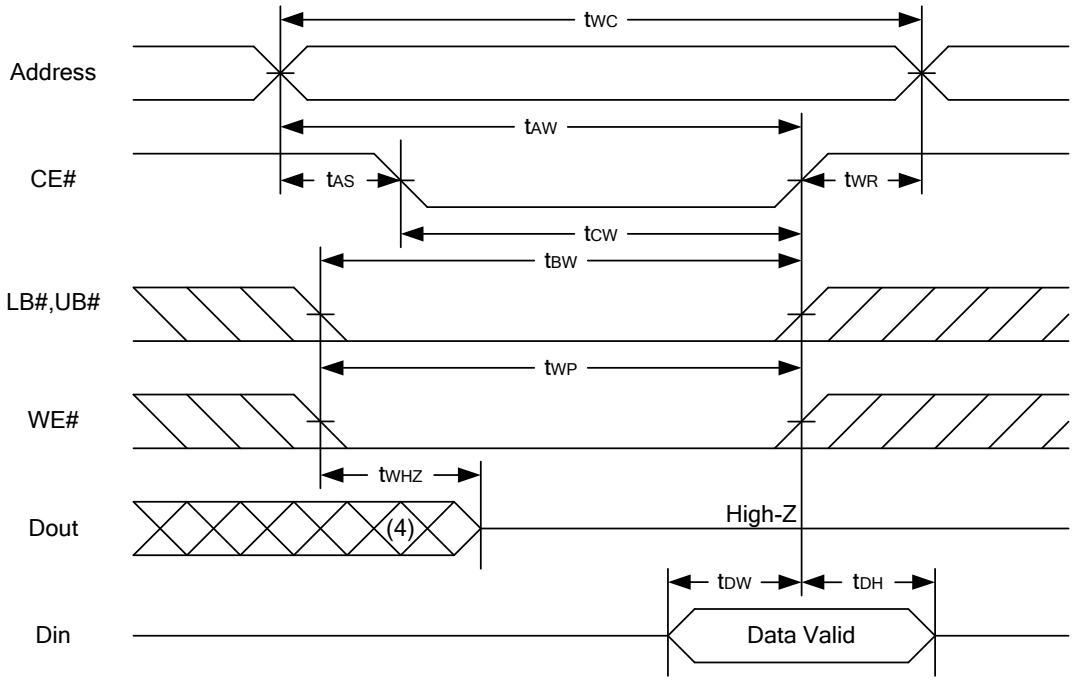


Notes :
1.WE#is high for read cycle.
2.Device is continuously selected OE# = low, CE# = low, LB# or UB# = low.
3.Address must be valid prior to or coincident with CE# = low, LB# or UB# = low transition; otherwise t_{AA} is the limiting parameter.
4.t_{CLZ}, t_{BLZ}, t_{OLZ}, t_{CHZ}, t_{BHZ} and t_{OHZ} are specified with C_L = 5pF. Transition is measured ±500mV from steady state.
5.At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{BHZ} is less than t_{BLZ}, t_{OHZ} is less than t_{OLZ}.

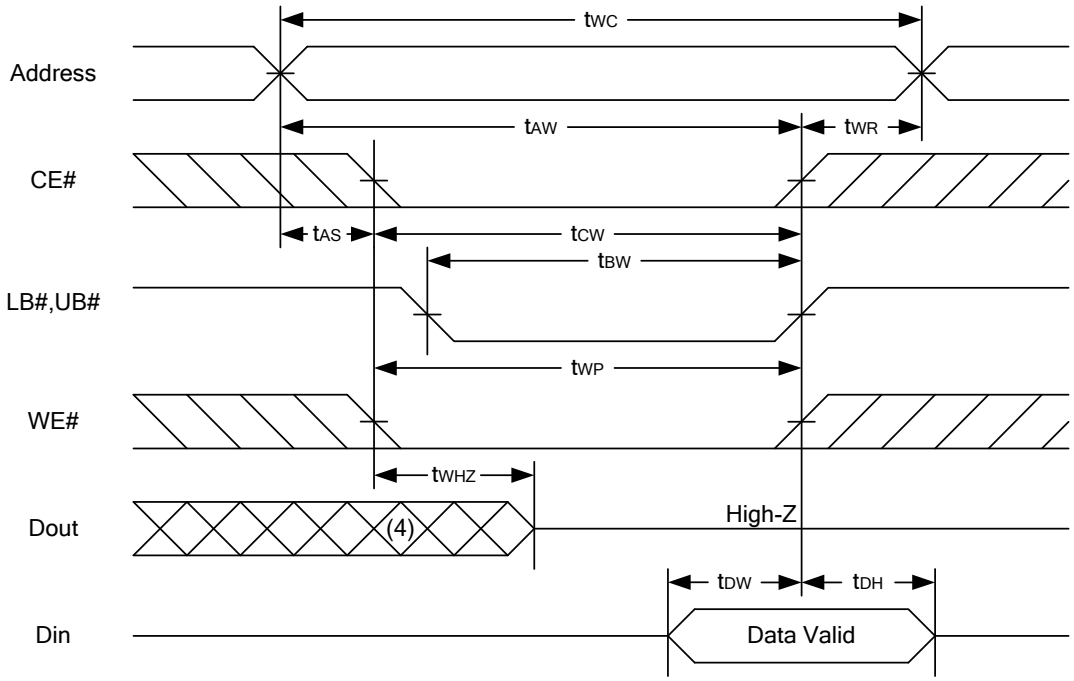
WRITE CYCLE 1 (WE# Controlled) (1,2,4,5)



WRITE CYCLE 2 (CE# Controlled) (1,4,5)



WRITE CYCLE 3 (LB#,UB# Controlled) (1,4,5)



Notes :
1.A write occurs during the overlap of a low CE#, low WE#, LB# or UB# = low.
2.During a WE# controlled write cycle with OE# low, t_{WP} must be greater than $t_{WHZ} + t_{DW}$ to allow the drivers to turn off and data to be placed on the bus.
3.During this period, I/O pins are in the output state, and input signals must not be applied.
4.If the CE#, LB#, UB# low transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
5.t_{OW} and t_{WHZ} are specified with C_L = 5pF. Transition is measured ±500mV from steady state.

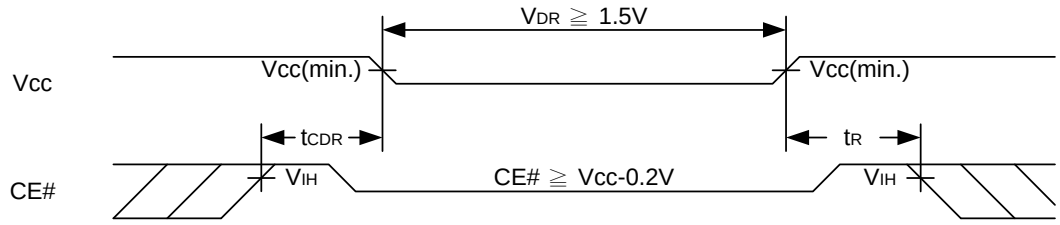
DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
V_{CC} for Data Retention	V_{DR}	CE# ≧ V_{CC} - 0.2V			1.5	-	5.5	V
Data Retention Current	I_{DR}	V_{CC} = 1.5V CE# ≧ V_{CC} - 0.2V Other pins at 0.2V or V_{CC}-0.2V	LL		-	4	30	µA
			LLI		-	4	50	µA
			SL	25℃	-	3	10	µA
			SLI	40℃	-	3	10	µA
			SL		-	3	20	µA
			SLI		-	3	25	µA
Chip Disable to Data Retention Time	t_{CDR}	See Data Retention Waveforms (below)			0	-	-	ns
Recovery Time	t_R				t_{RC*}	-	-	ns

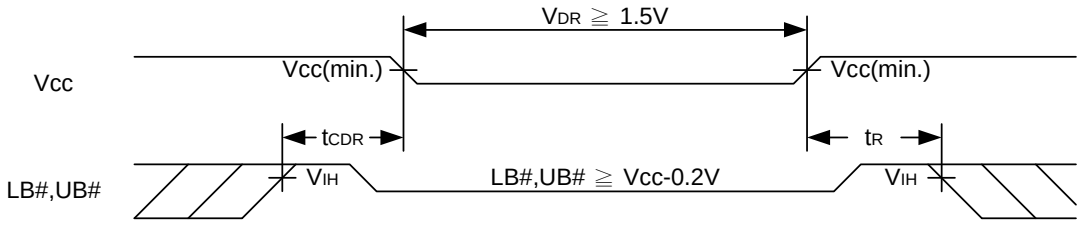
t_{RC*} = Read Cycle Time

DATA RETENTION WAVEFORM

Low Vcc Data Retention Waveform (1) (CE# controlled)

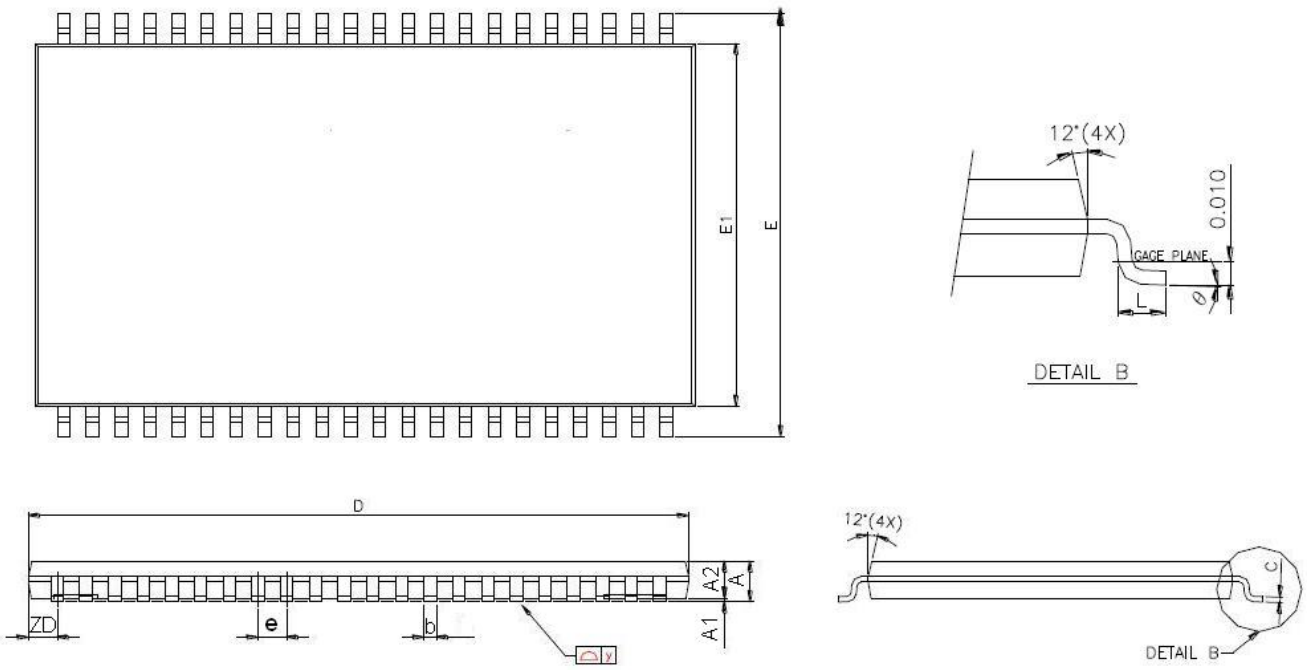


Low Vcc Data Retention Waveform (2) (LB#, UB# controlled)



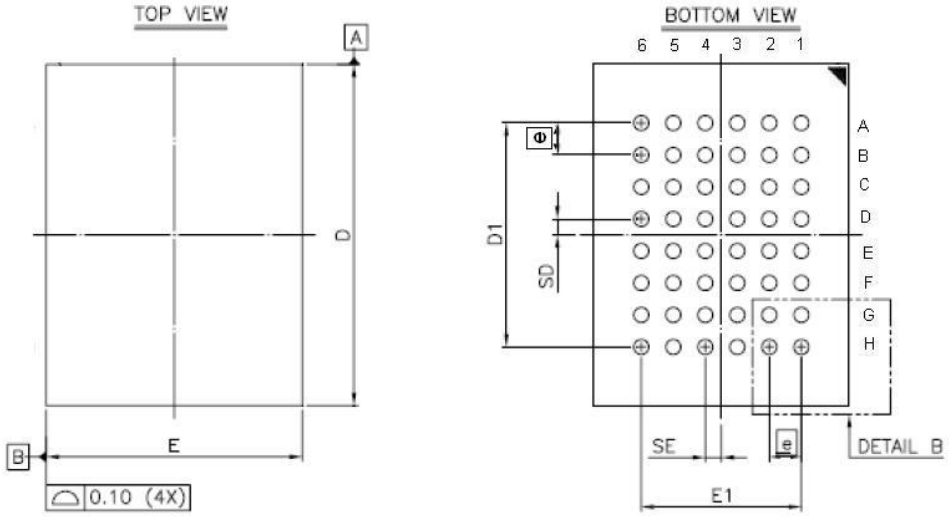
PACKAGE OUTLINE DIMENSION

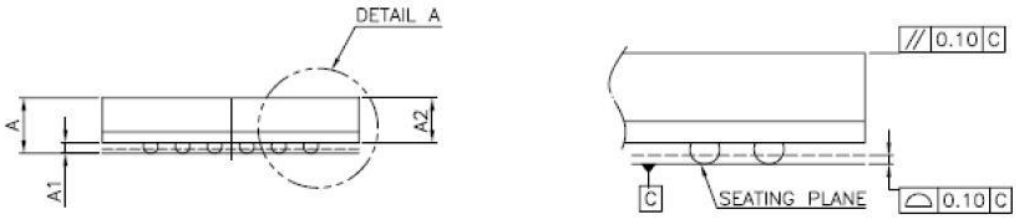
44-pin 400mil TSOP-Ⅱ Package Outline Dimension

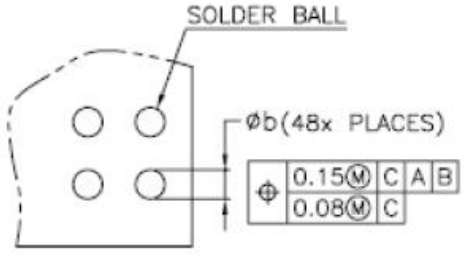


SYMBOLS	DIMENSIONS IN MILLMETERS			DIMENSIONS IN MILS		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	-	-	1.20	-	-	47.2
A1	0.05	0.10	0.15	2.0	3.9	5.9
A2	0.95	1.00	1.05	37.4	39.4	41.3
b	0.30	-	0.45	11.8	-	17.7
c	0.12	-	0.21	4.7	-	8.3
D	18.212	18.415	18.618	717	725	733
E	11.506	11.760	12.014	453	463	473
E1	9.957	10.160	10.363	392	400	408
e	-	0.800	-	-	31.5	-
L	0.40	0.50	0.60	15.7	19.7	23.6
ZD	-	0.805	-	-	31.7	-
y	-	-	0.076	-	-	3
θ	0^o	3^o	6^o	0^o	3^o	6^o

48-ball 6mm × 8mm TFBGA Package Outline Dimension







SYM.	DIMENSION (mm)			DIMENSION (inch)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.40	—	—	0.055
A1	0.20	0.25	0.30	0.008	0.010	0.012
A2	—	—	1.05	—	—	0.041
b	0.30	0.35	0.40	0.012	0.014	0.016
D	7.95	8.00	8.05	0.313	0.315	0.317
D1	5.25 BSC			0.207 BSC		
E	5.95	6.00	6.05	0.234	0.236	0.238
E1	3.75 BSC			0.148 BSC		
SE	0.375 TYP			0.015 TYP		
SD	0.375 TYP			0.015 TYP		
e	0.75 BSC			0.030 BSC		

NOTE:
1. CONTROLLING DIMENSION : MILLIMETER.
2. REFERENCE DOCUMENT : JEDEC MO-207.

ORDERING INFORMATION

Package Type	Access Time (Speed/ns)	Power Type	Temperature Range(℃)	Packing Type	Lyontek Item No.
44Pin 400mil TSOP-II	55	Special Ultra Low Power	0℃~70℃	Tray	LY62W51216ML-55SL
				Tape Reel	LY62W51216ML-55SLT
			-40℃~85℃	Tray	LY62W51216ML-55SLI
				Tape Reel	LY62W51216ML-55SLIT
		Ultra Low Power	0℃~70℃	Tray	LY62W51216ML-55LL
				Tape Reel	LY62W51216ML-55LLT
			-40℃~85℃	Tray	LY62W51216ML-55LLI
				Tape Reel	LY62W51216ML-55LLIT
	70	Special Ultra Low Power	0℃~70℃	Tray	LY62W51216ML-70SL
				Tape Reel	LY62W51216ML-70SLT
			-40℃~85℃	Tray	LY62W51216ML-70SLI
				Tape Reel	LY62W51216ML-70SLIT
		Ultra Low Power	0℃~70℃	Tray	LY62W51216ML-70LL
				Tape Reel	LY62W51216ML-70LLT
			-40℃~85℃	Tray	LY62W51216ML-70LLI
				Tape Reel	LY62W51216ML-70LLIT

ORDERING INFORMATION

Package Type	Access Time (Speed/ns)	Power Type	Temperature Range(℃)	Packing Type	Lyontek Item No.
48-Ball 6mm x 8mm TFBGA	55	Special Ultra Low Power	0℃~70℃	Tray	LY62W51216GL-55SL
				Tape Reel	LY62W51216GL-55SLT
			-40℃~85℃	Tray	LY62W51216GL-55SLI
				Tape Reel	LY62W51216GL-55SLIT
		Ultra Low Power	0℃~70℃	Tray	LY62W51216GL-55LL
				Tape Reel	LY62W51216GL-55LLT
			-40℃~85℃	Tray	LY62W51216GL-55LLI
				Tape Reel	LY62W51216GL-55LLIT
	70	Special Ultra Low Power	0℃~70℃	Tray	LY62W51216GL-70SL
				Tape Reel	LY62W51216GL-70SLT
			-40℃~85℃	Tray	LY62W51216GL-70SLI
				Tape Reel	LY62W51216GL-70SLIT
		Ultra Low Power	0℃~70℃	Tray	LY62W51216GL-70LL
				Tape Reel	LY62W51216GL-70LLT
			-40℃~85℃	Tray	LY62W51216GL-70LLI
				Tape Reel	LY62W51216GL-70LLIT

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