



REVISION HISTORY

<u>Revision</u>	<u>Description</u>	<u>Issue Date</u>
Rev. 1.0	Initial Issue	Jul.25.2004
Rev. 1.1	Delete I _{CC1} Spec.	Sep.21.2004
Rev. 1.2	Add E/I grade	Apr.07.2005
Rev. 1.3	Revised V _{TERM} to V _{T1} and V _{T2} Revised TEST CONDITION of I _{SB1} /I _{DR} Added LL Spec.	Feb.02.2009
Rev. 1.4	Revised TEST CONDITION of I _{CC} /I _{SB} Revised FEATURES & ORDERING INFORMATION <u>Lead free and green package available</u> to <u>Green package available</u> Deleted TSOLDER in ABSOLUTE MAXIMUM RATINGS Added packing type in ORDERING INFORMATION	Apr.17.2009
Rev. 1.5	Revised PACKAGE OUTLINE DIMENSION in page 9/10	May.07.2010
Rev. 1.6	Revised ORDERING INFORMATION in page 11	Aug.30.2010
Rev. 1.7	Deleted WRITE CYCLE Notes : 1. WE#, CE# must be high or CE2 must be low during all address transitions. In page 6.	Jan.17.2016
Rev. 1.8	Revised Typo error of PACKAGE OUTLINE DIMENSION : 32 pin 8mm x 20mm TSOP I L1 in page 9	Aug.11.2025

FEATURES

- Fast access time : 12/15ns
- Low power consumption:
Operating current : 50/40mA (TYP.)
Standby current : 1mA (TYP.)
2μA (TYP.) LL -version
- Single 4.5V ~ 5.5V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data retention voltage : 2.0V (MIN.)
- **Green package available**
- Package : 32-pin 300mil SOJ
32-pin 8mm x 20mm TSOP I
32-pin 8mm x 13.4mm sTSOP

GENERAL DESCRIPTION

The LY611024 is a 1,048,576-bit low power CMOS static random access memory organized as 131,072 words by 8 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

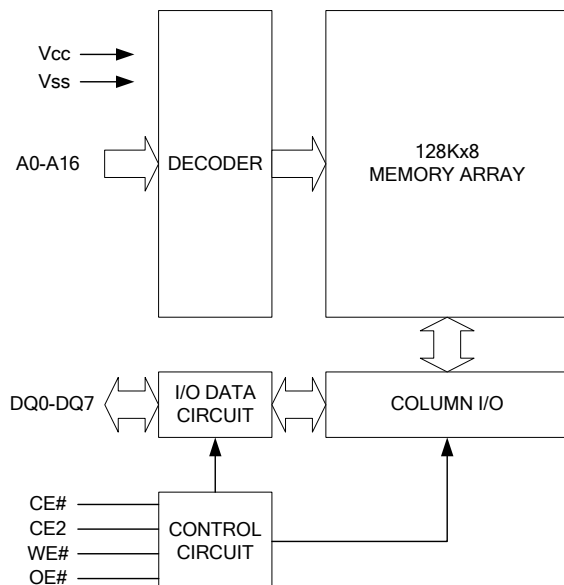
The LY611024 is well designed for very high speed system applications, and particularly well suited for battery back-up nonvolatile memory application.

The LY611024 operates from a single power supply of 4.5V ~ 5.5V and all inputs and outputs are fully TTL compatible

PRODUCT FAMILY

Product Family	Operating Temperature	V _{CC} Range	Speed	Power Dissipation	
				Standby(I _{SB1} , TYP.)	Operating(I _{CC} , TYP.)
LY611024	0 ~ 70°C	4.5 ~ 5.5V	12/15ns	1mA	50/40mA
LY611024(E)	-20 ~ 80°C	4.5 ~ 5.5V	12/15ns	1mA	50/40mA
LY611024(I)	-40 ~ 85°C	4.5 ~ 5.5V	12/15ns	1mA	50/40mA
LY611024(LL)	0 ~ 70°C	4.5 ~ 5.5V	12/15ns	2μA	50/40mA
LY611024(LLE)	-20 ~ 80°C	4.5 ~ 5.5V	12/15ns	2μA	50/40mA
LY611024(LLI)	-40 ~ 85°C	4.5 ~ 5.5V	12/15ns	2μA	50/40mA

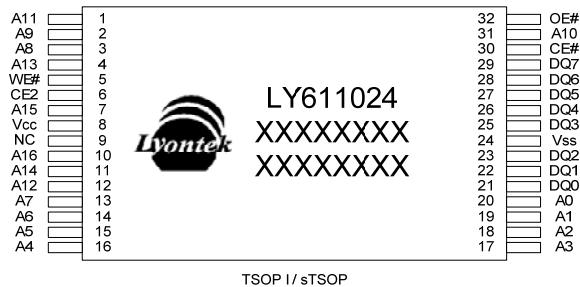
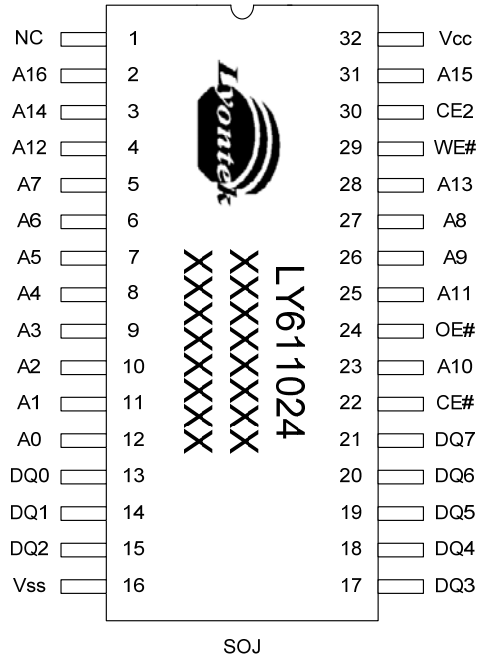
FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A16	Address Inputs
DQ0 - DQ7	Data Inputs/Outputs
CE#, CE2	Chip Enable Inputs
WE#	Write Enable Input
OE#	Output Enable Input
V _{CC}	Power Supply
V _{SS}	Ground
NC	No Connection

PIN CONFIGURATION



ABSOLUTE MAXIMUN RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on V _{CC} relative to V _{SS}	V _{T1}	-0.5 to 6.5	V
Voltage on any other pin relative to V _{SS}	V _{T2}	-0.5 to V _{CC} +0.5	V
Operating Temperature	T _A	0 to 70(C grade)	°C
		-20 to 80(E grade)	
		-40 to 85(I grade)	
Storage Temperature	T _{STG}	-65 to 150	°C
Power Dissipation	P _D	1	W
DC Output Current	I _{OUT}	50	mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE#	CE2	OE#	WE#	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	X	High-Z	I _{SB} , I _{SB1}
	X	L	X	X	High-Z	I _{SB} , I _{SB1}
Output Disable	L	H	H	H	High-Z	I _{CC}
Read	L	H	L	H	D _{OUT}	I _{CC}
Write	L	H	X	L	D _{IN}	I _{CC}

Note: H = V_{IH}, L = V_{IL}, X = Don't care.

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP. ^{*4}	MAX.	UNIT
Supply Voltage	V _{CC}			4.5	5.0	5.5	V
Input High Voltage	V _{IH} ^{*1}			2.4	-	V _{CC} +0.5	V
Input Low Voltage	V _{IL} ^{*2}			- 0.5	-	0.8	V
Input Leakage Current	I _{LI}	V _{CC} ≥ V _{IN} ≥ V _{SS}		- 1	-	1	μA
Output Leakage Current	I _{LO}	V _{CC} ≥ V _{OUT} ≥ V _{SS} , Output Disabled		- 1	-	1	μA
Output High Voltage	V _{OH}	I _{OH} = -4mA		2.4	-	-	V
Output Low Voltage	V _{OL}	I _{OL} = 8mA		-	-	0.4	V
Average Operating Power supply Current	I _{CC}	Cycle time = MIN. CE# = V _{IL} and CE2 = V _{IH} , I _{I/O} = 0mA Others at V _{IL} or V _{IH}	- 12	-	50	80	mA
			- 15	-	40	65	mA
Standby Power Supply Current	I _{SB}	CE# = V _{IH} or CE2 = V _{IL} Others at V _{IL} or V _{IH}		-	3	20	mA
	I _{SB1}	CE# ≥ V _{CC} -0.2V or CE2 ≤ 0.2V	Normal	-	1	5	mA
		CE# ≥ V _{CC} -0.2V or CE2 ≤ 0.2V Others at 0.2V or V _{CC} -0.2V	LL	-	2	50	μA

Notes:

1. V_{IH}(max) = V_{CC} + 3.0V for pulse width less than 10ns.
2. V_{IL}(min) = V_{SS} - 3.0V for pulse width less than 10ns.
3. Over/Undershoot specifications are characterized, not 100% tested.
4. Typical values are included for reference only and are not guaranteed or tested.

Typical valued are measured at V_{CC} = V_{CC}(TYP.) and T_A = 25°C

CAPACITANCE (T_A = 25°C, f = 1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Input Capacitance	C _{IN}	-	6	pF
Input/Output Capacitance	C _{I/O}	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0.2V to V _{CC} - 0.2V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	C _L = 30pF + 1TTL, I _{OH} /I _{OL} = -4mA/8mA



AC ELECTRICAL CHARACTERISTICS

(1) READ CYCLE

PARAMETER	SYM.	LY611024-12		LY611024-15		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t _{RC}	12	-	15	-	ns
Address Access Time	t _{AA}	-	12	-	15	ns
Chip Enable Access Time	t _{ACE}	-	12	-	15	ns
Output Enable Access Time	t _{OE}	-	6	-	7	ns
Chip Enable to Output in Low-Z	t _{CLZ} *	3	-	4	-	ns
Output Enable to Output in Low-Z	t _{OLZ} *	0	-	0	-	ns
Chip Disable to Output in High-Z	t _{CHZ} *	-	6	-	7	ns
Output Disable to Output in High-Z	t _{OHZ} *	-	6	-	7	ns
Output Hold from Address Change	t _{OH}	3	-	3	-	ns

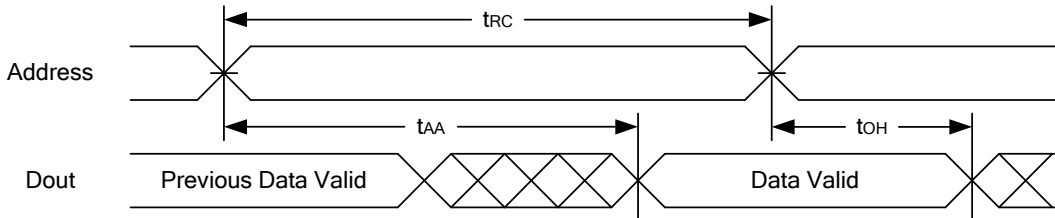
(2) WRITE CYCLE

PARAMETER	SYM.	LY611024-12		LY611024-15		UNIT
		MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t _{WC}	12	-	15	-	ns
Address Valid to End of Write	t _{AW}	10	-	12	-	ns
Chip Enable to End of Write	t _{CW}	10	-	12	-	ns
Address Set-up Time	t _{AS}	0	-	0	-	ns
Write Pulse Width	t _{WP}	9	-	10	-	ns
Write Recovery Time	t _{WR}	0	-	0	-	ns
Data to Write Time Overlap	t _{DW}	7	-	8	-	ns
Data Hold from End of Write Time	t _{DH}	0	-	0	-	ns
Output Active from End of Write	t _{OW} *	3	-	4	-	ns
Write to Output in High-Z	t _{WHZ} *	-	7	-	8	ns

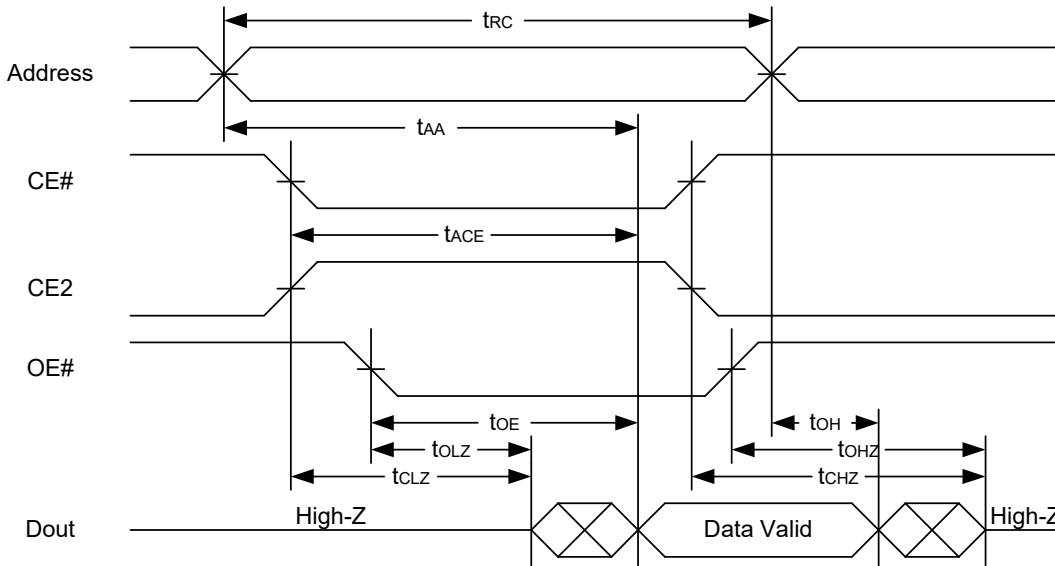
*These parameters are guaranteed by device characterization, but not production tested.

TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)



READ CYCLE 2 (CE# and CE2 and OE# Controlled) (1,3,4,5)

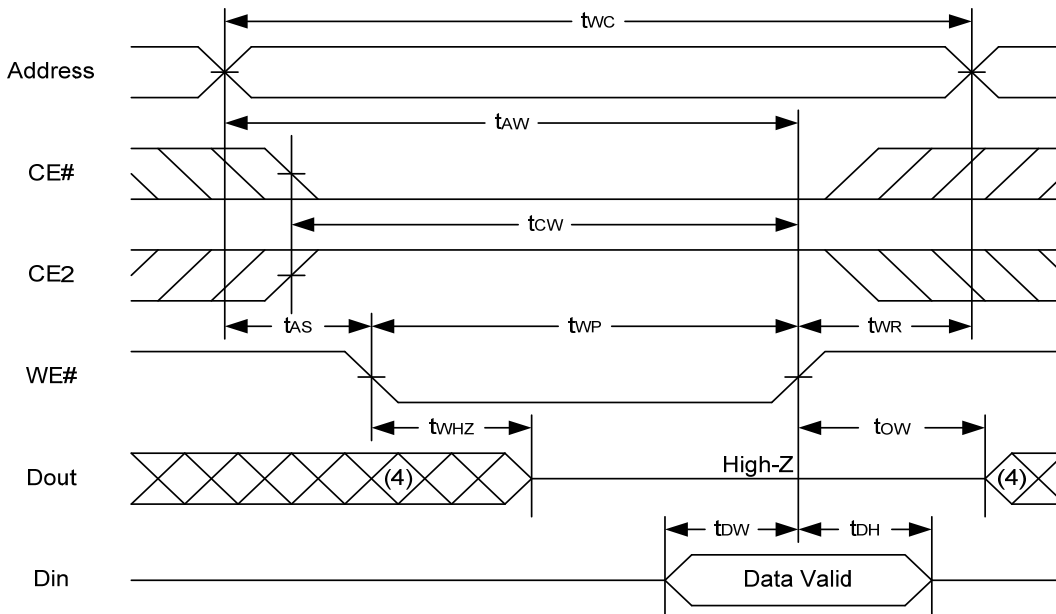


Notes :

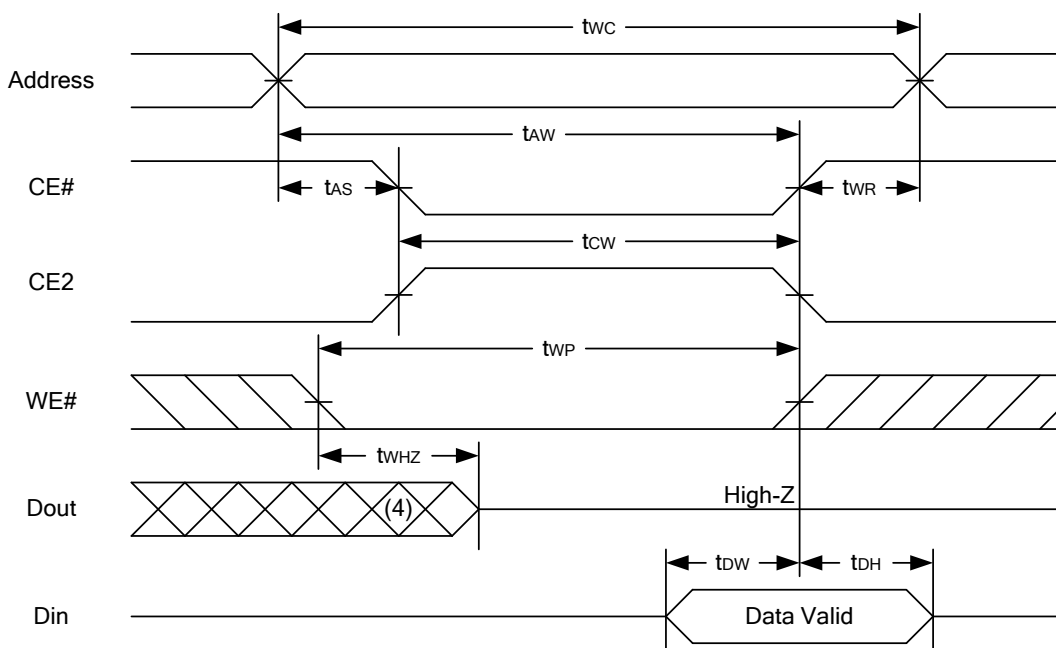
1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low, CE2 = high.
3. Address must be valid prior to or coincident with CE# = low, CE2 = high; otherwise t_{AA} is the limiting parameter.
4. t_{CLZ} , t_{OLZ} , t_{CHZ} and t_{OHZ} are specified with $C_L = 5\text{pF}$. Transition is measured $\pm 500\text{mV}$ from steady state.
5. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{OHZ} is less than t_{OLZ} .



WRITE CYCLE 1 (WE# Controlled) (1,2,4,5)



WRITE CYCLE 2 (CE# and CE2 Controlled) (1,4,5)



Notes :

1. A write occurs during the overlap of a low CE#, high CE2, low WE#.
2. During a WE# controlled write cycle with OE# low, t_{WP} must be greater than $t_{WHZ} + t_{DW}$ to allow the drivers to turn off and data to be placed on the bus.
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the CE# low transition and CE2 high transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
5. t_{OW} and t_{WHZ} are specified with $C_L = 5\text{pF}$. Transition is measured $\pm 500\text{mV}$ from steady state.



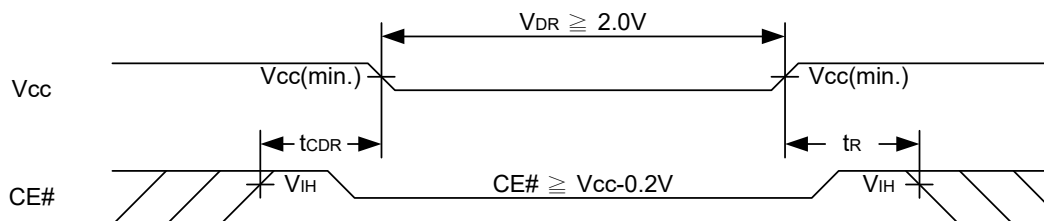
DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
V _{CC} for Data Retention	V _{DR}	CE# $\geq$ V _{CC} - 0.2V or CE2 $\leq$ 0.2V	2.0	-	5.5	V
Data Retention Current	I _{DR}	V _{CC} = 2.0V CE# $\geq$ V _{CC} - 0.2V or CE2 $\leq$ 0.2V Normal	-	0.01	3	mA
		V _{CC} = 2.0V CE# $\geq$ V _{CC} - 0.2V or CE2 $\leq$ 0.2V LL others at 0.2V or V _{CC} -0.2V	-	0.5	30	μ A
Chip Disable to Data Retention Time	t _{CDR}	See Data Retention Waveforms (below)	0	-	-	ns
Recovery Time	t _R		t _{RC} *	-	-	ns

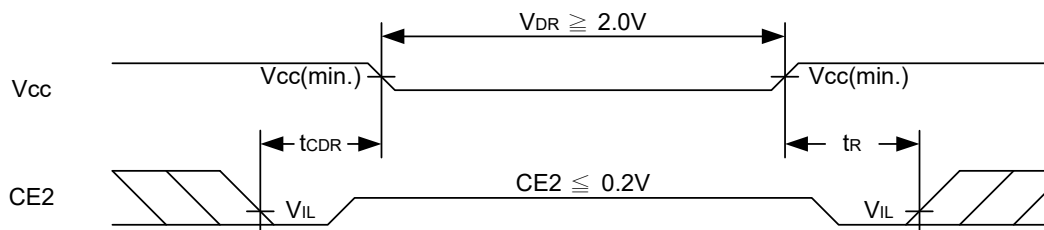
t_{RC}* = Read Cycle Time

DATA RETENTION WAVEFORM

Low V_{CC} Data Retention Waveform (1) (CE# controlled)



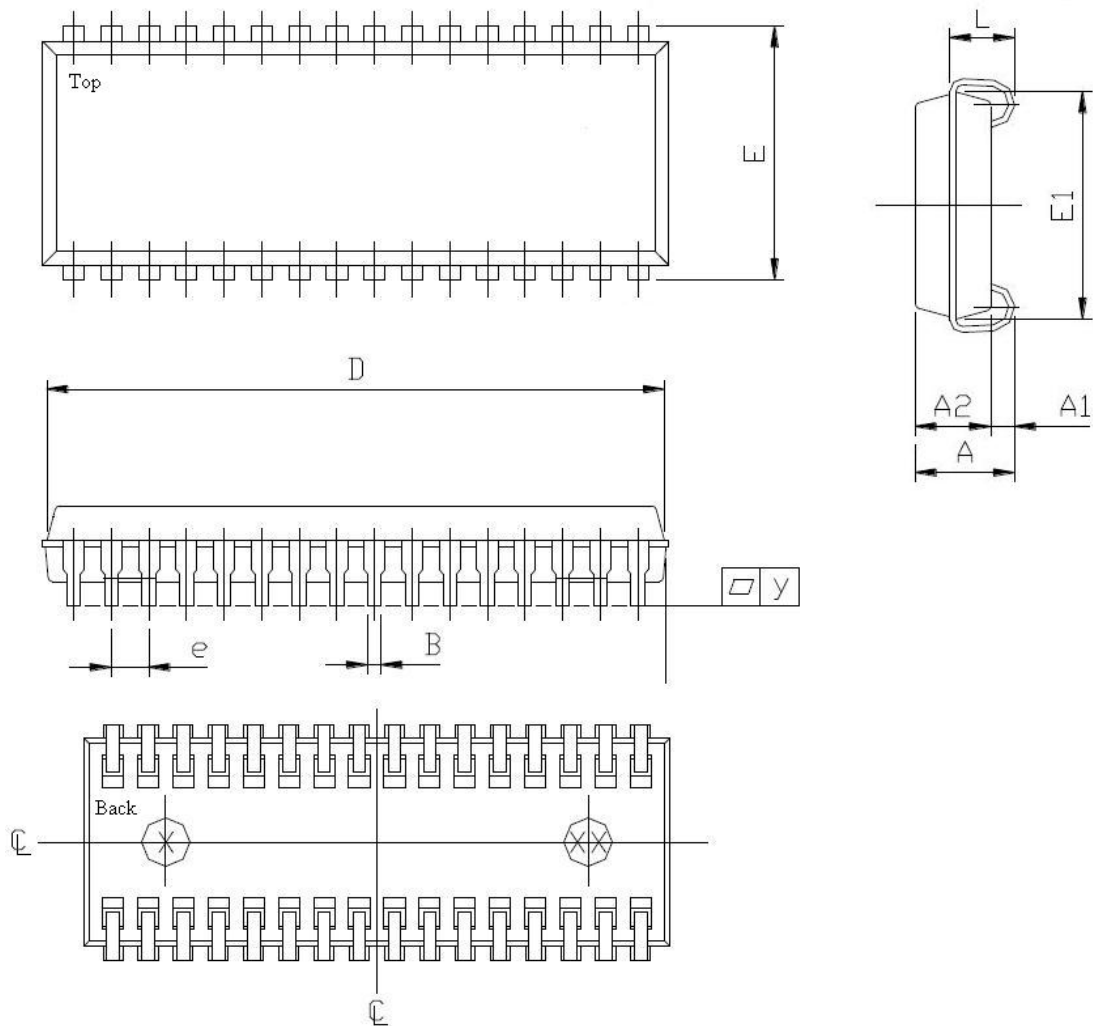
Low V_{CC} Data Retention Waveform (2) (CE2 controlled)





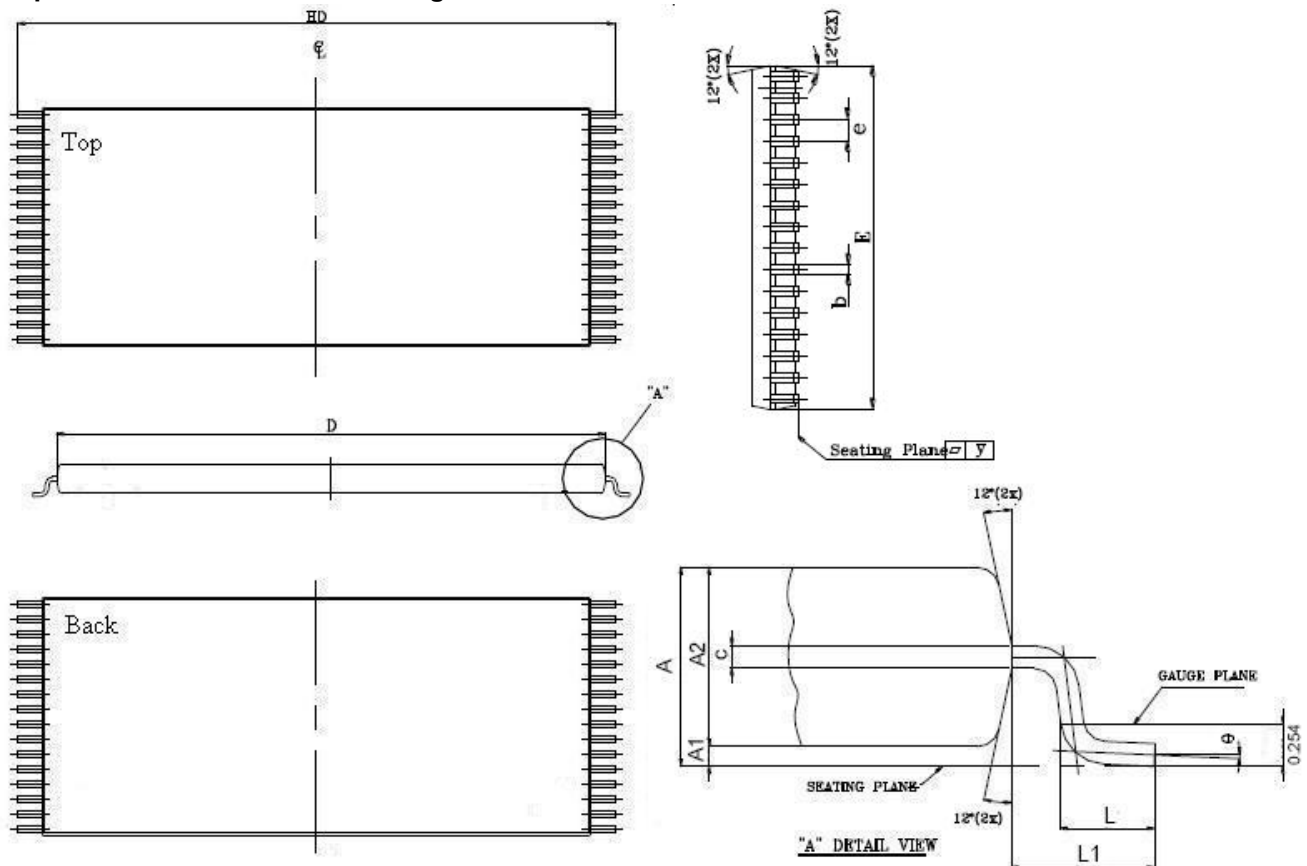
PACKAGE OUTLINE DIMENSION

32-pin 300mil SOJ Package Outline Dimension



SYMBOL	UNIT	INCH(BASE)	MM(REF)
A		0.148(MAX)	3.759(MAX)
A1		0.025(MIN)	0.635(MIN)
A2		0.123(MAX)	3.124(MAX)
B		0.018(TYP)	0.457(TYP)
D		0.825±0.005	20.955±0.127
E		0.335(TYP)	8.509(TYP)
E1		0.300±0.005	7.620±0.127
e		0.050(TYP)	1.270(TYP)
L		0.086±0.010	2.184±0.254
y		0.003(MAX)	0.076(MAX)

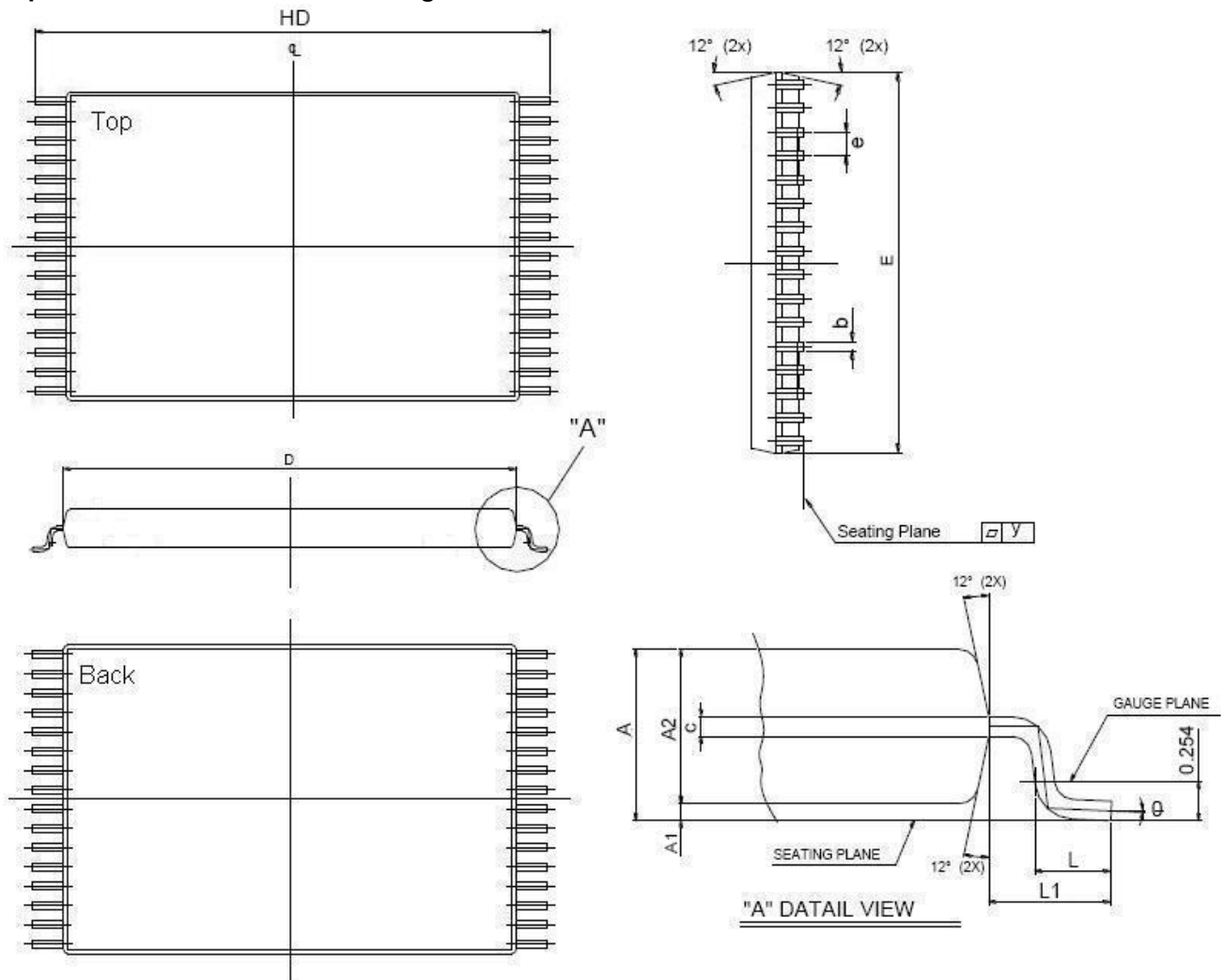
32-pin 8mm x 20mm TSOP I Package Outline Dimension



SYM.	UNIT	INCH(BASE)	MM(REF)
A		0.047 (MAX)	1.20 (MAX)
A1		0.004 ±0.002	0.10 ±0.05
A2		0.039 ±0.002	1.00 ±0.05
b		0.009 ±0.002	0.22 ±0.05
c		0.006 ±0.002	0.155 ±0.055
D		0.724 ±0.008	18.40 ±0.20
E		0.315 ±0.008	8.00 ±0.20
e		0.020 (TYP)	0.50 (TYP)
HD		0.787 ±0.008	20.00 ±0.20
L		0.024 ±0.004	0.60 ±0.10
L1		0.031 REF	0.8 REF
y		0.003 (MAX)	0.08 (MAX)
Θ		0°~5°	0°~5°



32-pin 8mm x 13.4mm sTSP Package Outline Dimension



SYM.	UNIT	INCH(BASE)	MM(REF)
A		0.049 (MAX)	1.25 (MAX)
A1		0.004 ±0.002	0.10 ±0.05
A2		0.039 ±0.002	1.00 ±0.05
b		0.009 ±0.002	0.22 ±0.05
c		0.006 ±0.002	0.155 ±0.055
D		0.465 ±0.008	11.80 ±0.20
E		0.315 ±0.008	8.00 ±0.20
e		0.020 (TYP)	0.50 (TYP)
HD		0.528±0.008	13.40 ±0.20.
L		0.02 ±0.008	0.50 ±0.20
L1		0.031 ±0.005	0.8 ±0.125
y		0.003 (MAX)	0.076 (MAX)
Θ		0°~5°	0°~5°

**ORDERING INFORMATION**

Package Type	Access Time (Speed)(ns)	Power Type	Temperature Range(°C)	Packing Type	Lyontek Item No.
32-pin (300mil) SOJ	12	Normal Power	0°C~70°C	Tube	LY611024JL-12
				Tape Reel	LY611024JL-12T
			-20°C~80°C	Tube	LY611024JL-12E
				Tape Reel	LY611024JL-12ET
			-40°C~85°C	Tube	LY611024JL-12I
				Tape Reel	LY611024JL-12IT
		Ultra Low Power	0°C~70°C	Tube	LY611024JL-12LL
				Tape Reel	LY611024JL-12LLT
			-20°C~80°C	Tube	LY611024JL-12LLE
				Tape Reel	LY611024JL-12LLET
			-40°C~85°C	Tube	LY611024JL-12LLI
				Tape Reel	LY611024JL-12LLIT
	15	Normal Power	0°C~70°C	Tube	LY611024JL-15
				Tape Reel	LY611024JL-15T
			-20°C~80°C	Tube	LY611024JL-15E
				Tape Reel	LY611024JL-15ET
			-40°C~85°C	Tube	LY611024JL-15I
				Tape Reel	LY611024JL-15IT
		Ultra Low Power	0°C~70°C	Tube	LY611024JL-15LL
				Tape Reel	LY611024JL-15LLT
			-20°C~80°C	Tube	LY611024JL-15LLE
				Tape Reel	LY611024JL-15LLET
			-40°C~85°C	Tube	LY611024JL-15LLI
				Tape Reel	LY611024JL-15LLIT

**ORDERING INFORMATION**

Package Type	Access Time (Speed)(ns)	Power Type	Temperature Range(°C)	Packing Type	Lyontek Item No.
32-pin (8mm x 20mm) TSOP I	12	Normal Power	0°C~70°C	Tray	LY611024LL-12
				Tape Reel	LY611024LL-12T
			-20°C~80°C	Tray	LY611024LL-12E
				Tape Reel	LY611024LL-12ET
			-40°C~85°C	Tray	LY611024LL-12I
				Tape Reel	LY611024LL-12IT
		Ultra Low Power	0°C~70°C	Tray	LY611024LL-12LL
				Tape Reel	LY611024LL-12LLT
			-20°C~80°C	Tray	LY611024LL-12LLE
				Tape Reel	LY611024LL-12LLET
			-40°C~85°C	Tray	LY611024LL-12LLI
				Tape Reel	LY611024LL-12LLIT
	15	Normal Power	0°C~70°C	Tray	LY611024LL-15
				Tape Reel	LY611024LL-15T
			-20°C~80°C	Tray	LY611024LL-15E
				Tape Reel	LY611024LL-15ET
			-40°C~85°C	Tray	LY611024LL-15I
				Tape Reel	LY611024LL-15IT
		Ultra Low Power	0°C~70°C	Tray	LY611024LL-15LL
				Tape Reel	LY611024LL-15LLT
			-20°C~80°C	Tray	LY611024LL-15LLE
				Tape Reel	LY611024LL-15LLET
			-40°C~85°C	Tray	LY611024LL-15LLI
				Tape Reel	LY611024LL-15LLIT

**ORDERING INFORMATION**

Package Type	Access Time (Speed)(ns)	Power Type	Temperature Range(°C)	Packing Type	Lyontek Item No.
32-pin (8mm x 13.4mm) sTSOP	12	Normal Power	0°C ~70°C	Tray	LY611024RL-12
				Tape Reel	LY611024RL-12T
			-20°C ~80°C	Tray	LY611024RL-12E
				Tape Reel	LY611024RL-12ET
			-40°C ~85°C	Tray	LY611024RL-12I
				Tape Reel	LY611024RL-12IT
		Ultra Low Power	0°C ~70°C	Tray	LY611024RL-12LL
				Tape Reel	LY611024RL-12LLT
			-20°C ~80°C	Tray	LY611024RL-12LLE
				Tape Reel	LY611024RL-12LLET
			-40°C ~85°C	Tray	LY611024RL-12LLI
				Tape Reel	LY611024RL-12LLIT
	15	Normal Power	0°C ~70°C	Tray	LY611024RL-15
				Tape Reel	LY611024RL-15T
			-20°C ~80°C	Tray	LY611024RL-15E
				Tape Reel	LY611024RL-15ET
			-40°C ~85°C	Tray	LY611024RL-15I
				Tape Reel	LY611024RL-15IT
		Ultra Low Power	0°C ~70°C	Tray	LY611024RL-15LL
				Tape Reel	LY611024RL-15LLT
			-20°C ~80°C	Tray	LY611024RL-15LLE
				Tape Reel	LY611024RL-15LLET
			-40°C ~85°C	Tray	LY611024RL-15LLI
				Tape Reel	LY611024RL-15LLIT



Lyontek Inc.

LY611024

Rev. 1.8

128K X 8 BIT HIGH SPEED CMOS SRAM

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