



REVISION HISTORY

<u>Revision</u>	<u>Description</u>	<u>Issue Date</u>
Rev. 1.0	Initial Issue	Jul.25.2004
Rev. 1.1	Delete I _{CC1} / I _{SB} Spec.	Sep.21.2004
Rev. 1.2	Adding Skinny PDIP	Aug.18.2005
Rev. 1.3	Revised sTSOP Package Outline Dimension	Mar.26.2008
Rev. 1.4	Revised V _{TERM} to V _{T1} and V _{T2} Revised TEST CONDITION of I _{SB1} /I _{DR} Added LL Spec.	Feb.2.2009
Rev. 1.5	Revised TEST CONDITION of I _{CC} Revised FEATURES & ORDERING INFORMATION Lead free and green package available to Green package available Deleted T _{SOLDER} in ABSOLUTE MAXIMUM RATINGS Added packing type in ORDERING INFORMATION	Apr.17.2009
Rev. 1.6	Revised PACKAGE OUTLINE DIMENSION in page 10	May.7.2010
Rev. 1.7	Revised ORDERING INFORMATION in page 11	Aug.31.2010
Rev. 1.8	Revised ORDERING INFORMATION in page 11/12/13 Revised PACKAGE OUTLINE DIMENSION in page 9/10/11	Jan.05.2015
Rev. 1.9	Correct ORDERING INFORMATION Typo.	May.20.2016
Rev. 1.10	Deleted WRITE CYCLE Notes : 1. WE#,CE# must be high during all address transitions. In page 6.	Jun.28.2016
Rev. 1.11	Revised ORDERING INFORMATION in page 11/12/13 Revised TEST CONDITION of I _{SB1} Revised SOJ Package Outline Dimension in page 8 Deleted -8/10ns Spec.	Jan.24.2017

FEATURES

- Fast access time : 12/15ns
- Low power consumption:
Operating current : 90/80mA (TYP.)
Standby current : 1mA (TYP.)
2 μ A (TYP.) LL-version
- Single 5V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data retention voltage : 2.0V (MIN.)
- **Green package available**
- Package : 28-pin 300 mil SOJ
28-pin 300 mil Skinny PDIP
28-pin 8mm x 13.4mm sTSP

GENERAL DESCRIPTION

The LY61256 is a 262,144-bit high speed CMOS static random access memory organized as 32,768 words by 8 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

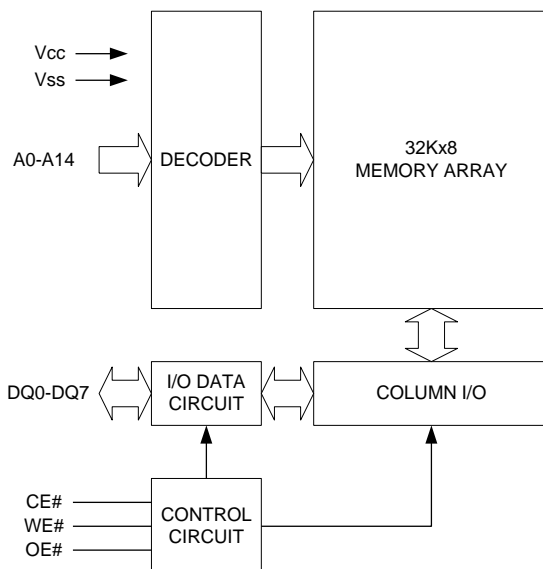
The LY61256 is well designed for high speed system application. Easy expansion is provided by using an active LOW Chip Enable(CE#). The active LOW Write Enable(WE#) controls both writing and reading of the memory.

The LY61256 operates from a single power supply of 5V and all inputs and outputs are fully TTL compatible

PRODUCT FAMILY

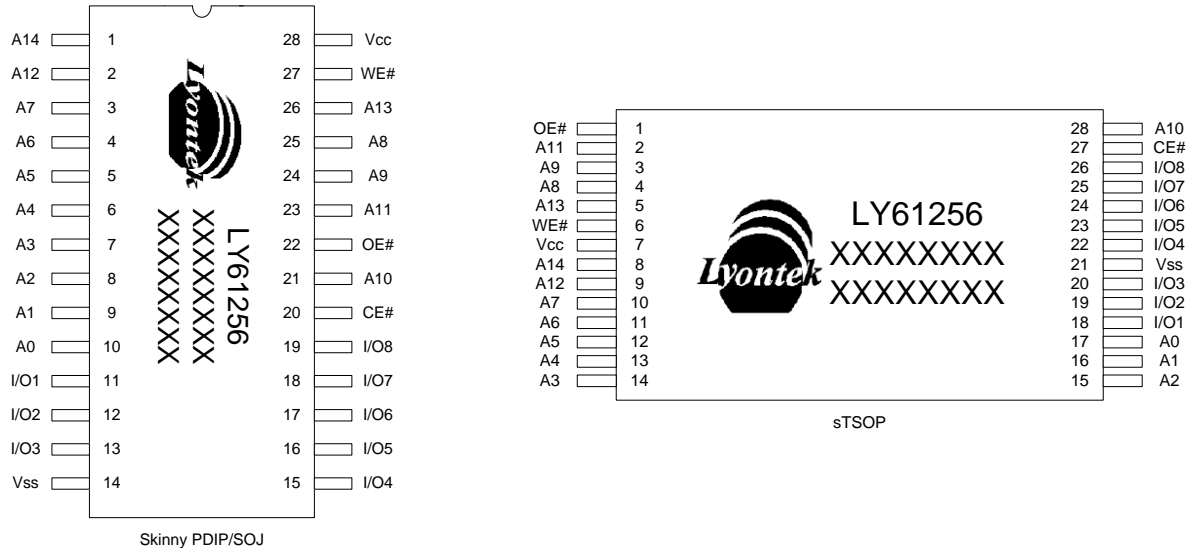
Product Family	Operating Temperature	V _{CC} Range	Speed	Power Dissipation	
				Standby(I _{SB1} , TYP.)	Operating(I _{CC} , TYP.)
LY61256	0 ~ 70°C	4.5 ~ 5.5V	12/15ns	1mA	90/80mA
LY61256(E)	-20 ~ 80°C	4.5 ~ 5.5V	12/15ns	1mA	90/80mA
LY61256(I)	-40 ~ 85°C	4.5 ~ 5.5V	12/15ns	1mA	90/80mA
LY61256(LL)	0 ~ 70°C	4.5 ~ 5.5V	12/15ns	2 μ A	90/80mA
LY61256(LLE)	-20 ~ 80°C	4.5 ~ 5.5V	12/15ns	2 μ A	90/80mA
LY61256(LLI)	-40 ~ 85°C	4.5 ~ 5.5V	12/15ns	2 μ A	90/80mA

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A14	Address Inputs
DQ0 - DQ7	Data Inputs/Outputs
CE#	Chip Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
V _{CC}	Power Supply
V _{SS}	Ground

PIN CONFIGURATION

ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on V _{CC} relative to V _{SS}	V _{T1}	-0.5 to 6.5	V
Voltage on any other pin relative to V _{SS}	V _{T2}	-0.5 to V _{CC} +0.5	V
Operating Temperature	T _A	0 to 70(C grade)	°C
		-20 to 80(E grade)	
		-40 to 85(I grade)	
Storage Temperature	T _{STG}	-65 to 150	°C
Power Dissipation	P _D	1	W
DC Output Current	I _{OUT}	50	mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE#	OE#	WE#	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	High-Z	I _{SB1}
Output Disable	L	H	H	High-Z	I _{CC}
Read	L	L	H	D _{OUT}	I _{CC}
Write	L	X	L	D _{IN}	I _{CC}

Note: H = V_{IH}, L = V_{IL}, X = Don't care.



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.* ⁴	MAX.	UNIT	
Supply Voltage	V _{CC}		4.5	5.0	5.5	V	
Input High Voltage	V _{IH} ^{*1}		2.4	-	V _{CC} +0.5	V	
Input Low Voltage	V _{IL} ^{*2}		- 0.5	-	0.8	V	
Input Leakage Current	I _{LI}	V _{CC} ≥ V _{IN} ≥ V _{SS}	- 1	-	1	μA	
Output Leakage Current	I _{LO}	V _{CC} ≥ V _{OUT} ≥ V _{SS} , Output Disabled	- 1	-	1	μA	
Output High Voltage	V _{OH}	I _{OH} = -4mA	2.4	-	-	V	
Output Low Voltage	V _{OL}	I _{OL} = 8mA	-	-	0.4	V	
Average Operating Power supply Current	I _{CC}	Cycle time = MIN. CE# = V _{IL} , I _{I/O} = 0mA Others at V _{IL} or V _{IH}	-12	-	90	160	mA
			-15	-	80	140	mA
Standby Power Supply Current	I _{SB1}	CE# ≥ V _{CC} - 0.2V, Others at 0.2V or V _{CC} -0.2V	Normal	-	1	5	mA
			LL	-	2	50	μA

Notes:

- V_{IH}(max) = V_{CC} + 3.0V for pulse width less than 10ns.
- V_{IL}(min) = V_{SS} - 3.0V for pulse width less than 10ns.
- Over/Undershoot specifications are characterized, not 100% tested.
- Typical values are included for reference only and are not guaranteed or tested.
Typical values are measured at V_{CC} = V_{CC}(TYP.) and T_A = 25°C

CAPACITANCE (T_A = 25°C, f = 1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Input Capacitance	C _{IN}	-	6	pF
Input/Output Capacitance	C _{I/O}	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0.2V to V _{CC} - 0.2V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	C _L = 30pF + 1TTL, I _{OH} /I _{OL} = -4mA/8mA



AC ELECTRICAL CHARACTERISTICS

(1) READ CYCLE

PARAMETER	SYM.	LY61256-12		LY61256-15		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t _{RC}	12	-	15	-	ns
Address Access Time	t _{AA}	-	12	-	15	ns
Chip Enable Access Time	t _{ACE}	-	12	-	15	ns
Output Enable Access Time	t _{OE}	-	6	-	7	ns
Chip Enable to Output in Low-Z	t _{CLZ} *	3	-	4	-	ns
Output Enable to Output in Low-Z	t _{OLZ} *	0	-	0	-	ns
Chip Disable to Output in High-Z	t _{CHZ} *	-	6	-	7	ns
Output Disable to Output in High-Z	t _{OHZ} *	-	6	-	7	ns
Output Hold from Address Change	t _{OH}	3	-	3	-	ns

(2) WRITE CYCLE

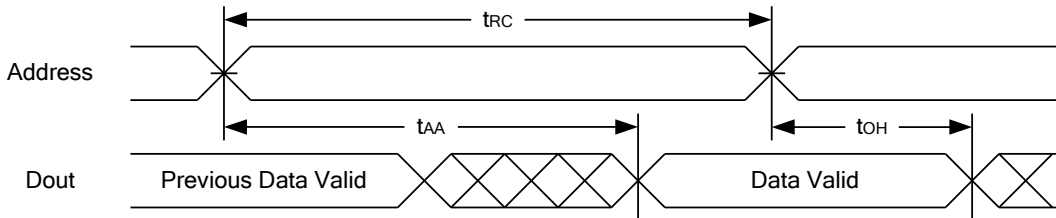
PARAMETER	SYM.	LY61256-12		LY61256-15		UNIT
		MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t _{WC}	12	-	15	-	ns
Address Valid to End of Write	t _{AW}	10	-	12	-	ns
Chip Enable to End of Write	t _{CW}	10	-	12	-	ns
Address Set-up Time	t _{AS}	0	-	0	-	ns
Write Pulse Width	t _{WP}	9	-	10	-	ns
Write Recovery Time	t _{WR}	0	-	0	-	ns
Data to Write Time Overlap	t _{DW}	7	-	8	-	ns
Data Hold from End of Write Time	t _{DH}	0	-	0	-	ns
Output Active from End of Write	t _{OW} *	3	-	4	-	ns
Write to Output in High-Z	t _{WHZ} *	-	7	-	8	ns

*These parameters are guaranteed by device characterization, but not production tested.

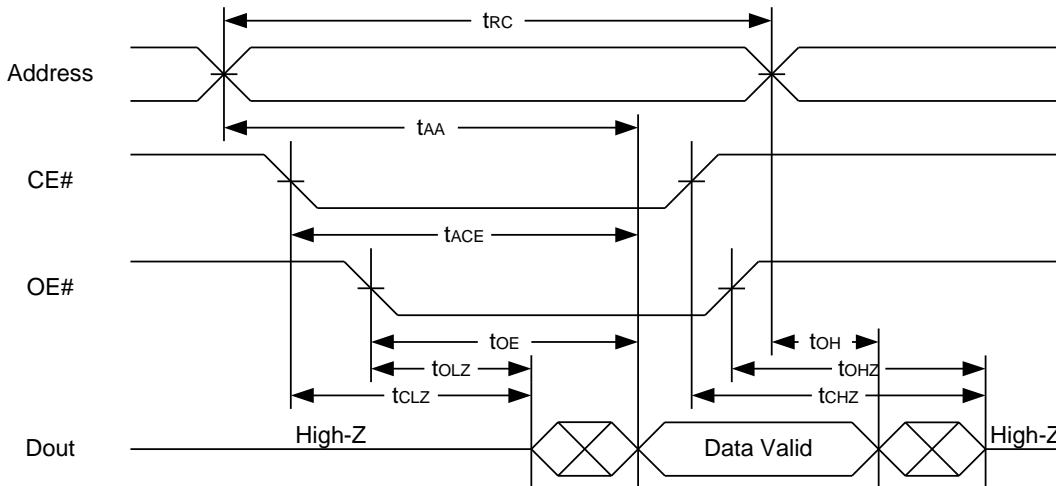


TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)

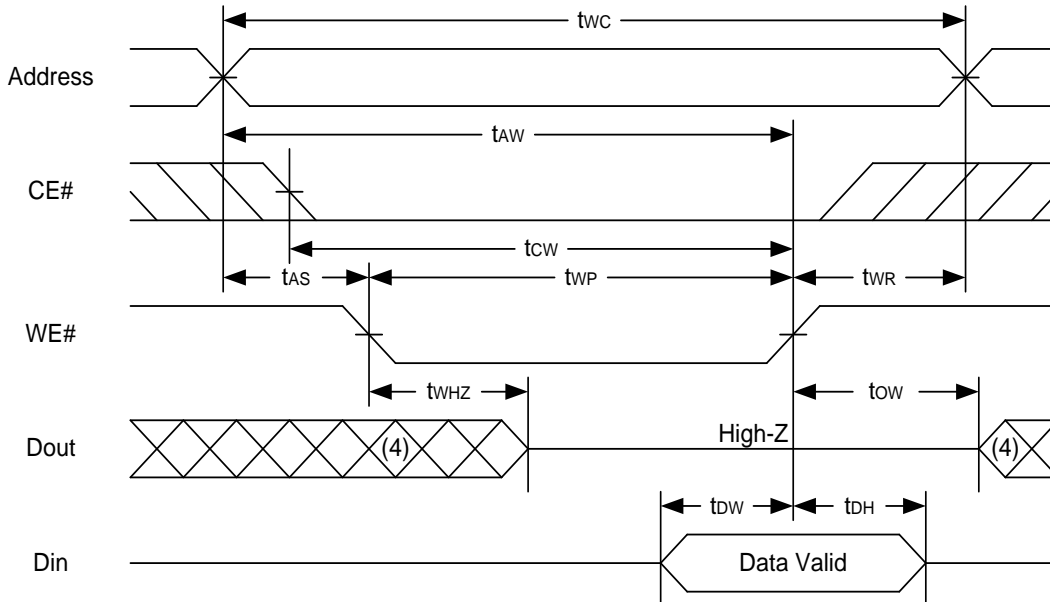
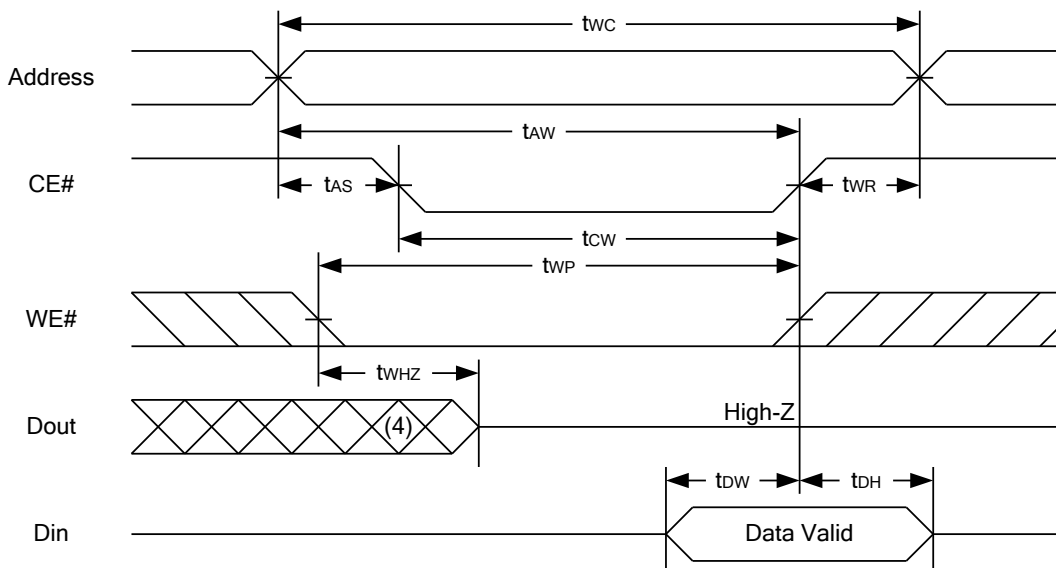


READ CYCLE 2 (CE# and OE# Controlled) (1,3,4,5)



Notes :

1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low.
3. Address must be valid prior to or coincident with CE# = low; otherwise t_{AA} is the limiting parameter.
4. t_{CLZ} , t_{OLZ} , t_{CHZ} and t_{OHZ} are specified with $C_L = 5pF$. Transition is measured $\pm 500mV$ from steady state.
5. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{OHZ} is less than t_{OLZ} .

WRITE CYCLE 1 (WE# Controlled) (1,2,4,5)

WRITE CYCLE 2 (CE# Controlled) (1,4,5)

Notes :

1. A write occurs during the overlap of a low CE#, low WE#.
2. During a WE# controlled write cycle with OE# low, t_{WP} must be greater than $t_{WHZ} + t_{DW}$ to allow the drivers to turn off and data to be placed on the bus.
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the CE# low transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
5. t_{OW} and t_{WHZ} are specified with $C_L = 5\text{pF}$. Transition is measured $\pm 500\text{mV}$ from steady state.

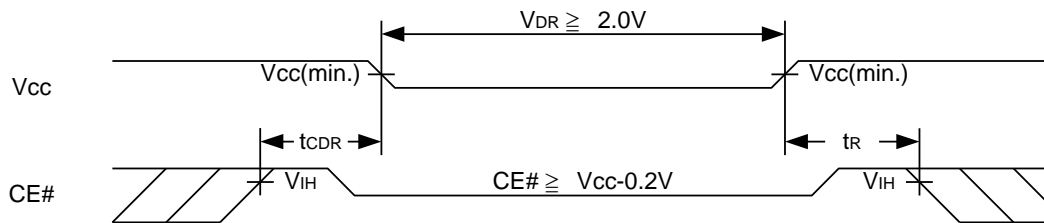


DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
V _{CC} for Data Retention	V _{DR}	CE# ≥ V _{CC} - 0.2V	2.0	-	5.5	V
Data Retention Current	I _{DR}	V _{CC} = 2.0V, CE# ≥ V _{CC} - 0.2V Normal	-	0.6	3	mA
		V _{CC} = 2.0V, CE# ≥ V _{CC} - 0.2V Others at 0.2V or V _{CC} -0.2V LL	-	0.5	20	μA
Chip Disable to Data Retention Time	t _{CDR}	See Data Retention Waveforms (below)	0	-	-	ns
Recovery Time	t _R		t _{RC} *	-	-	ns

t_{RC}* = Read Cycle Time

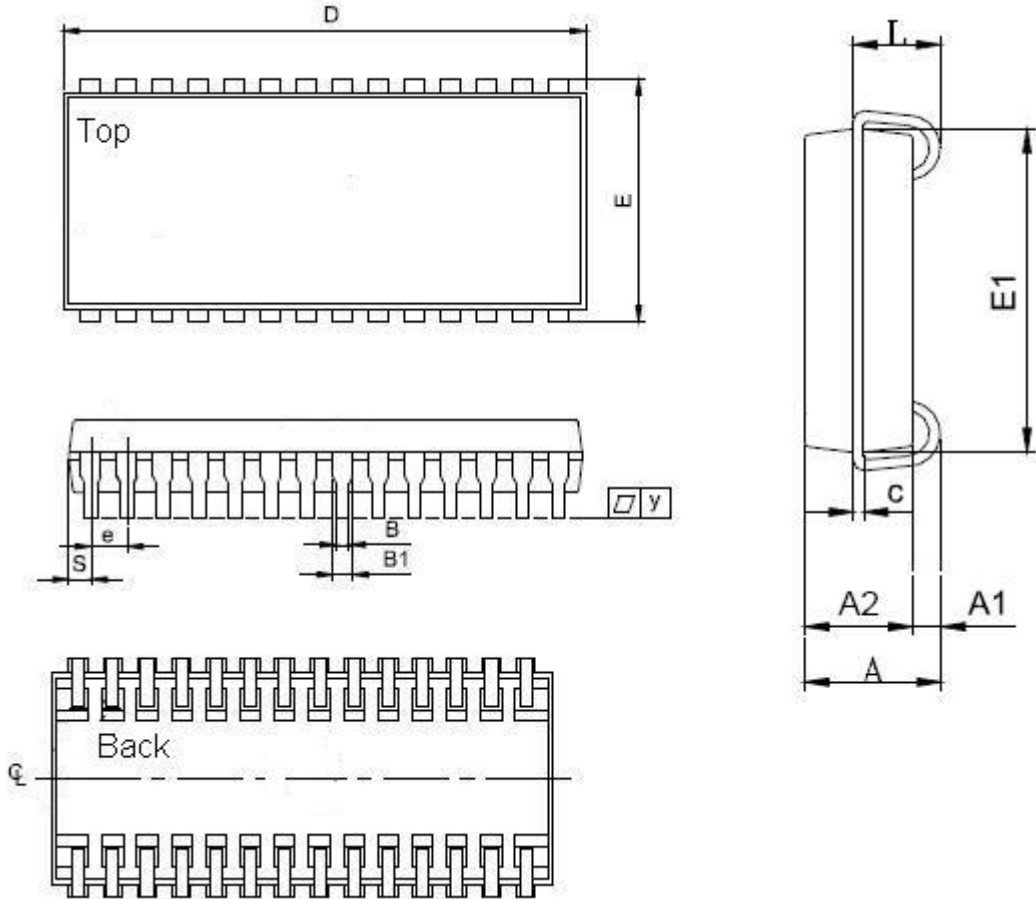
DATA RETENTION WAVEFORM





PACKAGE OUTLINE DIMENSION

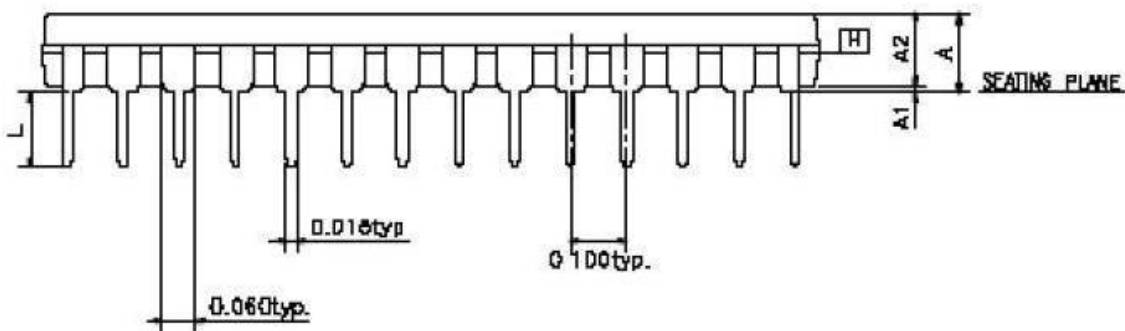
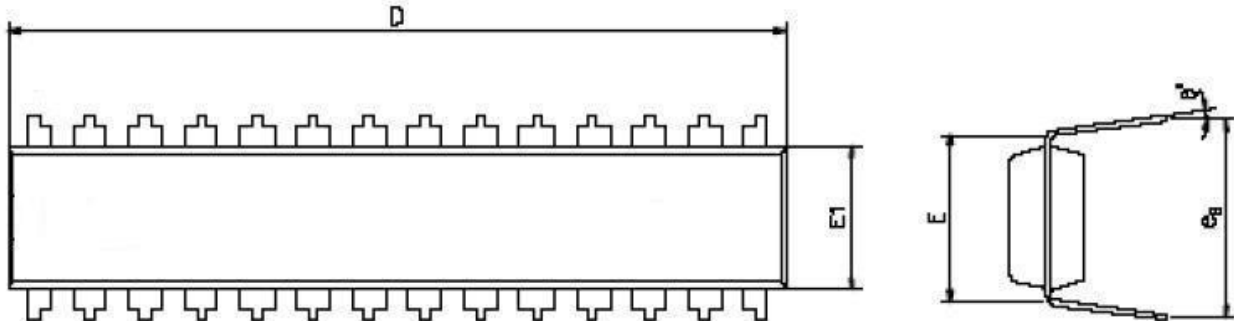
28-pin 300mil SOJ Package Outline Dimension



SYM.	UNIT	
	INCH(REF)	MM(BASE)
A	0.140(MAX)	3.556(MAX)
A1	0.025(MIN)	0.635(MIN)
A2	0.100±0.015	2.540±0.381
B	0.018±0.004	0.457±0.102
B1	0.028±0.004	0.711±0.102
c	0.010±0.004	0.254±0.102
D	0.710±0.020	18.03±0.508
E	0.337±0.010	8.560±0.254
E1	0.300±0.005	7.620±0.127
e	0.050±0.006	1.270±0.152
L	0.087±0.010	2.210±0.254
S	0.045(MAX)	1.143(MAX)
Y	0.004(MAX)	0.102(MAX)

Note : 1.S/E/D dimension is not including mold flash.
 2.The end flash in package lengthwise is not more than 10 mils each side.

28-pin 300mil PDIP Package Outline Dimension

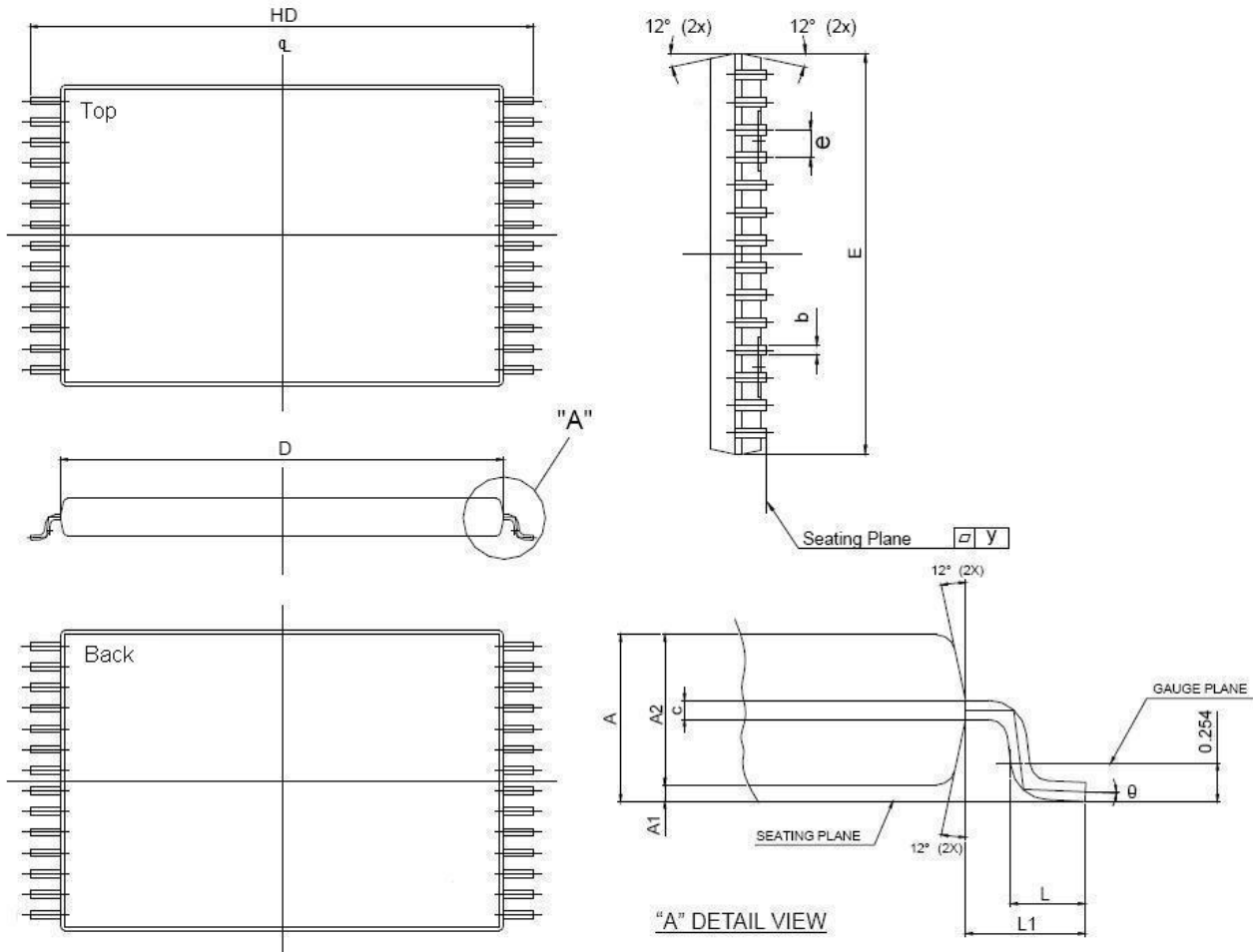


SYMBOLS	MIN.	NOR.	MAX.
A	—	—	0.210
A1	0.015	—	—
A2	0.125	0.130	0.135
D	1.385	1.390	1.400
E	0.310 BSC		
E1	0.283	0.288	0.293
L	0.115	0.130	0.150
θ	0	7	15

UNIT : INCH

NOTE:

1. JEDEC OUTLINE : MS-D15 AH

28-pin 8 x 13.4mm sTSP Package Outline Dimension


SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.00	1.10	1.20	0.040	0.043	0.047
A1	0.05	-	0.15	0.002	-	0.006
A2	0.91	1.00	1.05	0.036	0.039	0.041
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.07	0.15	0.23	0.003	0.006	0.009
HD	13.20	13.40	13.60	0.520	0.528	0.535
D	11.60	11.80	12.00	0.457	0.465	0.472
E	7.80	8.00	8.20	0.307	0.315	0.323
e	-	0.55	-	-	0.0216	-
L	0.30	0.50	0.70	0.012	0.020	0.028
L1	0.675	-	-	0.027	-	-
Y	0.00	-	0.076	0.000	-	0.003
θ	0°	3°	5°	0°	3°	5°

ORDERING INFORMATION

Package Type	Access Time (Speed)(ns)	Power Type	Temperature Range(°C)	Packing Type	Lyontek Item No.
28-pin (300mil) SOJ	12	Normal Power	0°C ~70°C	Tube	LY61256JL-12
				Tape Reel	LY61256JL-12T
			-20°C ~80°C	Tube	LY61256JL-12E
				Tape Reel	LY61256JL-12ET
			-40°C ~85°C	Tube	LY61256JL-12I
				Tape Reel	LY61256JL-12IT
	12	Ultra Low Power	0°C ~70°C	Tube	LY61256JL-12LL
				Tape Reel	LY61256JL-12LLT
			-20°C ~80°C	Tube	LY61256JL-12LLE
				Tape Reel	LY61256JL-12LLET
			-40°C ~85°C	Tube	LY61256JL-12LLI
				Tape Reel	LY61256JL-12LLIT
	15	Normal Power	0°C ~70°C	Tube	LY61256JL-15
				Tape Reel	LY61256JL-15T
			-20°C ~80°C	Tube	LY61256JL-15E
				Tape Reel	LY61256JL-15ET
			-40°C ~85°C	Tube	LY61256JL-15I
				Tape Reel	LY61256JL-15IT
	15	Ultra Low Power	0°C ~70°C	Tube	LY61256JL-15LL
				Tape Reel	LY61256JL-15LLT
-20°C ~80°C			Tube	LY61256JL-15LLE	
			Tape Reel	LY61256JL-15LLET	
-40°C ~85°C			Tube	LY61256JL-15LLI	
			Tape Reel	LY61256JL-15LLIT	



ORDERING INFORMATION

Package Type	Access Time (Speed)(ns)	Power Type	Temperature Range(°C)	Packing Type	Lyontek Item No.
28-pin (300mil) Skinny PDIP	12	Normal Power	0°C ~70°C	Tube	LY61256DL-12
			-20°C ~80°C	Tube	LY61256DL-12E
			-40°C ~85°C	Tube	LY61256DL-12I
	12	Ultra Low Power	0°C ~70°C	Tube	LY61256DL-12LL
			-20°C ~80°C	Tube	LY61256DL-12LLE
			-40°C ~85°C	Tube	LY61256DL-12LLI
	15	Normal Power	0°C ~70°C	Tube	LY61256DL-15
			-20°C ~80°C	Tube	LY61256DL-15E
			-40°C ~85°C	Tube	LY61256DL-15I
	15	Ultra Low Power	0°C ~70°C	Tube	LY61256DL-15LL
			-20°C ~80°C	Tube	LY61256DL-15LLE
			-40°C ~85°C	Tube	LY61256DL-15LLI



ORDERING INFORMATION

Package Type	Access Time (Speed)(ns)	Power Type	Temperature Range(°C)	Packing Type	Lyontek Item No.
28-pin (8mm x 13.4mm) sTSOP	12	Normal Power	0°C~70°C	Tray	LY61256RL-12
				Tape Reel	LY61256RL-12T
			-20°C~80°C	Tray	LY61256RL-12E
				Tape Reel	LY61256RL-12ET
	-40°C~85°C	Normal Power	Tray	LY61256RL-12I	
			Tape Reel	LY61256RL-12IT	
	12	Ultra Low Power	0°C~70°C	Tray	LY61256RL-12LL
				Tape Reel	LY61256RL-12LLT
			-20°C~80°C	Tray	LY61256RL-12LLE
				Tape Reel	LY61256RL-12LLET
	-40°C~85°C	Ultra Low Power	Tray	LY61256RL-12LLI	
			Tape Reel	LY61256RL-12LLIT	
	15	Normal Power	0°C~70°C	Tray	LY61256RL-15
				Tape Reel	LY61256RL-15T
			-20°C~80°C	Tray	LY61256RL-15E
				Tape Reel	LY61256RL-15ET
-40°C~85°C	Normal Power	Tray	LY61256RL-15I		
		Tape Reel	LY61256RL-15IT		
15	Ultra Low Power	0°C~70°C	Tray	LY61256RL-15LL	
			Tape Reel	LY61256RL-15LLT	
		-20°C~80°C	Tray	LY61256RL-15LLE	
			Tape Reel	LY61256RL-15LLET	
-40°C~85°C	Ultra Low Power	Tray	LY61256RL-15LLI		
		Tape Reel	LY61256RL-15LLIT		



Lyontek Inc.

LY61256

Rev. 1.11

32K X 8 BIT HIGH SPEED CMOS SRAM

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