



REVISION HISTORY

<u>Revision</u>	<u>Description</u>	<u>Issue Date</u>
Rev. 1.0	Initial Issue	Apr.28.2006
Rev. 1.1	Revised PACKAGE OUTLINE DIMENSION (TSOP II)	Apr.12.2007
Rev. 1.2	Revised V_{TERM} to V_{T1} and V_{T2} Revised TEST CONDITION of $I_{CC}/I_{SB1}/I_{DR}$ Revised FEATURES & ORDERING INFORMATION Lead free and green package available to Green package available Deleted T_{SOLDER} in ABSOLUTE MAXIMUM RATINGS Added packing type in ORDERING INFORMATION	Apr.17.2009
Rev. 1.3	Revised ORDERING INFORMATION in page 9 Added E/I grade	Aug.25.2010
Rev. 1.4	Added -20ns Spec. Deleted E-grade Revised $V_{IH(max)}$ & $V_{IL(min)}$ Notes in page 4 $V_{IH(max)} = V_{CC} + 2.0V$ for pulse width less than 6ns. $V_{IL(min)} = V_{SS} - 2.0V$ for pulse width less than 6ns.	Mar.05.2014
Rev. 1.5	Revised $V_{IL(max)}$ from 0.6V to 0.8V	May.08.2014
Rev. 1.6	Corrected symbols in DC ELECTRICAL CHARACTERISTICS Deleted WRITE CYCLE Notes : 1. WE#,CE# must be high during all address transitions. in page 6	Mar.22.2017

FEATURES

- Fast access time : 10/12/15/20ns
- Low power consumption:
 Operating current: 220/200/180/160mA (TYP.)
 Standby current: 1mA (TYP.) 10/12/15-version
 4 μ A (TYP.) 20-version
- Single 5V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data retention voltage : 2.0V (MIN.)
- **Green package available**
- Package : 44-pin 400mil TSOP II

GENERAL DESCRIPTION

The LY615128 is a 4,194,304-bit low power CMOS static random access memory organized as 524,288 words by 8 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

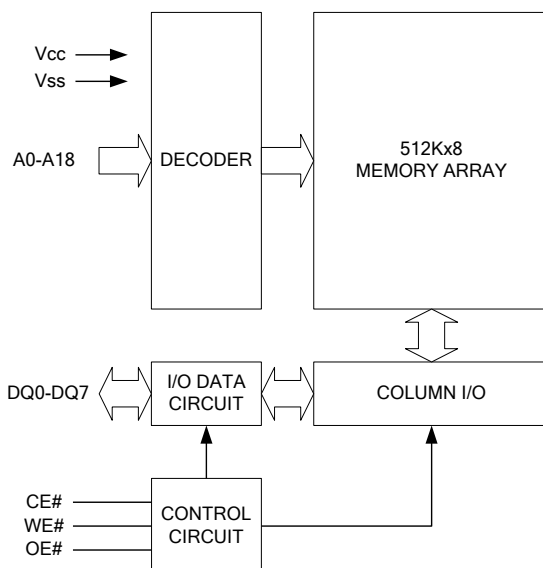
The LY615128 is well designed for low power application, and particularly well suited for battery back-up nonvolatile memory application.

The LY615128 operates from a single power supply of 5V and all inputs and outputs are fully TTL compatible.

PRODUCT FAMILY

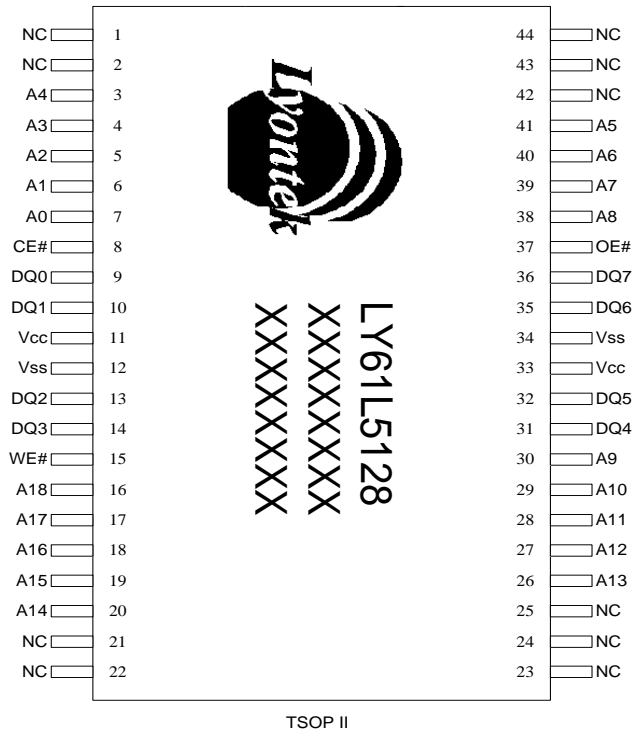
Product Family	Operating Temperature	V _{CC} Range	Speed	Power Dissipation	
				Standby(I _{SB1} , TYP.)	Operating(I _{CC1} , TYP.)
LY615128	0 ~ 70°C	4.5 ~ 5.5V	10/12/15ns	1mA	220/200/180mA
LY615128(I)	-40 ~ 85°C	4.5 ~ 5.5V	10/12/15ns	1mA	220/200/180mA
LY615128	0 ~ 70°C	4.5 ~ 5.5V	20ns	4 μ A	160mA
LY615128(I)	-40 ~ 85°C	4.5 ~ 5.5V	20ns	4 μ A	160mA

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A18	Address Inputs
DQ0 - DQ7	Data Inputs/Outputs
CE#	Chip Enable Inputs
WE#	Write Enable Input
OE#	Output Enable Input
V _{CC}	Power Supply
V _{SS}	Ground
NC	No Connection

PIN CONFIGURATION

ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on V _{CC} relative to V _{SS}	V _{T1}	-0.5 to 6.5	V
Voltage on any other pin relative to V _{SS}	V _{T2}	-0.5 to V _{CC} +0.5	V
Operating Temperature	T _A	0 to 70(C grade)	°C
		-40 to 85(I grade)	
Storage Temperature	T _{STG}	-65 to 150	°C
Power Dissipation	P _D	1	W
DC Output Current	I _{OUT}	50	mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE#	OE#	WE#	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	High-Z	I _{SB} , I _{SB1}
Output Disable	L	H	H	High-Z	I _{CC}
Read	L	L	H	D _{OUT}	I _{CC}
Write	L	X	L	D _{IN}	I _{CC}

Note: H = V_{IH}, L = V_{IL}, X = Don't care

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP. ⁴	MAX.	UNIT	
Supply Voltage	V_{CC}		4.5	5.0	5.5	V	
Input High Voltage	V_{IH}^{*1}		2.2	-	$V_{CC}+0.3$	V	
Input Low Voltage	V_{IL}^{*2}		-0.3	-	0.8	V	
Input Leakage Current	I_{LI}	$V_{CC} \geq V_{IN} \geq V_{SS}$	-1	-	1	μA	
Output Leakage Current	I_{LO}	$V_{CC} \geq V_{OUT} \geq V_{SS}$, Output Disabled	-1	-	1	μA	
Output High Voltage	V_{OH}	$I_{OH} = -4mA$	2.4	-	-	V	
Output Low Voltage	V_{OL}	$I_{OL} = 8mA$	-	-	0.4	V	
Average Operating Power supply Current	I_{CC}	Cycle time = MIN. $CE\# = V_{IL}$, $I_{I/O} = 0mA$, Others at V_{IL} or V_{IH}	-10	-	220	280	mA
			-12	-	200	250	mA
			-15	-	180	220	mA
			-20	-	160	200	mA
Standby Power Supply Current	I_{SB}	$CE\# = V_{IH}$, Others at V_{IL} or V_{IH}	-	5	50	mA	
	I_{SB1}	$CE\# \geq V_{CC} - 0.2V$, Others at 0.2V or $V_{CC}-0.2V$	-10/12/15	-	1	10	mA
			-20	-	4	100	μA

Notes:

- $V_{IH(max)} = V_{CC} + 2.0V$ for pulse width less than 6ns.
- $V_{IL(min)} = V_{SS} - 2.0V$ for pulse width less than 6ns.
- Over/Undershoot specifications are characterized on engineering evaluation stage, not for mass production test.
- Typical values are included for reference only and are not guaranteed or tested.
Typical values are measured at $V_{CC} = V_{CC(TYP)}$ and $T_A = 25^\circ C$

CAPACITANCE ($T_A = 25^\circ C$, $f = 1.0MHz$)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Input Capacitance	C_{IN}	-	8	pF
Input/Output Capacitance	$C_{I/O}$	-	10	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0.2V to $V_{CC} - 0.2V$
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	$C_L = 30pF + 1TTL$, $I_{OH}/I_{OL} = -8mA/16mA$

AC ELECTRICAL CHARACTERISTICS
(1) READ CYCLE

PARAMETER	SYM.	LY615128-10		LY615128-12		LY615128-15		LY615128-20		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t _{RC}	10	-	12	-	15	-	20	-	ns
Address Access Time	t _{AA}	-	10	-	12	-	15	-	20	ns
Chip Enable Access Time	t _{ACE}	-	10	-	12	-	15	-	20	ns
Output Enable Access Time	t _{OE}	-	5	-	6	-	8	-	8	ns
Chip Enable to Output in Low-Z	t _{CLZ} *	2	-	3	-	4	-	5	-	ns
Output Enable to Output in Low-Z	t _{OLZ} *	0	-	0	-	0	-	0	-	ns
Chip Disable to Output in High-Z	t _{CHZ} *	-	5	-	6	-	7	-	8	ns
Output Disable to Output in High-Z	t _{OHZ} *	-	5	-	6	-	7	-	8	ns
Output Hold from Address Change	t _{OH}	3	-	3	-	3	-	3	-	ns

(2) WRITE CYCLE

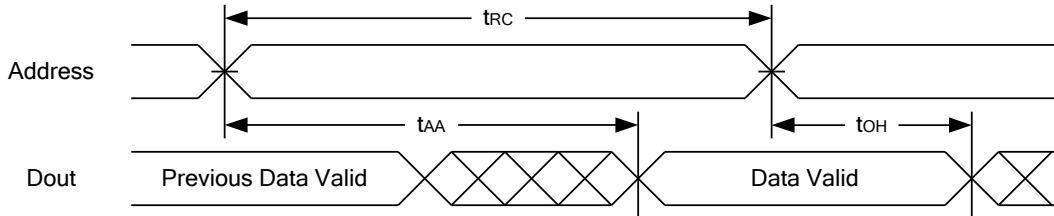
PARAMETER	SYM.	LY615128-10		LY615128-12		LY615128-15		LY615128-20		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t _{WC}	10	-	12	-	15	-	20	-	ns
Address Valid to End of Write	t _{AW}	8	-	10	-	12	-	15	-	ns
Chip Enable to End of Write	t _{CW}	8	-	10	-	12	-	15	-	ns
Address Set-up Time	t _{AS}	0	-	0	-	0	-	0	-	ns
Write Pulse Width	t _{WP}	8	-	9	-	10	-	12	-	ns
Write Recovery Time	t _{WR}	0	-	0	-	0	-	0	-	ns
Data to Write Time Overlap	t _{DW}	6	-	7	-	8	-	10	-	ns
Data Hold from End of Write Time	t _{DH}	0	-	0	-	0	-	0	-	ns
Output Active from End of Write	t _{OW} *	2	-	3	-	4	-	5	-	ns
Write to Output in High-Z	t _{WHZ} *	-	6	-	7	-	8	-	10	ns

*These parameters are guaranteed by device characterization, but not production tested.

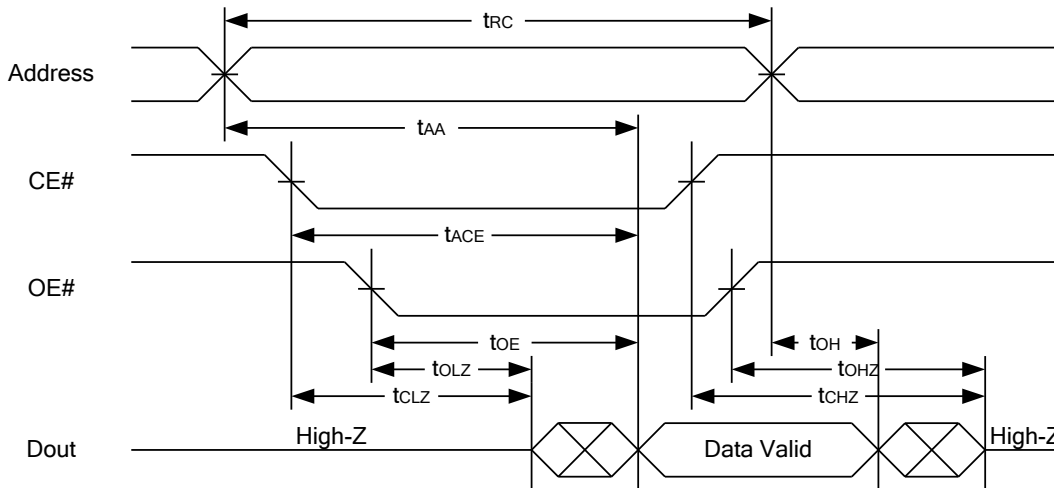


TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)

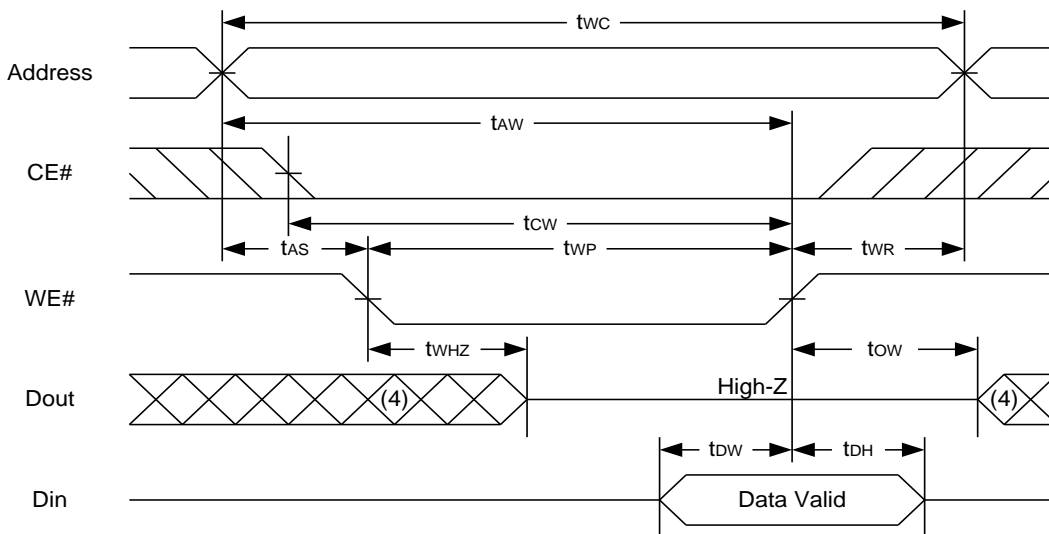
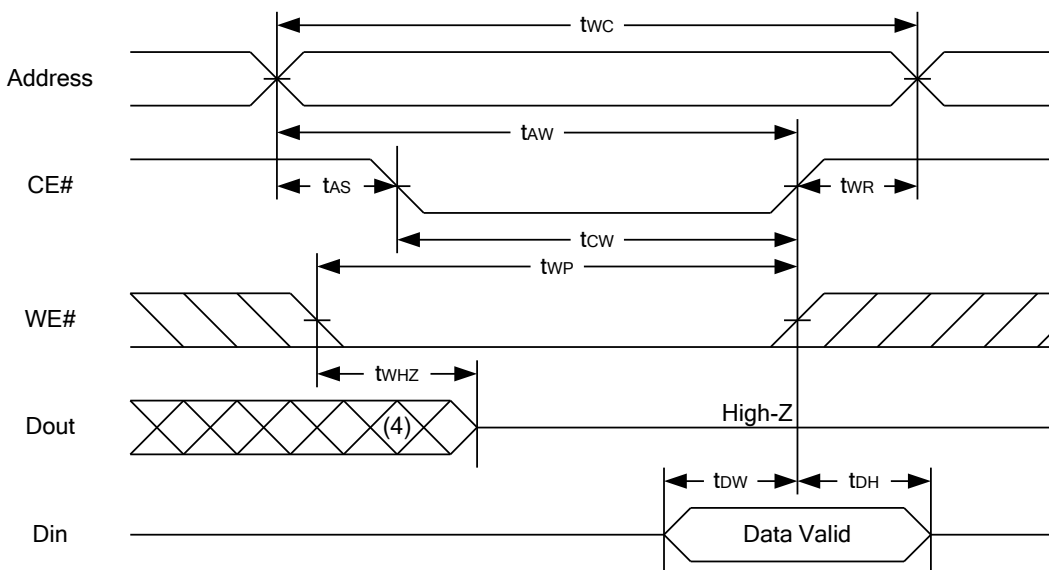


READ CYCLE 2 (CE# and OE# Controlled) (1,3,4,5)



Notes :

1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low.
3. Address must be valid prior to or coincident with CE# = low,; otherwise t_{AA} is the limiting parameter.
4. t_{CLZ} , t_{OLZ} , t_{CHZ} and t_{OHZ} are specified with $C_L = 5pF$. Transition is measured $\pm 500mV$ from steady state.
5. At a given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{OHZ} is less than t_{OLZ} .

WRITE CYCLE 1 (WE# Controlled) (1,2,4,5)

WRITE CYCLE 2 (CE# Controlled) (1,4,5)


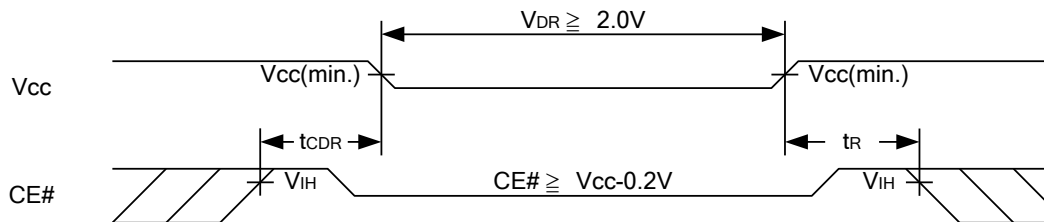
Notes :

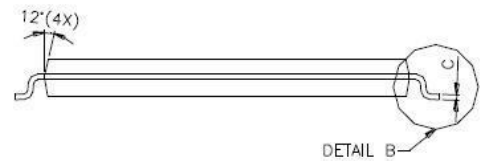
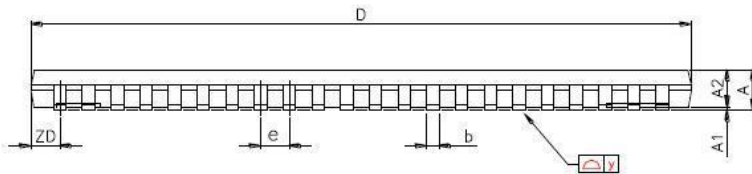
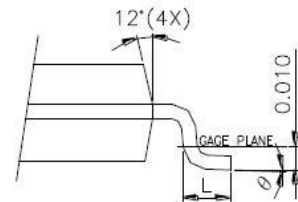
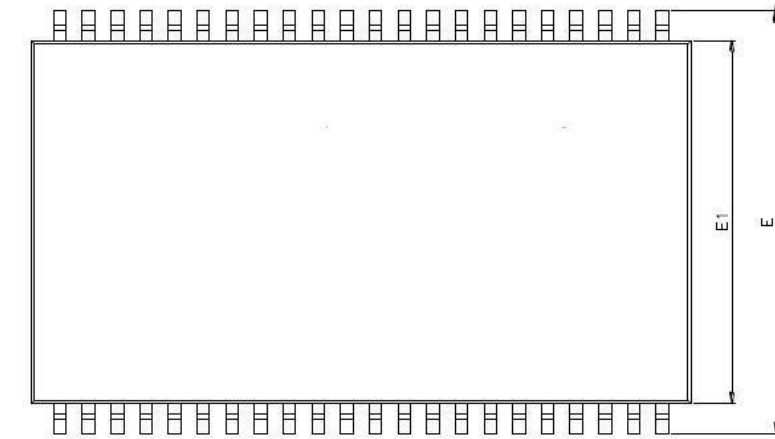
1. A write occurs during the overlap of a low CE#, low WE#.
2. During a WE# controlled write cycle with OE# low, t_{WP} must be greater than $t_{WHZ} + t_{DW}$ to allow the drivers to turn off and data to be placed on the bus.
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the CE# low transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
5. t_{OW} and t_{WHZ} are specified with $C_L = 5\text{pF}$. Transition is measured $\pm 500\text{mV}$ from steady state.

DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
V _{CC} for Data Retention	V _{DR}	CE# ≥ V _{CC} - 0.2V	2.0	-	5.5	V
Data Retention Current	I _{DR}	V _{CC} = 2.0V, CE# ≥ V _{CC} - 0.2V	-10/12/15	0.5	1	mA
		Others at 0.2V or V _{CC} - 0.2V	-20	4	100	μA
Chip Disable to Data Retention Time	t _{CDR}	See Data Retention Waveforms (below)	0	-	-	ns
Recovery Time	t _R		t _{RC} *	-	-	ns

 t_{RC}* = Read Cycle Time

DATA RETENTION WAVEFORM


PACKAGE OUTLINE DIMENSION
44-pin 400 mil TSOP II Package Outline Dimension


SYMBOLS	DIMENSIONS IN MILLMETERS			DIMENSIONS IN MILS		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	-	-	1.20	-	-	47.2
A1	0.05	0.10	0.15	2.0	3.9	5.9
A2	0.95	1.00	1.05	37.4	39.4	41.3
b	0.30	-	0.45	11.8	-	17.7
c	0.12	-	0.21	4.7	-	8.3
D	18.212	18.415	18.618	717	725	733
E	11.506	11.760	12.014	453	463	473
E1	9.957	10.160	10.363	392	400	408
e	-	0.800	-	-	31.5	-
L	0.40	0.50	0.60	15.7	19.7	23.6
ZD	-	0.805	-	-	31.7	-
y	-	-	0.076	-	-	3
θ	0°	3°	6°	0°	3°	6°

**ORDERING INFORMATION**

Package Type	Access Time (Speed/ns)	Temperature Range(°C)	Packing Type	Lyontek Item No.
44-pin (400mil) TSOP II	10	0°C~70°C	Tray	LY615128ML-10
			Tape Reel	LY615128ML-10T
		-40°C~85°C	Tray	LY615128ML-10I
			Tape Reel	LY615128ML-10IT
	12	0°C~70°C	Tray	LY615128ML-12
			Tape Reel	LY615128ML-12T
		-40°C~85°C	Tray	LY615128ML-12I
			Tape Reel	LY615128ML-12IT
	20	0°C~70°C	Tray	LY615128ML-20
			Tape Reel	LY615128ML-20T
		-40°C~85°C	Tray	LY615128ML-20I
			Tape Reel	LY615128ML-20IT



Lyontek Inc.

LY615128

Rev. 1.6

5V 512K X 8 BIT HIGH SPEED CMOS SRAM

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