



REVISION HISTORY

| <u>Revision</u> | <u>Description</u> | <u>Issue Date</u> |
|-----------------|--|-------------------|
| Rev. 1.0 | Initial Issue | Jul.25.2004 |
| Rev. 1.1 | Delete I _{CC1} Spec. | Sep.21.2004 |
| Rev. 2.0 | Adding -10ns Spec. | Aug.30.2005 |
| Rev. 2.1 | Revised V _{TERM} to V _{T1} and V _{T2} Revised TEST CONDITION of I _{SB1} /I _{DR} Added LL Spec. | Feb.02.2009 |
| Rev.2.2 | Revised TEST CONDITION of I _{CC} /I _{SB} Revised FEATURES & ORDERING INFORMATION Lead free and green package available to Green package available Deleted T _{SOLDER} in ABSOLUTE MAXIMUN RATINGS Added packing type in ORDERING INFORMATION | Apr.17.2009 |
| Rev. 2.3 | Revised PACKAGE OUTLINE DIMENSION in page 9 | Dec.18.2009 |
| Rev. 2.4 | Added I grade in normal grade Deleted -10/12/15ns Spec. in LL grade Added -18ns Spec. In LL grade | Apr.27.2010 |
| Rev. 2.5 | Revised PACKAGE OUTLINE DIMENSION in page 10/11 | May.07.2010 |
| Rev. 2.6 | Revised ORDERING INFORMATION in page 12 | Aug.30.2010 |
| Rev. 2.7 | Add package type: TFBGA 36-ball Revised ORDERING INFORMATION in page 14~page15 | Jan.23.2013 |
| Rev. 2.8 | Deleted -15ns Spec. Deleted WRITE CYCLE Notes : 1. WE#, CE# must be high or CE2 must be low during all address transitions in page 7. | Dec.13.2016 |

FEATURES

- Fast access time : 10/12/18ns
- Low power consumption:
 Operating current : 75/70/55mA (TYP.)
 Standby current : 0.6mA (TYP.)
 1 μ A (TYP.) LL -version
- Single 3.3V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data retention voltage : 2.0V (MIN.)
- **Green package available**
- Package : 32-pin 300 mil SOJ
 32-pin 8mm x 20mm TSOP I
 32-pin 8mm x 13.4mm sTSOP
 36-ball 6mm x 8mm TFBGA

GENERAL DESCRIPTION

The LY61L1024 is a 1,048,576-bit low power CMOS static random access memory organized as 131,072 words by 8 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

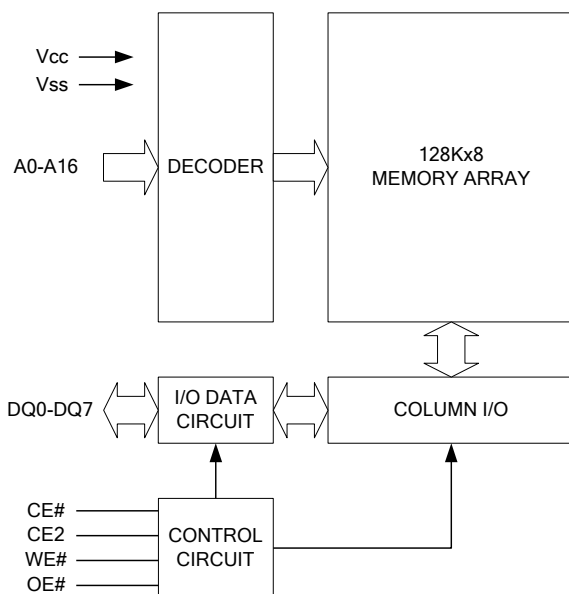
The LY61L1024 is well designed for very high speed system applications, and particularly well suited for battery back-up nonvolatile memory application.

The LY61L1024 operates from a single power supply of 3.3V and all inputs and outputs are fully TTL compatible

PRODUCT FAMILY

| Product Family | Operating Temperature | V _{CC} Range | Speed | Power Dissipation | |
|----------------|-----------------------|-----------------------|-------|----------------------------------|-----------------------------------|
| | | | | Standby(I _{SB1} , TYP.) | Operating(I _{CC} , TYP.) |
| LY61L1024 | 0 ~ 70°C | 3.15 ~ 3.6V | 10ns | 0.6mA | 75mA |
| LY61L1024 | 0 ~ 70°C | 3.0 ~ 3.6V | 12ns | 0.6mA | 70mA |
| LY61L1024(I) | -40 ~ 85°C | 3.15 ~ 3.6V | 10ns | 0.6mA | 75mA |
| LY61L1024(I) | -40 ~ 85°C | 3.0 ~ 3.6V | 12ns | 0.6mA | 70mA |
| LY61L1024(LL) | 0 ~ 70°C | 3.0 ~ 3.6V | 18ns | 1 μ A | 55mA |
| LY61L1024(LLI) | -40 ~ 85°C | 3.0 ~ 3.6V | 18ns | 1 μ A | 55mA |

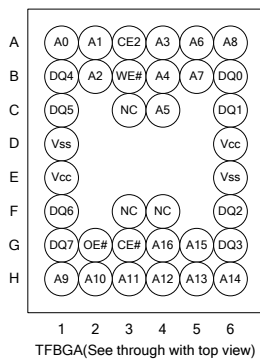
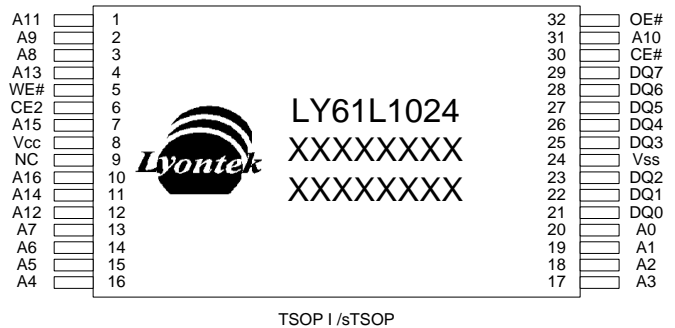
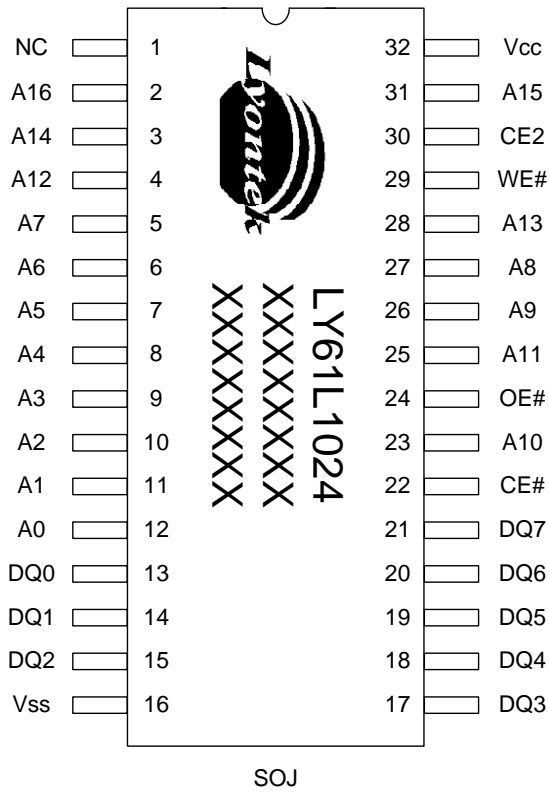
FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

| SYMBOL | DESCRIPTION |
|-----------------|---------------------|
| A0 - A16 | Address Inputs |
| DQ0 - DQ7 | Data Inputs/Outputs |
| CE#, CE2 | Chip Enable Inputs |
| WE# | Write Enable Input |
| OE# | Output Enable Input |
| V _{CC} | Power Supply |
| V _{SS} | Ground |
| NC | No Connection |

PIN CONFIGURATION



PS: All pin out definition are relative with "Lyontek logo" orientation.



ABSOLUTE MAXIMUM RATINGS*

| PARAMETER | SYMBOL | RATING | UNIT |
|--|------------------|------------------------------|------|
| Voltage on V _{CC} relative to V _{SS} | V _{T1} | -0.5 to 4.6 | V |
| Voltage on any other pin relative to V _{SS} | V _{T2} | -0.5 to V _{CC} +0.5 | V |
| Operating Temperature | T _A | 0 to 70(C grade) | °C |
| | | -40 to 85(I grade) | |
| Storage Temperature | T _{STG} | -65 to 150 | °C |
| Power Dissipation | P _D | 1 | W |
| DC Output Current | I _{OUT} | 50 | mA |

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

| MODE | CE# | CE2 | OE# | WE# | I/O OPERATION | SUPPLY CURRENT |
|----------------|-----|-----|-----|-----|------------------|------------------------------------|
| Standby | H | X | X | X | High-Z | I _{SB} , I _{SB1} |
| | X | L | X | X | High-Z | I _{SB} , I _{SB1} |
| Output Disable | L | H | H | H | High-Z | I _{CC} |
| Read | L | H | L | H | D _{OUT} | I _{CC} |
| Write | L | H | X | L | D _{IN} | I _{CC} |

Note: H = V_{IH}, L = V_{IL}, X = Don't care.



DC ELECTRICAL CHARACTERISTICS

| PARAMETER | SYMBOL | TEST CONDITION | MIN. | TYP. ⁴ | MAX. | UNIT | |
|--|-------------------------------|--|--------|-------------------|----------------------|------|----|
| Supply Voltage | V _{CC} | | 3.0 | 3.3 | 3.6 | V | |
| Input High Voltage | V _{IH} ^{*1} | | 2.0 | - | V _{CC} +0.5 | V | |
| Input Low Voltage | V _{IL} ^{*2} | | - 0.5 | - | 0.6 | V | |
| Input Leakage Current | I _{LI} | V _{CC} ≥ V _{IN} ≥ V _{SS} | - 1 | - | 1 | μA | |
| Output Leakage Current | I _{LO} | V _{CC} ≥ V _{OUT} ≥ V _{SS} , Output Disabled | - 1 | - | 1 | μA | |
| Output High Voltage | V _{OH} | I _{OH} = -4mA | 2.2 | - | - | V | |
| Output Low Voltage | V _{OL} | I _{OL} = 8mA | - | - | 0.4 | V | |
| Average Operating Power supply Current | I _{CC} | Cycle time = MIN. CE# = V _{IL} and CE2 = V _{IH} , I _{I/O} = 0mA Others at V _{IL} or V _{IH} | -10 | - | 75 | 120 | mA |
| | | | -12 | - | 70 | 100 | mA |
| | | | -18 | - | 55 | 80 | mA |
| Standby Power Supply Current | I _{SB} | CE# = V _{IH} or CE2 = V _{IL} Others at V _{IL} or V _{IH} | - | 3 | 20 | mA | |
| | I _{SB1} | CE# ≥ V _{CC} -0.2V or CE2 ≤ 0.2V | Normal | - | 0.6 | 3 | mA |
| | | CE# ≥ V _{CC} -0.2V or CE2 ≤ 0.2V Others at 0.2V or V _{CC} -0.2V | LL | - | 1 | 30 | μA |

Notes:

- V_{IH}(max) = V_{CC} + 3.0V for pulse width less than 10ns.
- V_{IL}(min) = V_{SS} - 3.0V for pulse width less than 10ns.
- Over/Undershoot specifications are characterized, not 100% tested.
- Typical values are included for reference only and are not guaranteed or tested.
Typical valued are measured at V_{CC} = V_{CC}(TYP.) and T_A = 25°C

CAPACITANCE (T_A = 25°C, f = 1.0MHz)

| PARAMETER | SYMBOL | MIN. | MAX. | UNIT |
|--------------------------|------------------|------|------|------|
| Input Capacitance | C _{IN} | - | 6 | pF |
| Input/Output Capacitance | C _{I/O} | - | 8 | pF |

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

| | |
|--|---|
| Input Pulse Levels | 0.2V to V _{CC} - 0.2V |
| Input Rise and Fall Times | 3ns |
| Input and Output Timing Reference Levels | 1.5V |
| Output Load | C _L = 30pF + 1TTL, I _{OH} /I _{OL} = -4mA/8mA |



AC ELECTRICAL CHARACTERISTICS

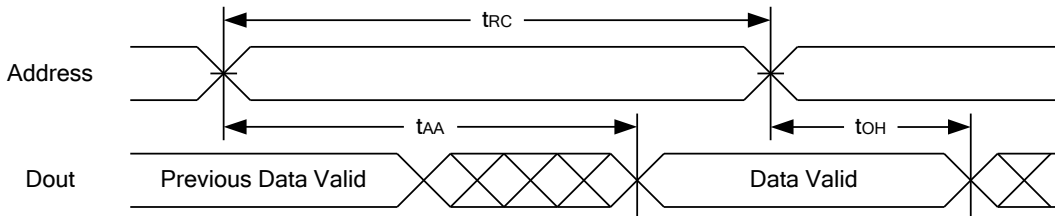
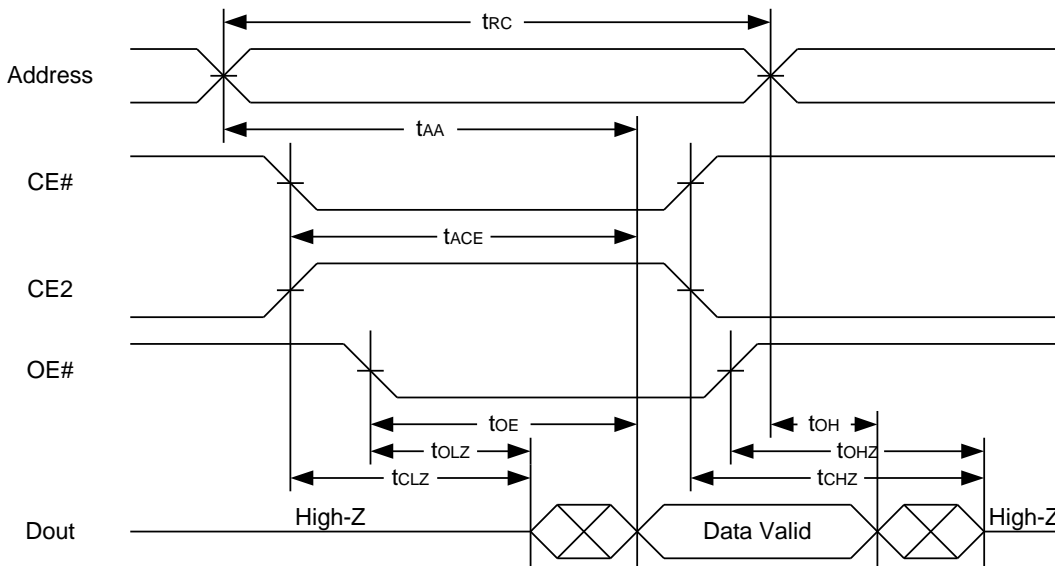
(1) READ CYCLE

| PARAMETER | SYM. | LY61L1024-10 | | LY61L1024-12 | | LY61L1024-18 | | UNIT |
|------------------------------------|--------------------|--------------|------|--------------|------|--------------|------|------|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Read Cycle Time | t _{RC} | 10 | - | 12 | - | 18 | - | ns |
| Address Access Time | t _{AA} | - | 10 | - | 12 | - | 18 | ns |
| Chip Enable Access Time | t _{ACE} | - | 10 | - | 12 | - | 18 | ns |
| Output Enable Access Time | t _{OE} | - | 5 | - | 6 | - | 8 | ns |
| Chip Enable to Output in Low-Z | t _{CLZ} * | 2 | - | 3 | - | 4 | - | ns |
| Output Enable to Output in Low-Z | t _{OLZ} * | 0 | - | 0 | - | 0 | - | ns |
| Chip Disable to Output in High-Z | t _{CHZ} * | - | 5 | - | 6 | - | 8 | ns |
| Output Disable to Output in High-Z | t _{OHZ} * | - | 5 | - | 6 | - | 8 | ns |
| Output Hold from Address Change | t _{OH} | 3 | - | 3 | - | 3 | - | ns |

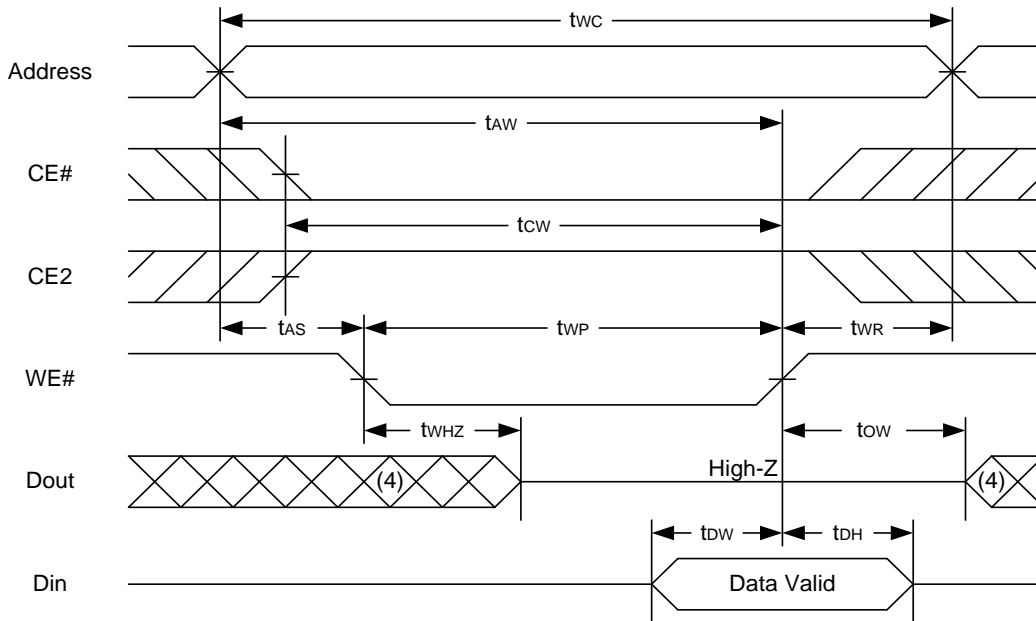
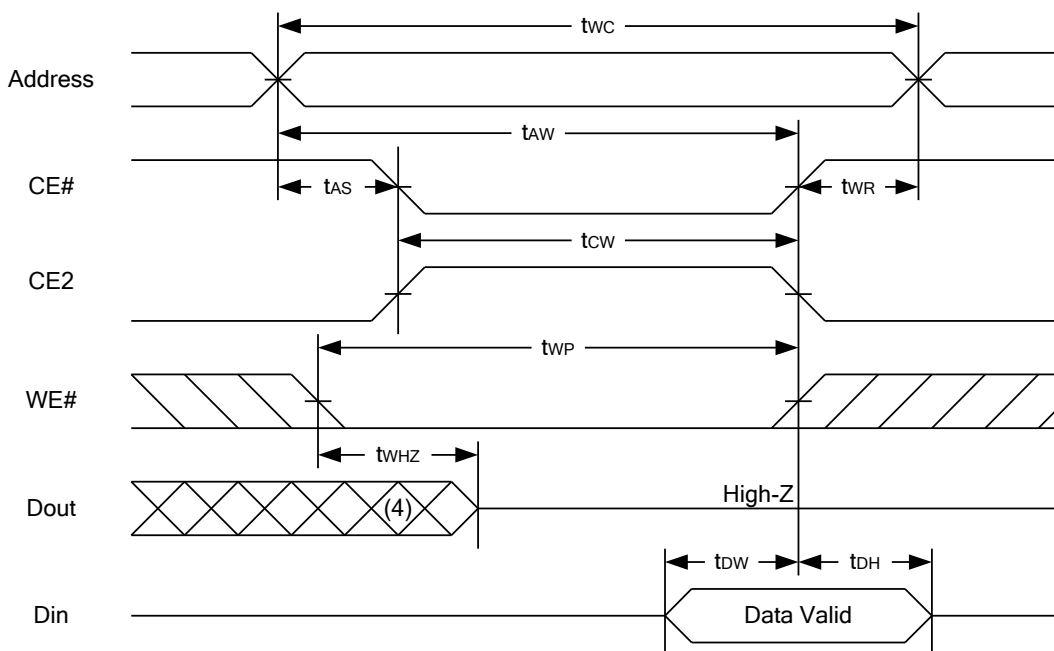
(2) WRITE CYCLE

| PARAMETER | SYM. | LY61L1024-10 | | LY61L1024-12 | | LY61L1024-18 | | UNIT |
|----------------------------------|--------------------|--------------|------|--------------|------|--------------|------|------|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Write Cycle Time | t _{WC} | 10 | - | 12 | - | 18 | - | ns |
| Address Valid to End of Write | t _{AW} | 8 | - | 10 | - | 16 | - | ns |
| Chip Enable to End of Write | t _{CW} | 8 | - | 10 | - | 16 | - | ns |
| Address Set-up Time | t _{AS} | 0 | - | 0 | - | 0 | - | ns |
| Write Pulse Width | t _{WP} | 8 | - | 9 | - | 11 | - | ns |
| Write Recovery Time | t _{WR} | 0 | - | 0 | - | 0 | - | ns |
| Data to Write Time Overlap | t _{DW} | 6 | - | 7 | - | 9 | - | ns |
| Data Hold from End of Write Time | t _{DH} | 0 | - | 0 | - | 0 | - | ns |
| Output Active from End of Write | t _{OW} * | 2 | - | 3 | - | 5 | - | ns |
| Write to Output in High-Z | t _{WHZ} * | - | 6 | - | 7 | - | 9 | ns |

*These parameters are guaranteed by device characterization, but not production tested.

TIMING WAVEFORMS
READ CYCLE 1 (Address Controlled) (1,2)

READ CYCLE 2 (CE# and CE2 and OE# Controlled) (1,3,4,5)

Notes :

1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low, CE2 = high.
3. Address must be valid prior to or coincident with CE# = low, CE2 = high; otherwise t_{AA} is the limiting parameter.
4. t_{CLZ} , t_{OLZ} , t_{CHZ} and t_{OHZ} are specified with $C_L = 5\text{pF}$. Transition is measured $\pm 500\text{mV}$ from steady state.
5. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{OHZ} is less than t_{OLZ} .

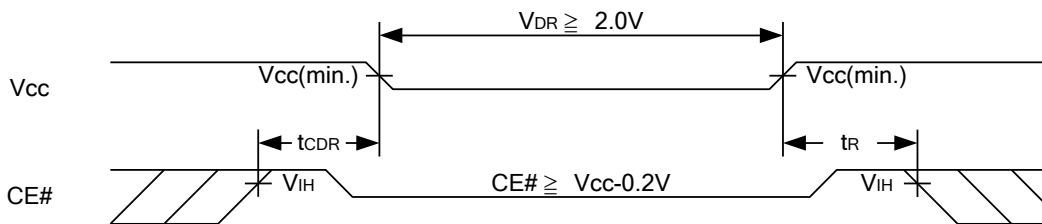
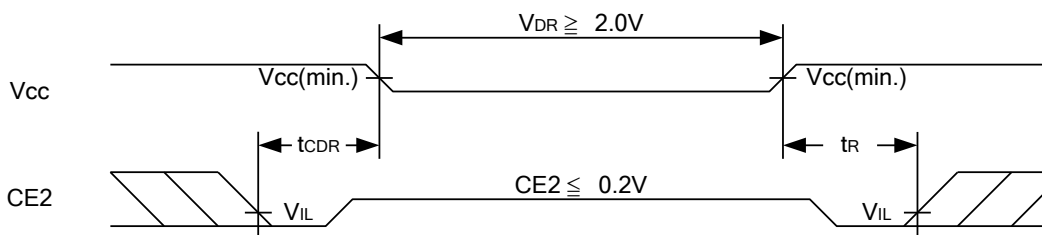
WRITE CYCLE 1 (WE# Controlled) (1,2,4,5)

WRITE CYCLE 2 (CE# and CE2 Controlled) (1,4,5)

Notes :

1. A write occurs during the overlap of a low CE#, high CE2, low WE#.
2. During a WE# controlled write cycle with OE# low, t_{WP} must be greater than $t_{WHZ} + t_{DW}$ to allow the drivers to turn off and data to be placed on the bus.
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the CE# low transition and CE2 high transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
5. t_{OW} and t_{WHZ} are specified with $C_L = 5\text{pF}$. Transition is measured $\pm 500\text{mV}$ from steady state.

DATA RETENTION CHARACTERISTICS

| PARAMETER | SYMBOL | TEST CONDITION | MIN. | TYP. | MAX. | UNIT | |
|-------------------------------------|------------------|---|-------------------|------|-------|------|----|
| V _{CC} for Data Retention | V _{DR} | CE# ≥ V _{CC} - 0.2V or CE2 ≤ 0.2V | 2.0 | - | 3.6 | V | |
| Data Retention Current | I _{DR} | V _{CC} = 2.0V CE# ≥ V _{CC} - 0.2V or CE2 ≤ 0.2V | Normal | - | 0.006 | 2 | mA |
| | | V _{CC} = 2.0V CE# ≥ V _{CC} - 0.2V or CE2 ≤ 0.2V Others at 0.2V or V _{CC} -0.2V | LL | - | 0.5 | 30 | μA |
| Chip Disable to Data Retention Time | t _{CDR} | See Data Retention Waveforms (below) | 0 | - | - | ns | |
| Recovery Time | t _R | | t _{RC} * | - | - | ns | |

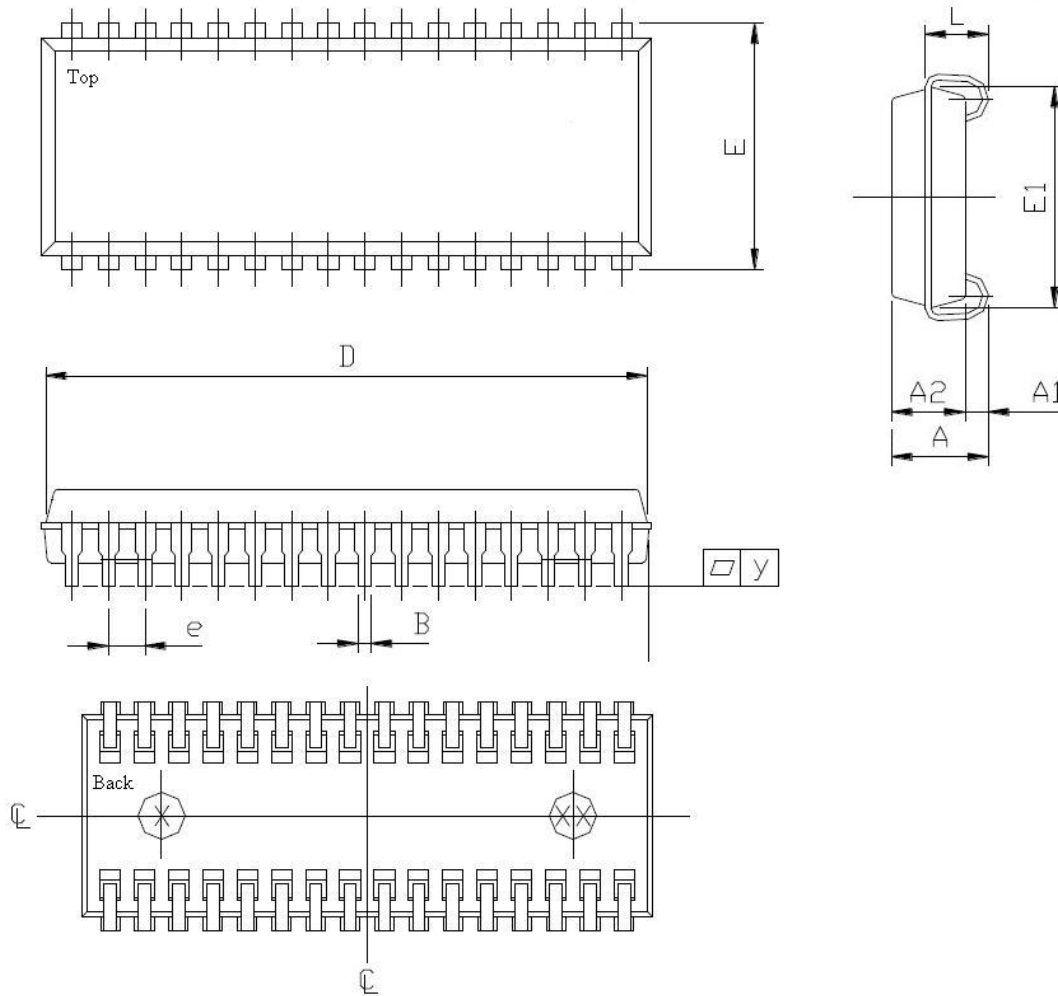
 t_{RC}* = Read Cycle Time

DATA RETENTION WAVEFORM
Low V_{CC} Data Retention Waveform (1) (CE# controlled)

Low V_{CC} Data Retention Waveform (2) (CE2 controlled)


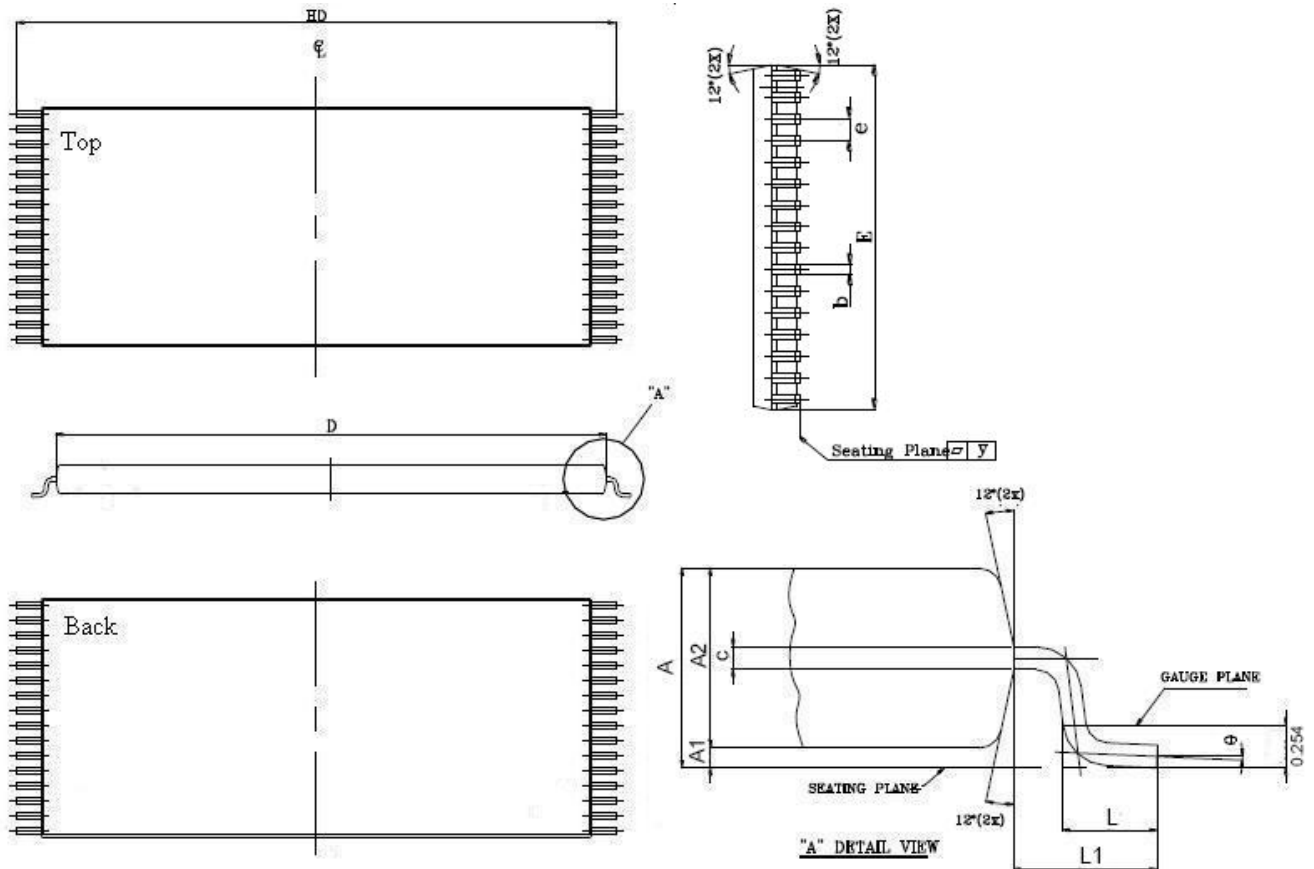


PACKAGE OUTLINE DIMENSION

32-pin 300mil SOJ Package Outline Dimension



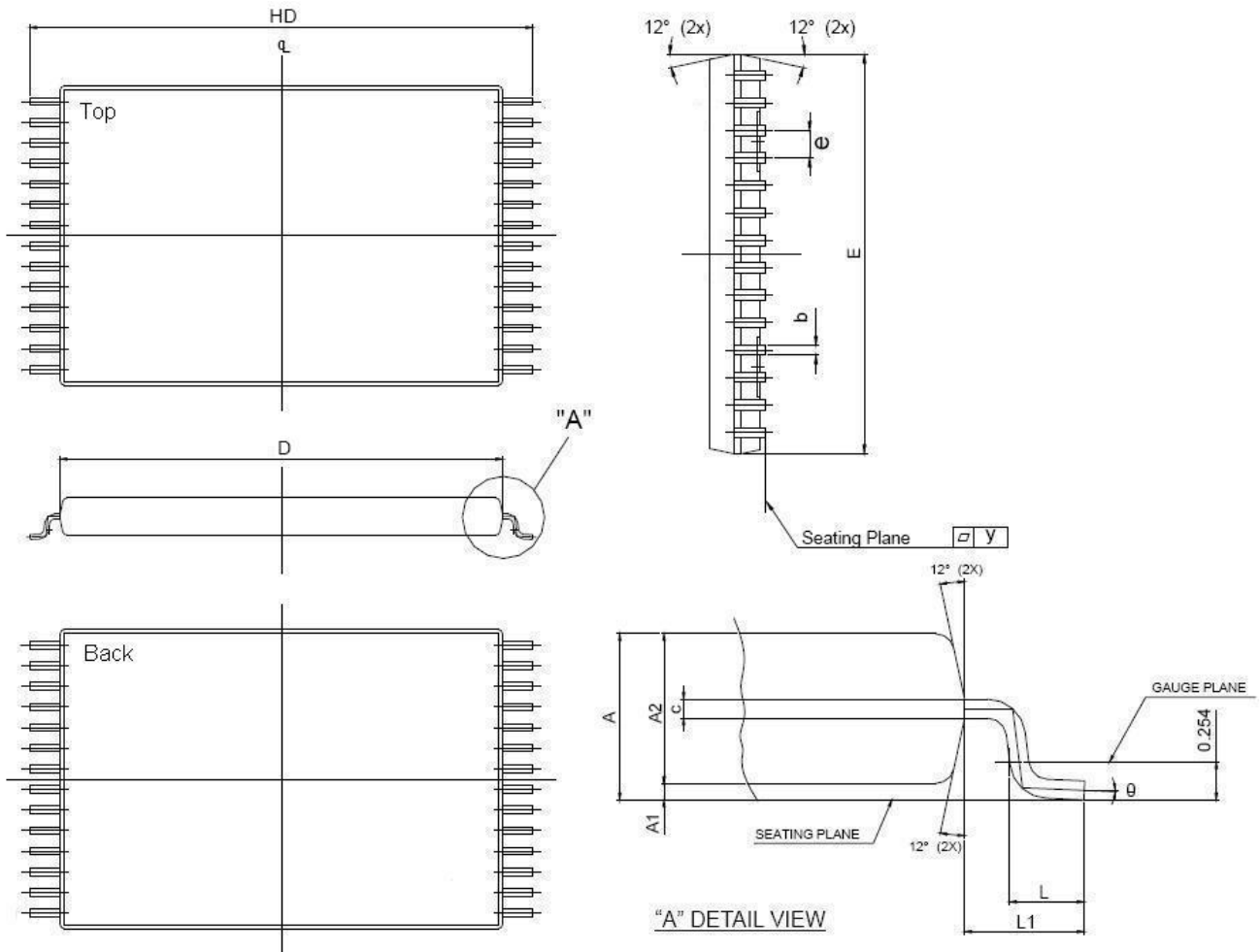
| SYMBOL | UNIT | INCH(BASE) | MM(REF) |
|--------|------|-------------|--------------|
| A | | 0.148(MAX) | 3.759(MAX) |
| A1 | | 0.025(MIN) | 0.635(MIN) |
| A2 | | 0.123(MAX) | 3.124(MAX) |
| B | | 0.018(TYP) | 0.457(TYP) |
| D | | 0.825±0.005 | 20.955±0.127 |
| E | | 0.335(TYP) | 8.509(TYP) |
| E1 | | 0.300±0.005 | 7.620±0.127 |
| e | | 0.050(TYP) | 1.270(TYP) |
| L | | 0.086±0.010 | 2.184±0.254 |
| y | | 0.003(MAX) | 0.076(MAX) |

32-pin 8mm x 20mm TSOP I Package Outline Dimension


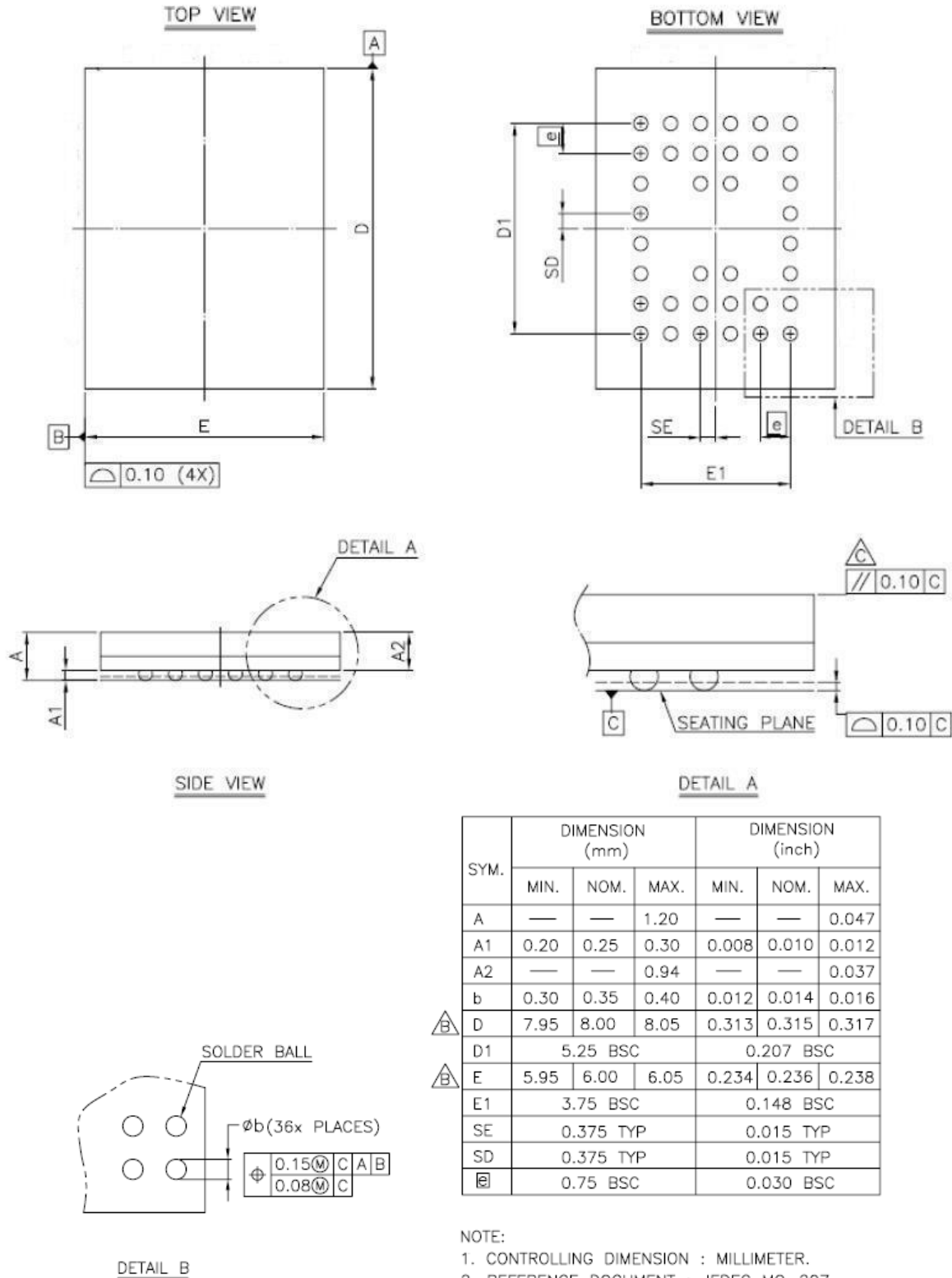
| SYM. | UNIT | INCH(BASE) | MM(REF) |
|------|------|---------------|--------------|
| A | | 0.047 (MAX) | 1.20 (MAX) |
| A1 | | 0.004 ±0.002 | 0.10 ±0.05 |
| A2 | | 0.039 ±0.002 | 1.00 ±0.05 |
| b | | 0.009 ±0.002 | 0.22 ±0.05 |
| c | | 0.006 ±0.002 | 0.155 ±0.055 |
| D | | 0.724 ±0.008 | 18.40 ±0.20 |
| E | | 0.315 ±0.008 | 8.00 ±0.20 |
| e | | 0.020 (TYP) | 0.50 (TYP) |
| HD | | 0.787 ±0.008 | 20.00 ±0.20 |
| L | | 0.024 ±0.004 | 0.60 ±0.10 |
| L1 | | 0.0315 ±0.004 | 0.08 ±0.10 |
| y | | 0.003 (MAX) | 0.08 (MAX) |
| ∅ | | 0°~5° | 0°~5° |



32-pin 8mm x 13.4mm sTSOP Package Outline Dimension



| SYM. | UNIT | INCH(BASE) | MM(REF) |
|------|------|--------------|--------------|
| A | | 0.049 (MAX) | 1.25 (MAX) |
| A1 | | 0.004 ±0.002 | 0.10 ±0.05 |
| A2 | | 0.039 ±0.002 | 1.00 ±0.05 |
| b | | 0.009 ±0.002 | 0.22 ±0.05 |
| c | | 0.006 ±0.002 | 0.155 ±0.055 |
| D | | 0.465 ±0.008 | 11.80 ±0.20 |
| E | | 0.315 ±0.008 | 8.00 ±0.20 |
| e | | 0.020 (TYP) | 0.50 (TYP) |
| HD | | 0.528±0.008 | 13.40 ±0.20. |
| L | | 0.02 ±0.008 | 0.50 ±0.20 |
| L1 | | 0.031 ±0.005 | 0.8 ±0.125 |
| y | | 0.003 (MAX) | 0.076 (MAX) |
| θ | | 0°~5° | 0°~5° |

36-ball 6mm x 8mm TFBGA Package Outline Dimension




ORDERING INFORMATION

| Package Type | Access Time (Speed)(ns) | Power Type | Temperature Range(°C) | Packing Type | Lyontek Item No. |
|------------------------|-------------------------|-----------------|-----------------------|--------------|--------------------|
| 32-pin (300mil) SOJ | 10 | Normal Power | 0°C~70°C | Tube | LY61L1024JL-10 |
| | | | | Tape Reel | LY61L1024JL-10T |
| | | | -40°C~85°C | Tube | LY61L1024JL-10I |
| | | | | Tape Reel | LY61L1024JL-10IT |
| | 12 | Normal Power | 0°C~70°C | Tube | LY61L1024JL-12 |
| | | | | Tape Reel | LY61L1024JL-12T |
| | | | -40°C~85°C | Tube | LY61L1024JL-12I |
| | | | | Tape Reel | LY61L1024JL-12IT |
| | 18 | Ultra Low Power | 0°C~70°C | Tube | LY61L1024JL-18LL |
| | | | | Tape Reel | LY61L1024JL-18LLT |
| | | | -40°C~85°C | Tube | LY61L1024JL-18LLI |
| | | | | Tape Reel | LY61L1024JL-18LLIT |



ORDERING INFORMATION

| Package Type | Access Time (Speed)(ns) | Power Type | Temperature Range(°C) | Packing Type | Lyontek Item No. |
|----------------------------------|-------------------------|-----------------|-----------------------|--------------|--------------------|
| 32-pin (8mm x 20mm) TSOP I | 10 | Normal Power | 0°C~70°C | Tray | LY61L1024LL-10 |
| | | | | Tape Reel | LY61L1024LL-10T |
| | | | -40°C~85°C | Tray | LY61L1024LL-10I |
| | | | | Tape Reel | LY61L1024LL-10IT |
| | 12 | Normal Power | 0°C~70°C | Tray | LY61L1024LL-12 |
| | | | | Tape Reel | LY61L1024LL-12T |
| | | | -40°C~85°C | Tray | LY61L1024LL-12I |
| | | | | Tape Reel | LY61L1024LL-12IT |
| | 18 | Ultra Low Power | 0°C~70°C | Tray | LY61L1024LL-18LL |
| | | | | Tape Reel | LY61L1024LL-18LLT |
| | | | -40°C~85°C | Tray | LY61L1024LL-18LLI |
| | | | | Tape Reel | LY61L1024LL-18LLIT |

ORDERING INFORMATION

| Package Type | Access Time (Speed)(ns) | Power Type | Temperature Range(°C) | Packing Type | Lyontek Item No. |
|-----------------------------------|-------------------------|-----------------|-----------------------|--------------|--------------------|
| 32-pin (8mm x 13.4mm) sTSOP | 10 | Normal Power | 0°C~70°C | Tray | LY61L1024RL-10 |
| | | | | Tape Reel | LY61L1024RL-10T |
| | | | -40°C~85°C | Tray | LY61L1024RL-10I |
| | | | | Tape Reel | LY61L1024RL-10IT |
| | 12 | Normal Power | 0°C~70°C | Tray | LY61L1024RL-12 |
| | | | | Tape Reel | LY61L1024RL-12T |
| | | | -40°C~85°C | Tray | LY61L1024RL-12I |
| | | | | Tape Reel | LY61L1024RL-12IT |
| | 18 | Ultra Low Power | 0°C~70°C | Tray | LY61L1024RL-18LL |
| | | | | Tape Reel | LY61L1024RL-18LLT |
| | | | -40°C~85°C | Tray | LY61L1024RL-18LLI |
| | | | | Tape Reel | LY61L1024RL-18LLIT |



ORDERING INFORMATION

| Package Type | Access Time (Speed)(ns) | Power Type | Temperature Range(°C) | Packing Type | Lyontek Item No. |
|---------------------------------|-------------------------|-----------------|-----------------------|--------------|--------------------|
| 36-ball (6mm x 8mm) TFBGA | 10 | Normal Power | 0°C~70°C | Tray | LY61L1024GL-10 |
| | | | | Tape Reel | LY61L1024GL-10T |
| | | | -40°C~85°C | Tray | LY61L1024GL-10I |
| | | | | Tape Reel | LY61L1024GL-10IT |
| | 12 | Normal Power | 0°C~70°C | Tray | LY61L1024GL-12 |
| | | | | Tape Reel | LY61L1024GL-12T |
| | | | -40°C~85°C | Tray | LY61L1024GL-12I |
| | | | | Tape Reel | LY61L1024GL-12IT |
| | 18 | Ultra Low Power | 0°C~70°C | Tray | LY61L1024GL-18LL |
| | | | | Tape Reel | LY61L1024GL-18LLT |
| | | | -40°C~85°C | Tray | LY61L1024GL-18LLI |
| | | | | Tape Reel | LY61L1024GL-18LLIT |



Lyontek Inc.

LY61L1024

Rev. 2.8

128K X 8 BIT HIGH SPEED CMOS SRAM

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