



REVISION HISTORY

<u>Revision</u>	<u>Description</u>	<u>Issue Date</u>
Rev. 1.0	Initial Issue	Jul.25.2004
Rev. 1.1	Deleted I _{CC1} Spec. Revised TRUTH TABLE	Sep.21.2004
Rev. 1.2	Deleted DATA RETENTION WAVEFORM (2) (UB# & LB# controlled)	Jun.20.2005
Rev. 1.3	Revised the typo in page 1	Feb.13.2006
Rev. 1.4	Added PKG Type : 48-ball 6mm x 8mm TFBGA Revised TEST CONDITION of I _{SB1} /I _{DR}	Jun.13.2007
Rev. 1.5	Added I Grade Spec. Revised V _{TERM} to V _{T1} and V _{T2}	Feb.04.2008
Rev. 1.6	Added -20ns Spec.	Mar.31.2008
Rev. 1.7	Added LL Spec.	Aug.07.2008
Rev. 1.8	Revised TEST CONDITION of I _{SB} Revised FEATURES & ORDERING INFORMATION Lead free and green package available to Green package available Deleted T _{SOLDER} in ABSOLUTE MAXIMUM RATINGS Added packing type in ORDERING INFORMATION	Apr.17.2009
Rev. 1.9	Revised PACKAGE OUTLINE DIMENSION in page 11	May.06.2010
Rev. 2.0	Revised ORDERING INFORMATION in page 12	Aug.30.2010
Rev. 2.1	Revised TRUTH TABLE in page 4	Dec.14.2015
Rev. 2.2	Correct ORDERING INFORMATION typo.	May.20.2016
Rev. 2.3	Revised PIN DESCRIPTION in page 2 Deleted -8/20ns Spec. Deleted Power Type in ORDERING INFORMATION Deleted DC ELECTRICAL CHARACTERISTICS Notes : 6. 50μA for special request. In page 5 Deleted WRITE CYCLE Notes : 1. WE#,CE#, LB#, UB# must be high during all address transitions. In page 9	Dec.13.2016
Rev. 3.0	Revised ORDERING INFORMATION in page 13 &14	Jun.11.2026



FEATURES

- Fast access time : 10/12/15ns
- Low power consumption:
Operating current : 105/95/85mA (TYP.)
Standby current : 0.6mA (TYP.)
- Single 3.3V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data byte control : LB# (DQ0 ~ DQ7)
UB# (DQ8 ~ DQ15)
- Data retention voltage : 2.0V (MIN.)
- **Green package available**
- Package : 44-pin 400 mil TSOP II
48-ball 6mm x 8mm TFBGA

GENERAL DESCRIPTION

The LY61L6416 is a 1,048,576-bit low power CMOS static random access memory organized as 65,536 words by 16 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

The LY61L6416 is well designed for low power application, and particularly well suited for battery back-up nonvolatile memory application.

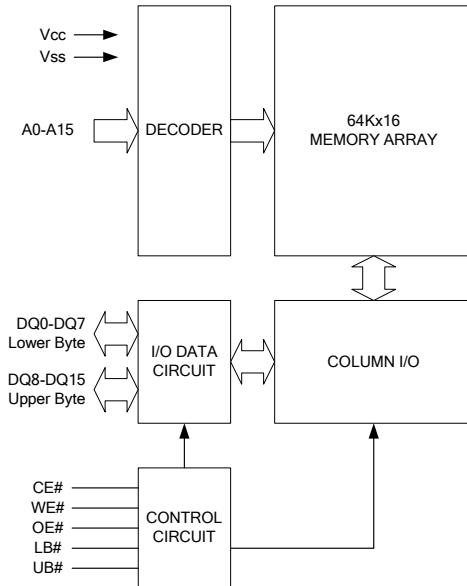
The LY61L6416 operates from a single power supply of 3.3V and all inputs and outputs are fully TTL compatible

PRODUCT FAMILY

Product Family	Operating Temperature	V _{CC} Range	Speed	Power Dissipation	
				Standby(I _{SB1} , TYP.)	Operating(I _{CC} , TYP.)
LY61L6416	0 ~ 70°C	3.15 ~ 3.6V	10ns	0.6mA	105mA
LY61L6416	0 ~ 70°C	3.0 ~ 3.6V	12/15ns	0.6mA	95/85mA
LY61L6416(E)	-20 ~ 80°C	3.15 ~ 3.6V	10ns	0.6mA	105mA
LY61L6416(E)	-20 ~ 80°C	3.0 ~ 3.6V	12/15ns	0.6mA	95/85mA
LY61L6416(I)	-40 ~ 85°C	3.15 ~ 3.6V	10ns	0.6mA	105mA
LY61L6416(I)	-40 ~ 85°C	3.0 ~ 3.6V	12/15ns	0.6mA	95/85mA



FUNCTIONAL BLOCK DIAGRAM

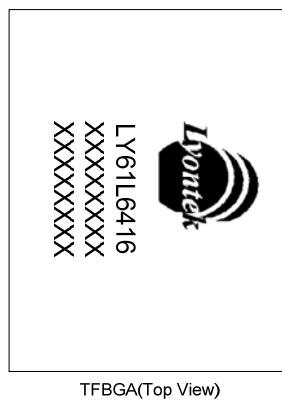
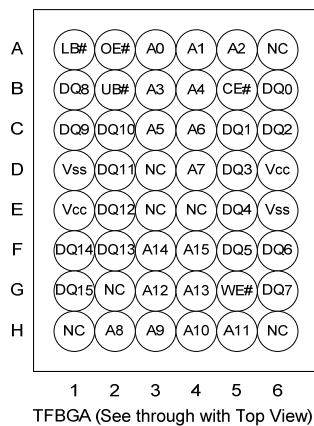
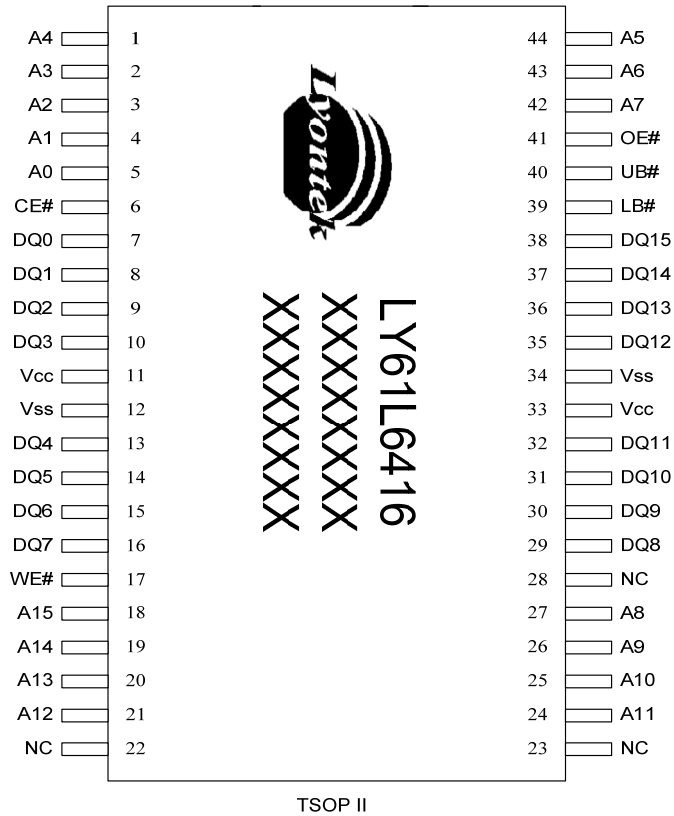


PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A15	Address Inputs
DQ0 - DQ15	Data Inputs/Outputs
CE#	Chip Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
LB#	Lower Byte Control
UB#	Upper Byte Control
V _{CC}	Power Supply
V _{SS}	Ground
NC	No Connection



PIN CONFIGURATION





ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on V _{CC} relative to V _{SS}	V _{T1}	-0.5 to 4.6	V
Voltage on any other pin relative to V _{SS}	V _{T2}	-0.5 to V _{CC} +0.5	V
Operating Temperature	T _A	0 to 70(C grade)	°C
		-20 to 80(E grade)	
		-40 to 85(I grade)	
Storage Temperature	T _{STG}	-65 to 150	°C
Power Dissipation	P _D	1	W
DC Output Current	I _{OUT}	50	mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE#	OE#	WE#	LB#	UB#	I/O OPERATION		SUPPLY CURRENT
						DQ0 - DQ7	DQ8 - DQ15	
Standby	H	X	X	X	X	High-Z	High-Z	I _{SB} , I _{SB1}
Output Disable	L	H	H	X	X	High-Z	High-Z	I _{CC}
	L	X	X	H	H	High-Z	High-Z	
Read	L	L	H	L	H	D _{OUT}	High-Z	I _{CC}
	L	L	H	H	L	High-Z	D _{OUT}	
	L	L	H	L	L	D _{OUT}	D _{OUT}	
Write	L	X	L	L	H	D _{IN}	High-Z	I _{CC}
	L	X	L	H	L	High-Z	D _{IN}	
	L	X	L	L	L	D _{IN}	D _{IN}	

Note: H = V_{IH}, L = V_{IL}, X = Don't care.



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.* ⁴	MAX.	UNIT
Supply Voltage	V _{CC}		-10	3.15	3.3	3.6	V
			-12/15	3.0	3.3	3.6	V
Input High Voltage	V _{IH} * ¹			2.0	-	V _{CC} +0.3	V
Input Low Voltage	V _{IL} * ²			- 0.3	-	0.8	V
Input Leakage Current	I _{LI}	V _{CC} ≥ V _{IN} ≥ V _{SS}		- 1	-	1	μA
Output Leakage Current	I _{LO}	V _{CC} ≥ V _{OUT} ≥ V _{SS} , Output Disabled		- 1	-	1	μA
Output High Voltage	V _{OH}	I _{OH} = -4mA		2.4	-	-	V
Output Low Voltage	V _{OL}	I _{OL} = 8mA		-	-	0.4	V
Average Operating Power supply Current	I _{CC}	Cycle time = MIN. CE# = V _{IL} , I _{I/O} = 0mA Other pins at V _{IH} or V _{IL}	-10	-	105	120	mA
			-12	-	95	100	mA
			-15	-	85	90	mA
Standby Power Supply Current	I _{SB}	CE# = V _{IH} , other pins at V _{IH} or V _{IL}		-	3	10	mA
	I _{SB1}	CE# ≥ V _{CC} - 0.2V, Others at 0.2V or V _{CC} - 0.2V		-	0.6	3* ⁵	mA

Notes:

- $V_{IH}(\max) = V_{CC} + 3.0V$ for pulse width less than 10ns.
- $V_{IL}(\min) = V_{SS} - 3.0V$ for pulse width less than 10ns.
- Over/Undershoot specifications are characterized, not 100% tested.
- Typical values are included for reference only and are not guaranteed or tested.
Typical values are measured at $V_{CC} = V_{CC}(\text{TYP.})$ and $T_A = 25^\circ C$
- 1mA for special request

CAPACITANCE ($T_A = 25^\circ C$, $f = 1.0MHz$)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Input Capacitance	C_{IN}	-	6	pF
Input/Output Capacitance	$C_{I/O}$	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0.2V to $V_{CC} - 0.2V$
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	$C_L = 30pF + 1TTL$, $I_{OH}/I_{OL} = -4mA/8mA$



AC ELECTRICAL CHARACTERISTICS

(1) READ CYCLE

PARAMETER	SYM.	LY61L6416-10		LY61L6416-12		LY61L6416-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t _{RC}	10	-	12	-	15	-	ns
Address Access Time	t _{AA}	-	10	-	12	-	15	ns
Chip Enable Access Time	t _{ACE}	-	10	-	12	-	15	ns
Output Enable Access Time	t _{OE}	-	5	-	6	-	7	ns
Chip Enable to Output in Low-Z	t _{CLZ} *	2	-	3	-	4	-	ns
Output Enable to Output in Low-Z	t _{OLZ} *	0	-	0	-	0	-	ns
Chip Disable to Output in High-Z	t _{CHZ} *	-	5	-	6	-	7	ns
Output Disable to Output in High-Z	t _{OHZ} *	-	5	-	6	-	7	ns
Output Hold from Address Change	t _{OH}	3	-	3	-	3	-	ns
LB#, UB# Access Time	t _{BA}	-	5	-	6	-	7	ns
LB#, UB# to High-Z Output	t _{BHZ} *	-	5	-	6	-	7	ns
LB#, UB# to Low-Z Output	t _{BLZ} *	0	-	0	-	0	-	ns

(2) WRITE CYCLE

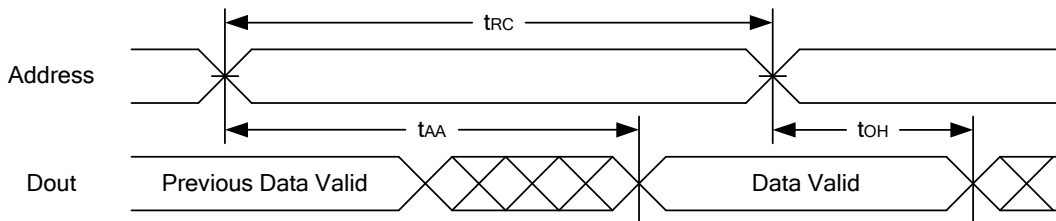
PARAMETER	SYM.	LY61L6416-10		LY61L6416-12		LY61L6416-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t _{WC}	10	-	12	-	15	-	ns
Address Valid to End of Write	t _{AW}	8	-	10	-	12	-	ns
Chip Enable to End of Write	t _{CW}	8	-	10	-	12	-	ns
Address Set-up Time	t _{AS}	0	-	0	-	0	-	ns
Write Pulse Width	t _{WP}	8	-	9	-	10	-	ns
Write Recovery Time	t _{WR}	0	-	0	-	0	-	ns
Data to Write Time Overlap	t _{DW}	6	-	7	-	8	-	ns
Data Hold from End of Write Time	t _{DH}	0	-	0	-	0	-	ns
Output Active from End of Write	t _{OW} *	2	-	3	-	4	-	ns
Write to Output in High-Z	t _{WHZ} *	-	6	-	7	-	8	ns
LB#, UB# Valid to End of Write	t _{BW}	8	-	10	-	12	-	ns

*These parameters are guaranteed by device characterization, but not production tested.

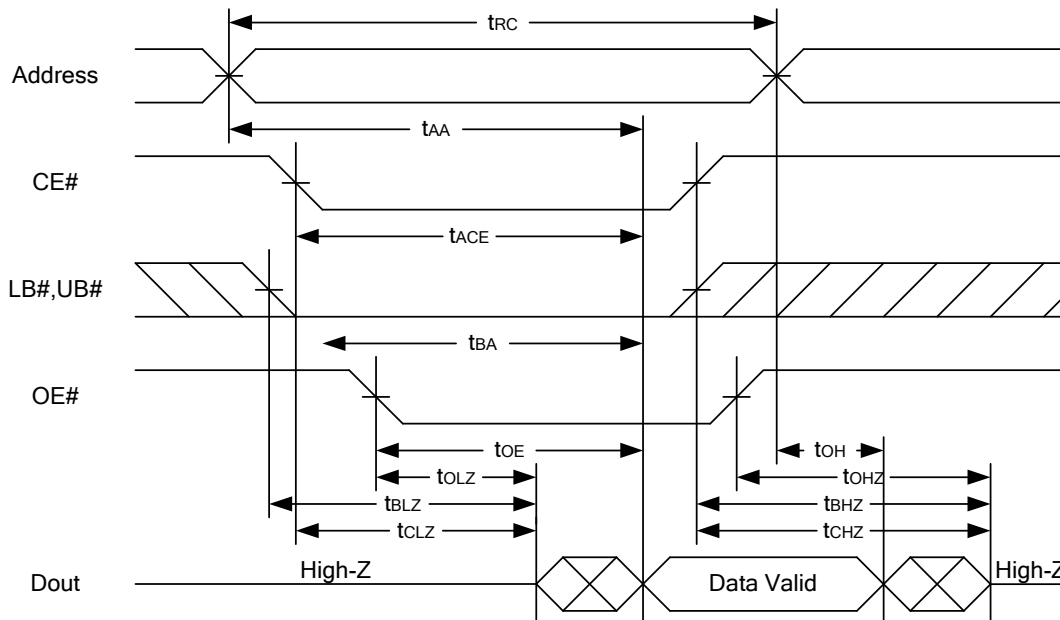


TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)



READ CYCLE 2 (CE# and OE# Controlled) (1,3,4,5)

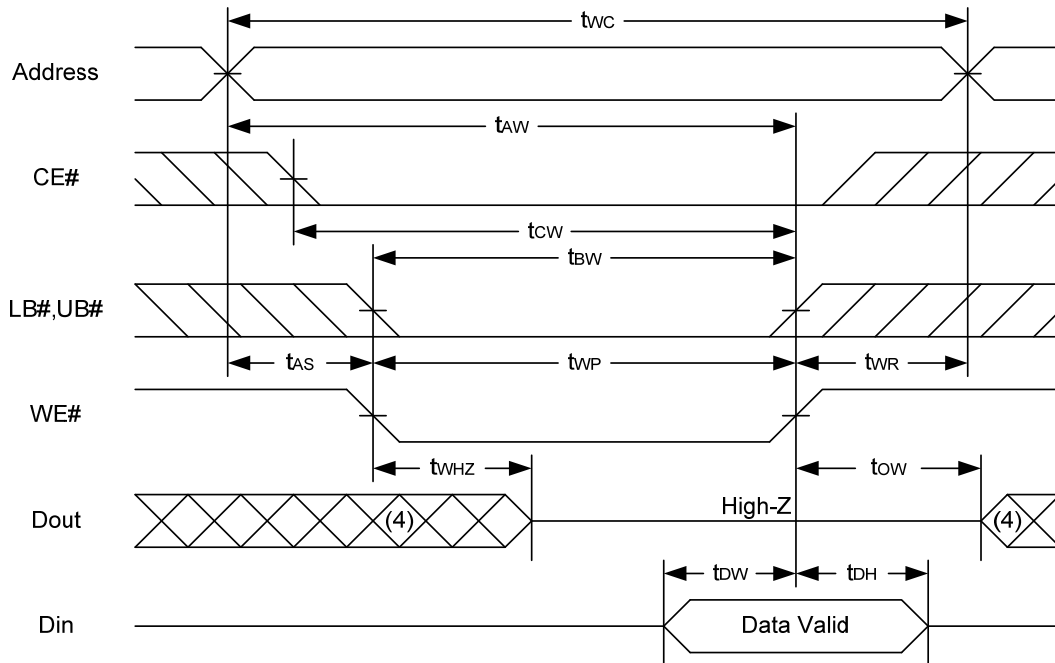


Notes :

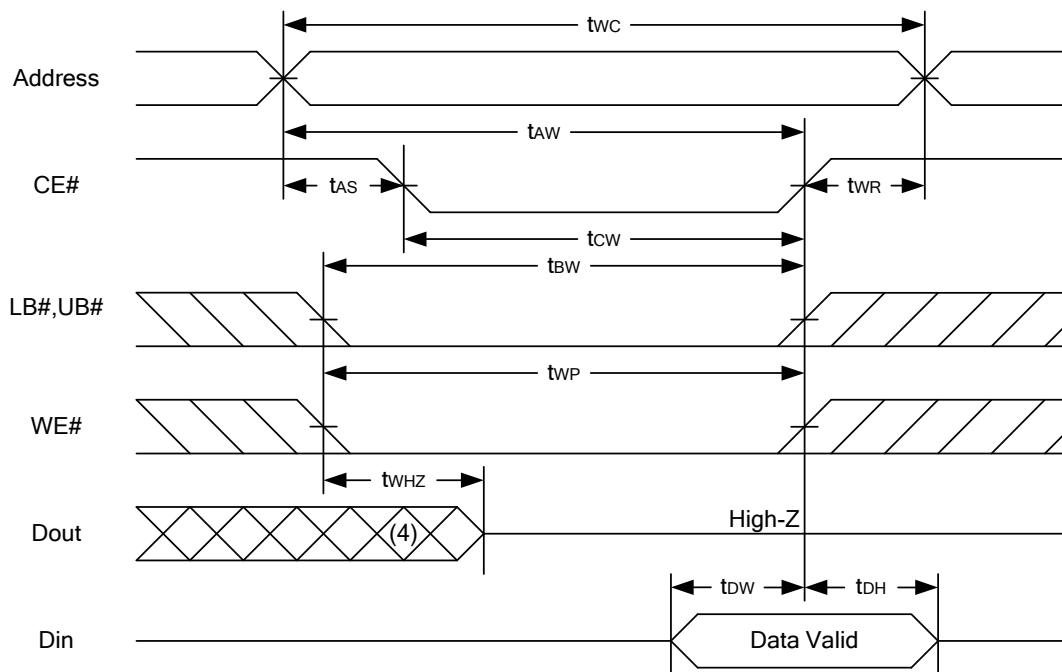
1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low, LB# or UB# = low.
3. Address must be valid prior to or coincident with CE# = low, LB# or UB# = low transition; otherwise t_{AA} is the limiting parameter.
4. t_{CLZ} , t_{BLZ} , t_{OLZ} , t_{CHZ} , t_{BHZ} and t_{OHZ} are specified with $C_L = 5pF$. Transition is measured $\pm 500mV$ from steady state.
5. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{BHZ} is less than t_{BLZ} , t_{OHZ} is less than t_{OLZ} .



WRITE CYCLE 1 (WE# Controlled) (1,2,4,5)

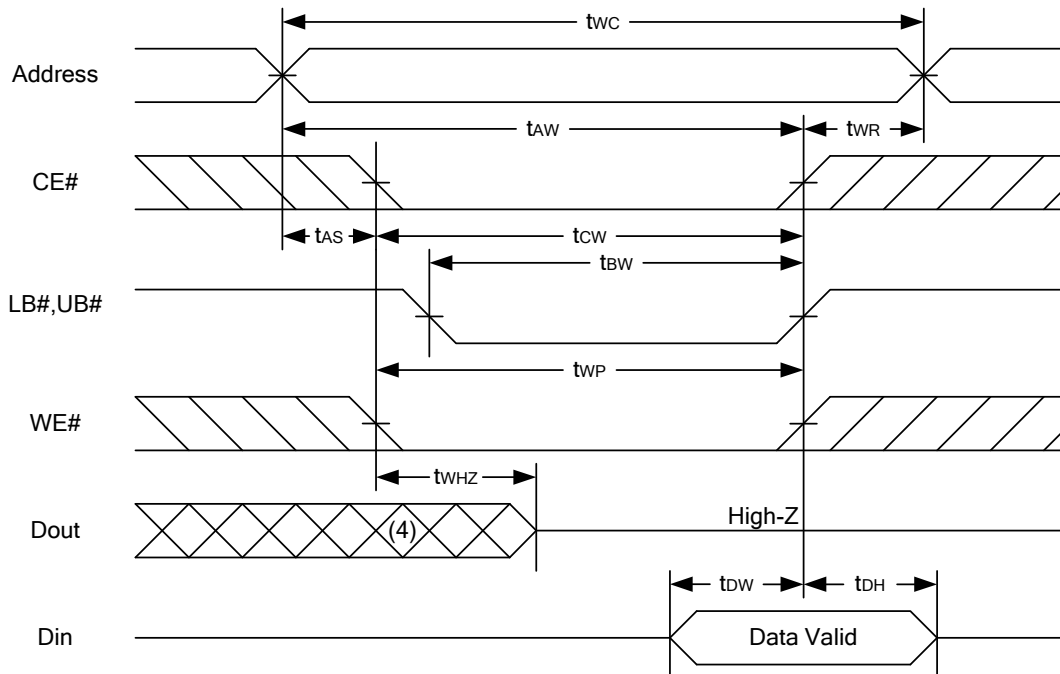


WRITE CYCLE 2 (CE# Controlled) (1,4,5)





WRITE CYCLE 3 (LB#,UB# Controlled) (1,4,5)



Notes :

1. A write occurs during the overlap of a low CE#, low WE#, LB# or UB# = low.
2. During a WE# controlled write cycle with OE# low, t_{WP} must be greater than $t_{WHZ} + t_{DW}$ to allow the drivers to turn off and data to be placed on the bus.
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the CE#, LB#, UB# low transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
5. t_{OW} and t_{WHZ} are specified with $C_L = 5\text{pF}$. Transition is measured $\pm 500\text{mV}$ from steady state.

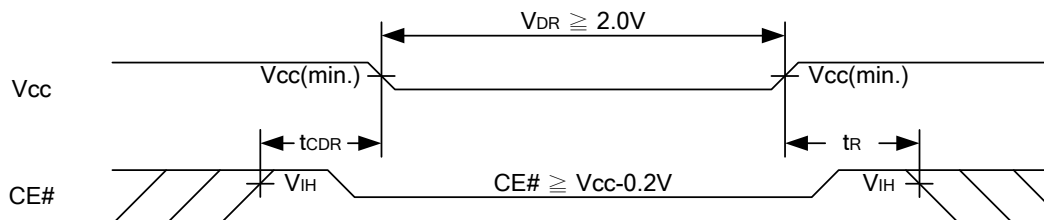


DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
V _{CC} for Data Retention	V _{DR}	CE# $\geq$ V _{CC} - 0.2V	2.0	-	3.6	V
Data Retention Current	I _{DR}	V _{CC} = 2.0V, CE# $\geq$ V _{CC} - 0.2V Others at 0.2V or V _{CC} - 0.2V	-	0.4	2	mA
Chip Disable to Data Retention Time	t _{CDR}	See Data Retention Waveforms (below)	0	-	-	ns
Recovery Time	t _R		t _{RC} *	-	-	ns

t_{RC}* = Read Cycle Time

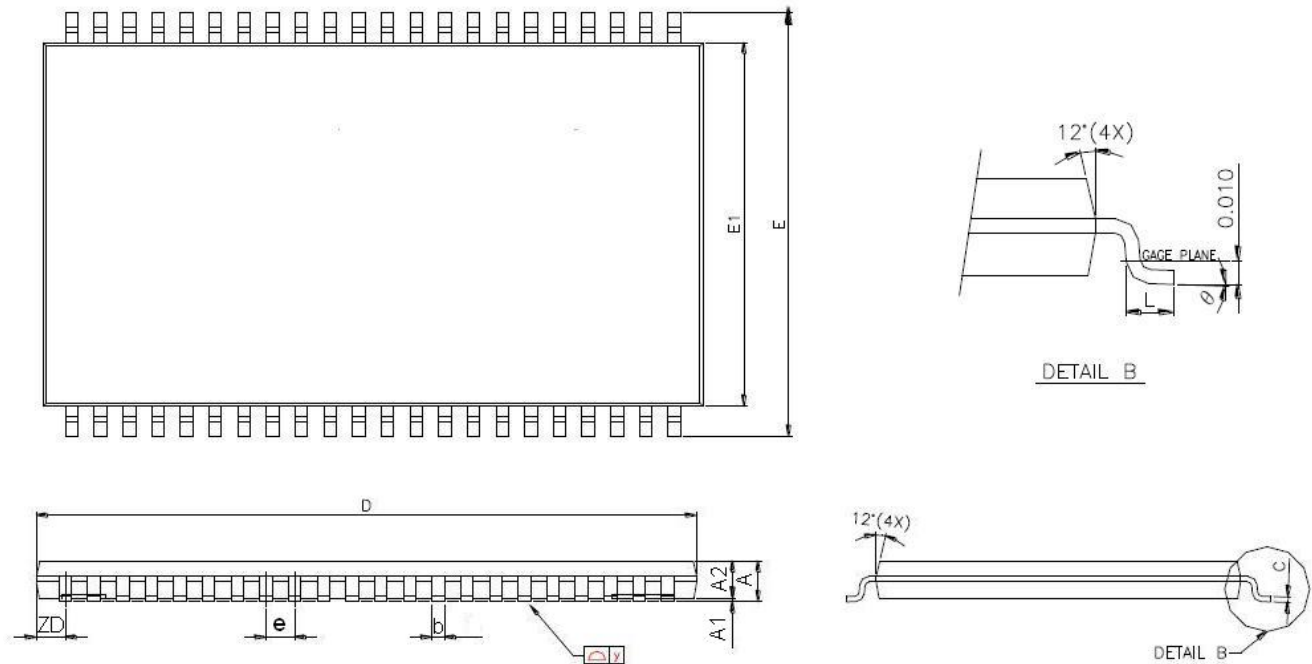
DATA RETENTION WAVEFORM





PACKAGE OUTLINE DIMENSION

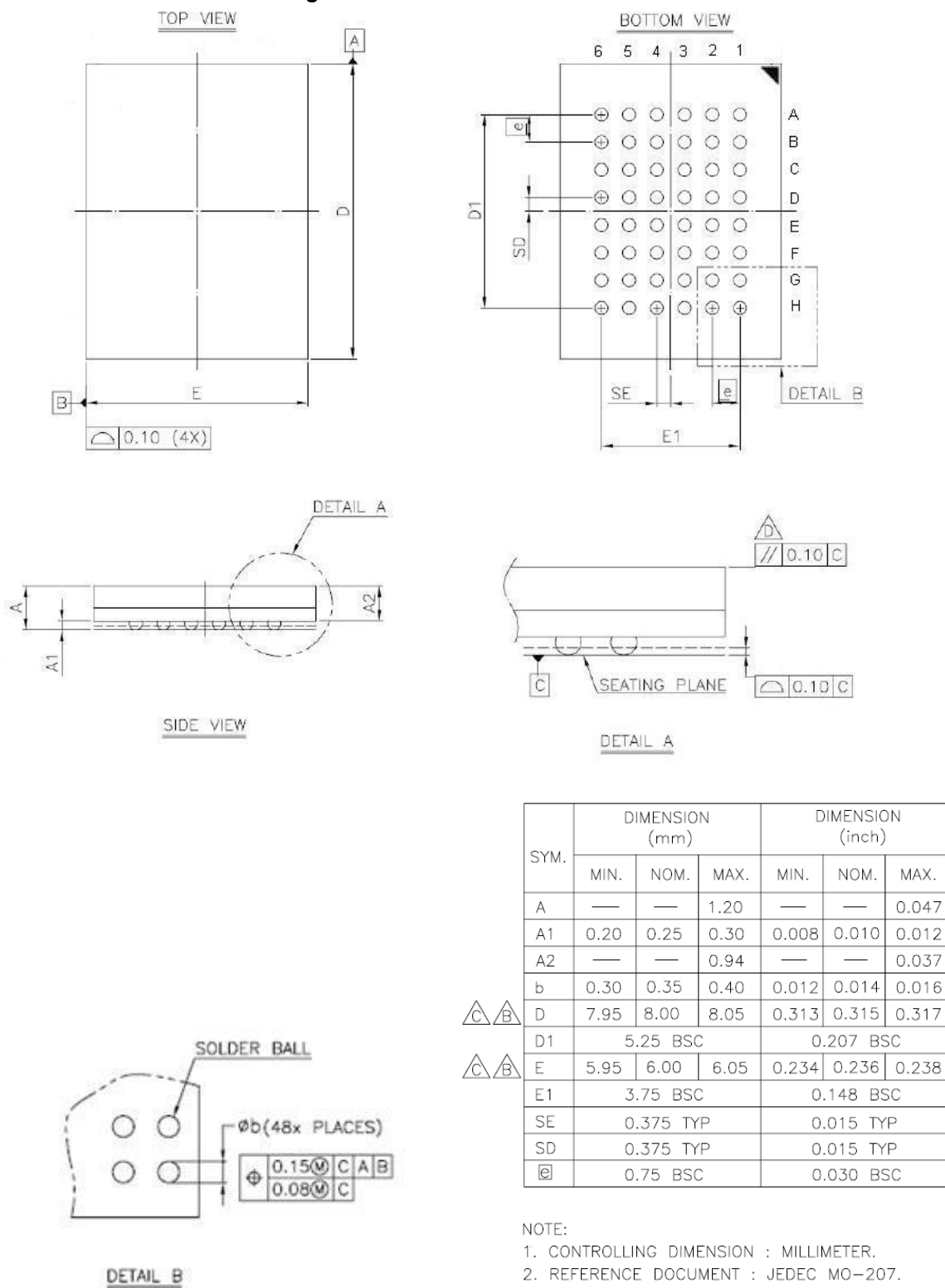
44-pin 400mil TSOP II Package Outline Dimension



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN MILS		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	-	-	1.20	-	-	47.2
A1	0.05	0.10	0.15	2.0	3.9	5.9
A2	0.95	1.00	1.05	37.4	39.4	41.3
b	0.30	-	0.45	11.8	-	17.7
c	0.12	-	0.21	4.7	-	8.3
D	18.212	18.415	18.618	717	725	733
E	11.506	11.760	12.014	453	463	473
E1	9.957	10.160	10.363	392	400	408
e	-	0.800	-	-	31.5	-
L	0.40	0.50	0.60	15.7	19.7	23.6
ZD	-	0.805	-	-	31.7	-
y	-	-	0.076	-	-	3
θ	0°	3°	6°	0°	3°	6°



48-ball 6mm × 8mm TFBGA Package Outline Dimension



**ORDERING INFORMATION****[Production Status: EOL]**

Package Type	Access Time (Speed)(ns)	Temperature Range(°C)	Packing Type	EOL Lyontek Item	Substitute Lyontek Item
44-pin (400mil) TSOP II	10	0°C~70°C	Tray	LY61L6416ML-10	LY61L12816AML-10
			Tape Reel	LY61L6416ML-10T	LY61L12816AML -10T
		-20°C~80°C	Tray	LY61L6416ML-10E	LY61L12816AML -10E
			Tape Reel	LY61L6416ML-10ET	LY61L12816AML -10ET
		-40°C~85°C	Tray	LY61L6416ML-10I	LY61L12816AML -10I
			Tape Reel	LY61L6416ML-10IT	LY61L12816AML -10IT
	12	0°C~70°C	Tray	LY61L6416ML-12	LY61L12816AML -12
			Tape Reel	LY61L6416ML-12T	LY61L12816AML -12T
		-20°C~80°C	Tray	LY61L6416ML-12E	LY61L12816AML -12E
			Tape Reel	LY61L6416ML-12ET	LY61L12816AML -12ET
		-40°C~85°C	Tray	LY61L6416ML-12I	LY61L12816AML -12I
			Tape Reel	LY61L6416ML-12IT	LY61L12816AML -12IT
	15	0°C~70°C	Tray	LY61L6416ML-15	LY61L12816AML -15
			Tape Reel	LY61L6416ML-15T	LY61L12816AML -15T
		-20°C~80°C	Tray	LY61L6416ML-15E	LY61L12816AML -15E
			Tape Reel	LY61L6416ML-15ET	LY61L12816AML -15ET
		-40°C~85°C	Tray	LY61L6416ML-15I	LY61L12816AML -15I
			Tape Reel	LY61L6416ML-15IT	LY61L12816AML -15IT



ORDERING INFORMATION

[Production Status: **EOL**]

Package Type	Access Time (Speed)(ns)	Temperature Range(°C)	Packing Type	EOL Lyontek Item	Substitute Lyontek Item
48-ball (6mmx8mm) TFBGA	10	0°C~70°C	Tray	LY61L6416GL-10	LY61L12816AGL-10
			Tape Reel	LY61L6416GL-10T	LY61L12816AGL-10T
		-20°C~80°C	Tray	LY61L6416GL-10E	LY61L12816AGL-10E
			Tape Reel	LY61L6416GL-10ET	LY61L12816AGL-10ET
		-40°C~85°C	Tray	LY61L6416GL-10I	LY61L12816AGL-10I
			Tape Reel	LY61L6416GL-10IT	LY61L12816AGL-10IT
	12	0°C~70°C	Tray	LY61L6416GL-12	LY61L12816AGL-12
			Tape Reel	LY61L6416GL-12T	LY61L12816AGL-12T
		-20°C~80°C	Tray	LY61L6416GL-12E	LY61L12816AGL-12E
			Tape Reel	LY61L6416GL-12ET	LY61L12816AGL-12ET
		-40°C~85°C	Tray	LY61L6416GL-12I	LY61L12816AGL-12I
			Tape Reel	LY61L6416GL-12IT	LY61L12816AGL-12IT
	15	0°C~70°C	Tray	LY61L6416GL-15	LY61L12816AGL-15
			Tape Reel	LY61L6416GL-15T	LY61L12816AGL-15T
		-20°C~80°C	Tray	LY61L6416GL-15E	LY61L12816AGL-15E
			Tape Reel	LY61L6416GL-15ET	LY61L12816AGL-15ET
		-40°C~85°C	Tray	LY61L6416GL-15I	LY61L12816AGL-15I
			Tape Reel	LY61L6416GL-15IT	LY61L12816AGL-15IT



Lyontek Inc.

LY61L6416

Rev. 3.0

64K X 16 BITS HIGH SPEED CMOS SRAM

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