



REVISION HISTORY

<u>Revision</u>	<u>Description</u>	<u>Issue Date</u>
Rev. 1.0.	Initial Issue	Jul.25.2004
Rev. 2.0.	Revised Vcc Range(Vcc=4.5~5.5V => 2.7~5.5V)	May.4.2005
Rev. 2.1.	Revised I _{SB1}	May.13.2005
Rev. 2.2	Adding PKG type : skinny P-DIP	Aug.29.2005
Rev. 2.3	Revised V _{IH} (min)=2.4V, V _{IL} (max)=0.6V	Feb.24.2006
Rev. 2.4	Revised V _{IH} (min)=2.4V, V _{IL} (max)=0.6V (V _{CC} =2.7~3.6V) V _{IH} (min)=2.4V, V _{IL} (max)=0.8V (V _{CC} =4.5~5.5V)	Jul.31.2006
Rev. 2.5	Revised STSOP <u>Package Outline Dimension</u>	Mar.26.2008
Rev. 2.6	Added SL grade Added I _{SB1} /I _{DR} values when T _A = 25°C and T _A = 40°C Revised <u>FEATURES</u> & <u>ORDERING INFORMATION</u> <u>Lead free and green</u> <u>package available</u> to <u>Green package available</u> Added packing type in <u>ORDERING INFORMATION</u> Revised I _{SB1} (MAX) Revised V _{TERM} to V _{T1} and V _{T2} Revised Test Condition of I _{SB1} /I _{DR} Deleted T _{SOLDER} in <u>ABSOLUTE MAXIMUM RATINGS</u>	Mar.30.2009
Rev. 2.7	Revised <u>PACKAGE OUTLINE DIMENSION</u> in page 8 & 9	Dec.18.2009
Rev. 2.8	Revised <u>PACKAGE OUTLINE DIMENSION</u> in page 10	May.7.2010
Rev. 2.9	Revised <u>ORDERING INFORMATION</u> in page 12 Revised <u>PACKAGE OUTLINE DIMENSION</u> in page 9	May.7.2010 Aug.25.2010
Rev. 2.10	Revised <u>ORDERING INFORMATION</u> in page 14 & 15 Deleted <u>WRITE CYCLE</u> Notes : WE#,CE# must be high during all address transitions. in page 6.	Jun.28.2016
Rev. 3.0	1. Deleted <u>FEATURES</u> Package:28-pin 330 mil SOP &28-pin 8mm x 13.4mm STSOP---Page 1 2. Deleted <u>PRODUCT FAMILY</u> Speed : 35ns-- Page 1 3. Deleted <u>PIN CONFIGURATION</u> : SOP & STSOP --- Page 2 4. Deleted <u>AC ELECTRICAL CHARACTERISTICS</u> : (1) READ CYCLE& (2) WRITE CYCLE :LY62256-35 --- Page 4 5. Deleted <u>PACKAGE OUTLINE DIMENSION</u> : 28 pin 330 mil SOP Package Outline Dimension--- V.2.10→Page 9 6. Deleted <u>PACKAGE OUTLINE DIMENSION</u> : 28 pin 8x13.4mm STSOP Package Outline Dimension --- V.2.10→Page 10 7. Deleted <u>ORDERING INFORMATION</u> 28-pin 600mil P-DIP/35ns Item--- Page 10 8. Deleted <u>ORDERING INFORMATION</u> 28-pin 300mil P-DIP /35ns Item--- Page 11 9. Revised <u>ORDERING INFORMATION</u> 28-pin 300mil SOP & 28-pin8mmx13.4mm STSOP --- Page 12~ Page 13	May.23.2025

FEATURES

- Fast access time : 35/55/70ns
- Low power consumption:
Operating current : 20/15/10mA (TYP.)
Standby current : 1μA (TYP.)
- Single 2.7~5.5V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data retention voltage : 1.5V (MIN.)
- **Green package available**
- Package : 28-pin 600 mil P-DIP
28-pin 300 mil Skinny P-DIP

GENERAL DESCRIPTION

The LY62256 is a 262,144-bit low power CMOS static random access memory organized as 32,768 words by 8 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

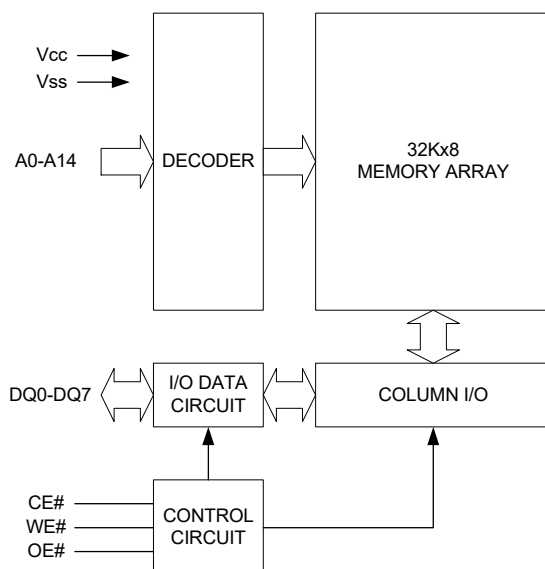
The LY62256 is well designed for low power application, and particularly well suited for battery back-up nonvolatile memory application.

The LY62256 operates from a single power supply of 2.7~5.5V and all inputs and outputs are fully TTL compatible

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation	
				Standby(I_{SB1} , TYP.)	Operating(I_{CC} , TYP.)
LY62256	0 ~ 70°C	2.7 ~ 5.5V	55/70ns	1μA	20/15/10mA
LY62256(E)	-20 ~ 80°C	2.7 ~ 5.5V	55/70ns	1μA	20/15/10mA
LY62256(I)	-40 ~ 85°C	2.7 ~ 5.5V	55/70ns	1μA	20/15/10mA

FUNCTIONAL BLOCK DIAGRAM

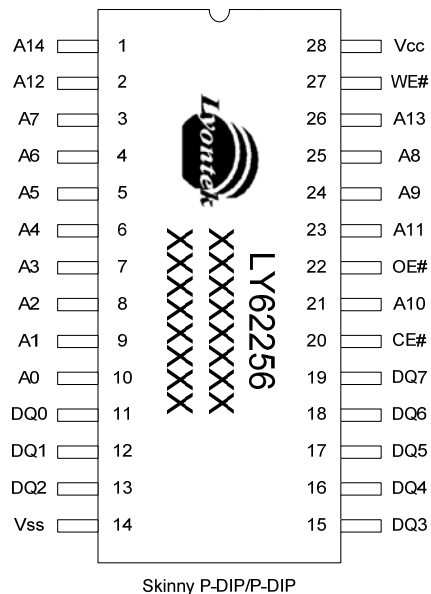


PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A14	Address Inputs
DQ0 - DQ7	Data Inputs/Outputs
CE#	Chip Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
Vcc	Power Supply
Vss	Ground



PIN CONFIGURATION



ABSOLUTE MAXIMUN RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on Vcc relative to Vss	V_{T1}	-0.5 to 6.5	V
Voltage on any other pin relative to Vss	V_{T2}	-0.5 to $V_{CC}+0.5$	V
Operating Temperature	T_A	0 to 70(C grade)	°C
		-20 to 80(E grade)	
		-40 to 85(I grade)	
Storage Temperature	T_{STG}	-65 to 150	°C
Power Dissipation	P_D	1	W
DC Output Current	I_{OUT}	50	mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE#	OE#	WE#	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	High-Z	I_{SB}, I_{SB1}
Output Disable	L	H	H	High-Z	I_{CC}, I_{CC1}
Read	L	L	H	DOUT	I_{CC}, I_{CC1}
Write	L	X	L	DIN	I_{CC}, I_{CC1}

Note: H = V_{IH} , L = V_{IL} , X = Don't care.



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP. ^{*4}	MAX.	UNIT	
Supply Voltage	V _{CC}			2.7	3.3	5.5	V	
Input High Voltage	V _{IH} ^{*1}			2.4	-	V _{CC} +0.5	V	
Input Low Voltage	V _{IL} ^{*2}	V _{CC} =2.7~3.6V		- 0.5	-	0.6	V	
		V _{CC} =4.5~5.5V		- 0.5	-	0.8	V	
Input Leakage Current	I _{LI}	V _{CC} ≥ V _{IN} ≥ V _{SS}		- 1	-	1	μA	
Output Leakage Current	I _{LO}	V _{CC} ≥ V _{OUT} ≥ V _{SS} , Output Disabled		- 1	-	1	μA	
Output High Voltage	V _{OH}	I _{OH} = -1mA		2.4	3.0	-	V	
Output Low Voltage	V _{OL}	I _{OL} = 2mA		-	-	0.4	V	
Average Operating Power supply Current	I _{CC}	Cycle time = Min. CE# = V _{IL} , I _{I/O} = 0mA Other pins at V _{IL} or V _{IH}	-35	-	20	50	mA	
			-55	-	15	45	mA	
			-70	-	10	40	mA	
	I _{CC1}	Cycle time = 1μs CE# ≤ 0.2V and I _{I/O} = 0mA other pins at 0.2V or V _{CC} -0.2V		-	3	10	mA	
	I _{SB}	CE# = V _{IH} , other pins at V _{IL} or V _{IH}		-	1	3	mA	
Standby Power Supply Current	I _{SB1}	CE# ≥ V _{CC} -0.2V Others at 0.2V or V _{CC} - 0.2V	LL		-	1	20	μA
			LLE/LLI		-	1	30	μA
			SL ^{*5}	25℃	-	1	3	μA
			SLE ^{*5}	40℃	-	1.5	4	μA
			SLI ^{*5}		-	1	10	μA
			SL		-	1	20	μA
			SLE/SLI		-	1	20	μA

Notes:

- V_{IH}(max) = V_{CC} + 3.0V for pulse width less than 10ns.
 - V_{IL}(min) = V_{SS} - 3.0V for pulse width less than 10ns.
 - Over/Undershoot specifications are characterized, not 100% tested.
 - Typical values are included for reference only and are not guaranteed or tested.
- Typical valued are measured at V_{CC} = V_{CC}(TYP.) and T_A = 25°C
- This parameter is measured at V_{CC} = 3.0V

CAPACITANCE (T_A = 25°C, f = 1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C _{IN}	-	6	pF
Input/Output Capacitance	C _{I/O}	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0.2V to V _{CC} - 0.2V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	C _L = 50pF + 1TTL, I _{OH} /I _{OL} = -1mA/2mA



AC ELECTRICAL CHARACTERISTICS

(1) READ CYCLE

PARAMETER	SYM.	LY62256-55		LY62256-70		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t _{RC}	55	-	70	-	ns
Address Access Time	t _{AA}	-	55	-	70	ns
Chip Enable Access Time	t _{ACE}	-	55	-	70	ns
Output Enable Access Time	t _{OE}	-	30	-	35	ns
Chip Enable to Output in Low-Z	t _{CLZ} *	10	-	10	-	ns
Output Enable to Output in Low-Z	t _{OLZ} *	5	-	5	-	ns
Chip Disable to Output in High-Z	t _{CHZ} *	-	20	-	25	ns
Output Disable to Output in High-Z	t _{OHZ} *	-	20	-	25	ns
Output Hold from Address Change	t _{OH}	10	-	10	-	ns

(2) WRITE CYCLE

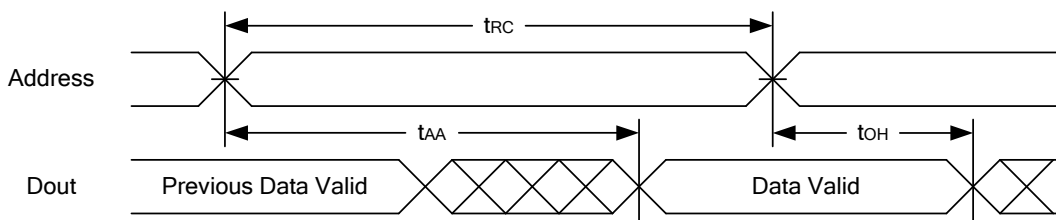
PARAMETER	SYM.	LY62256-55		LY62256-70		UNIT
		MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t _{WC}	55	-	70	-	ns
Address Valid to End of Write	t _{AW}	50	-	60	-	ns
Chip Enable to End of Write	t _{CW}	50	-	60	-	ns
Address Set-up Time	t _{AS}	0	-	0	-	ns
Write Pulse Width	t _{WP}	45	-	55	-	ns
Write Recovery Time	t _{WR}	0	-	0	-	ns
Data to Write Time Overlap	t _{DW}	25	-	30	-	ns
Data Hold from End of Write Time	t _{DH}	0	-	0	-	ns
Output Active from End of Write	t _{OW} *	5	-	5	-	ns
Write to Output in High-Z	t _{WHZ} *	-	20	-	25	ns

*These parameters are guaranteed by device characterization, but not production tested.

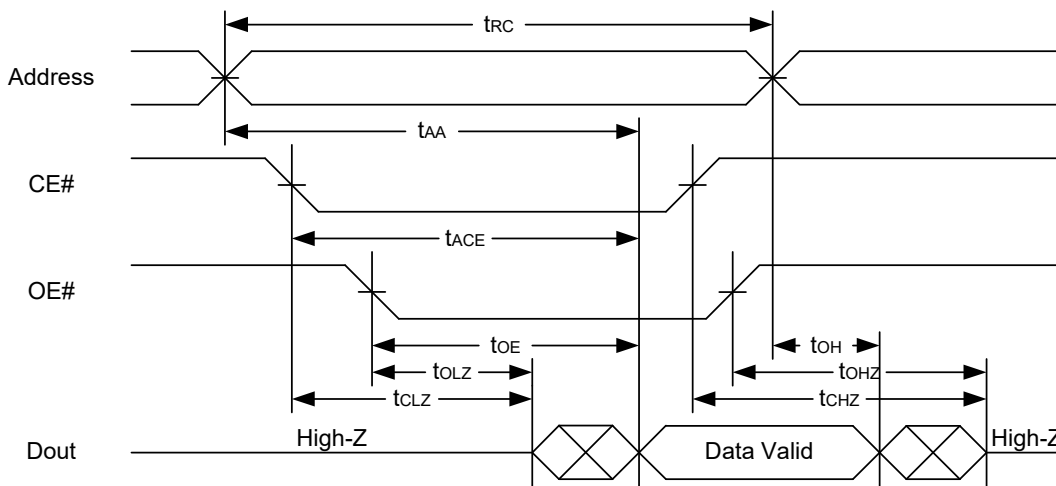


TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)



READ CYCLE 2 (CE# and OE# Controlled) (1,3,4,5)

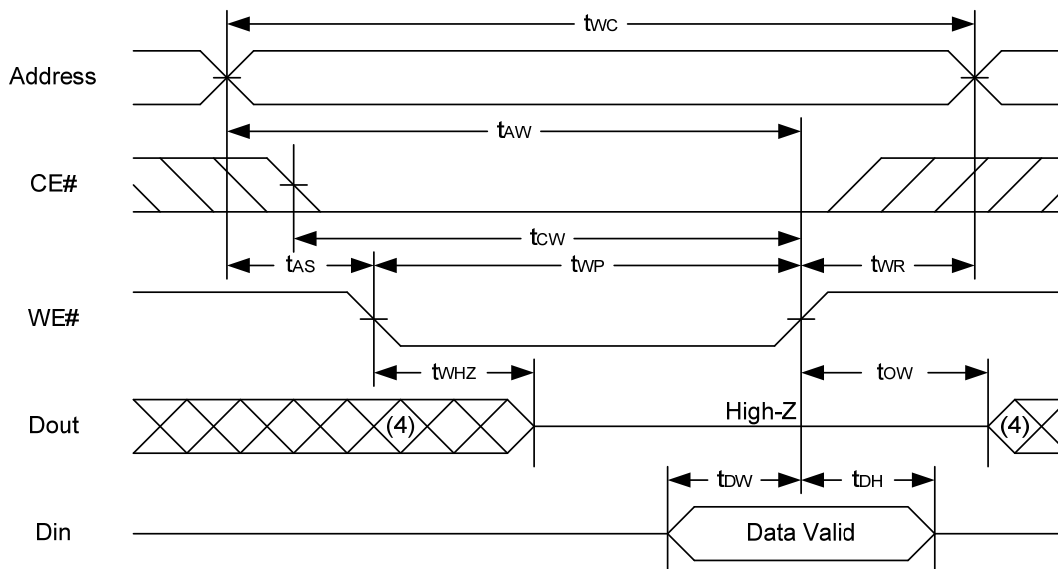


Notes :

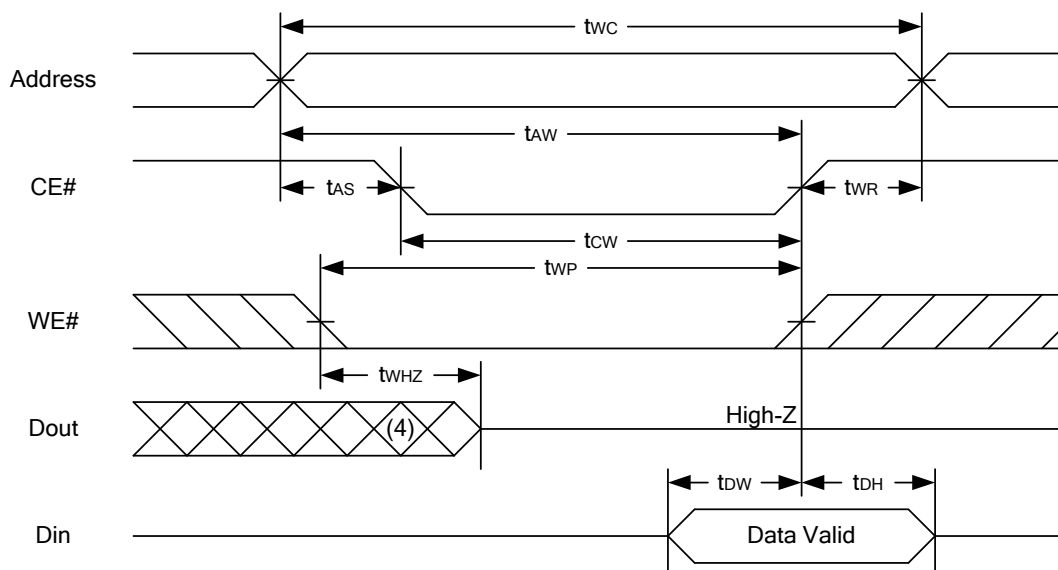
1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low.
3. Address must be valid prior to or coincident with CE# = low.; otherwise tAA is the limiting parameter.
4. tCLZ, tOLZ, tCHZ and tOHZ are specified with CL = 5pF. Transition is measured ±500mV from steady state.
5. At any given temperature and voltage condition, tCHZ is less than tCLZ, tOHZ is less than tOLZ.



WRITE CYCLE 1 (WE# Controlled) (1,2,4,5)



WRITE CYCLE 2 (CE# Controlled) (1,4,5)



Notes :

1. A write occurs during the overlap of a low CE#, low WE#.
2. During a WE# controlled write cycle with OE# low, tWP must be greater than tWHZ + tDW to allow the drivers to turn off and data to be placed on the bus.
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the CE# low transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
5. tOW and tWHZ are specified with CL = 5pF. Transition is measured $\pm 500\text{mV}$ from steady state.

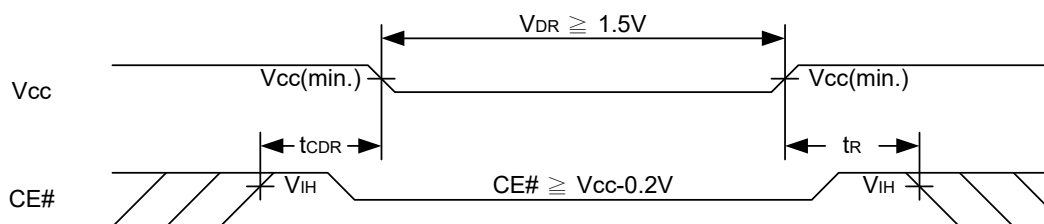


DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
V _{CC} for Data Retention	V _{DR}	CE# $\geq$ V _{CC} - 0.2V	1.5	-	5.5	V
Data Retention Current	I _{DR}	V _{CC} = 1.5V CE# $\geq$ V _{CC} - 0.2V Others at 0.2V or V _{CC} -0.2V	LL/LLE/LLI	-	0.5	20 μ A
			SL	25°C	-	0.5 μ A
			SLE	40°C	-	1 μ A
			SLI	-	1	3 μ A
			SL	-	0.5	8 μ A
			SLE/SLI	-	0.5	15 μ A
Chip Disable to Data Retention Time	t _{CDR}	See Data Retention Waveforms (below)	0	-	-	ns
Recovery Time	t _R		t _{RC} *	-	-	ns

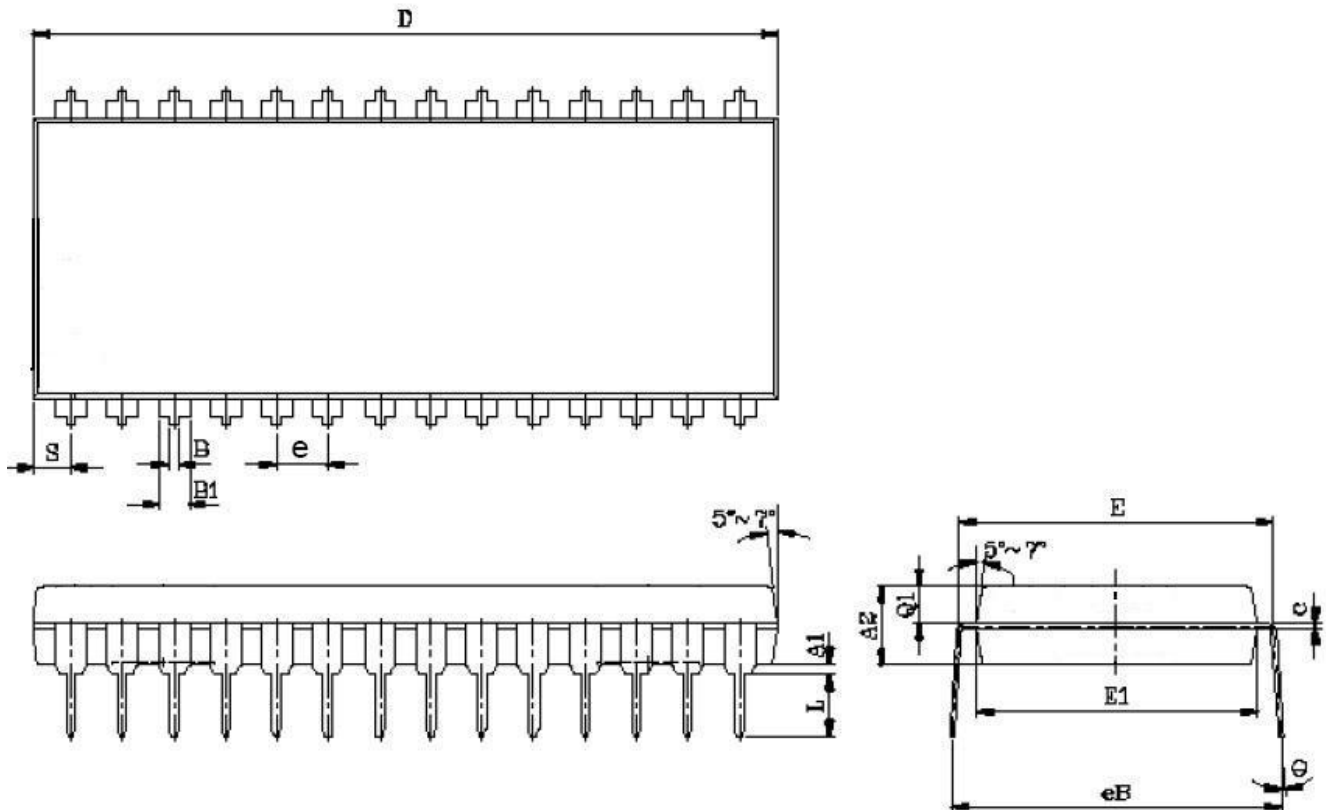
t_{RC}* = Read Cycle Time

DATA RETENTION WAVEFORM



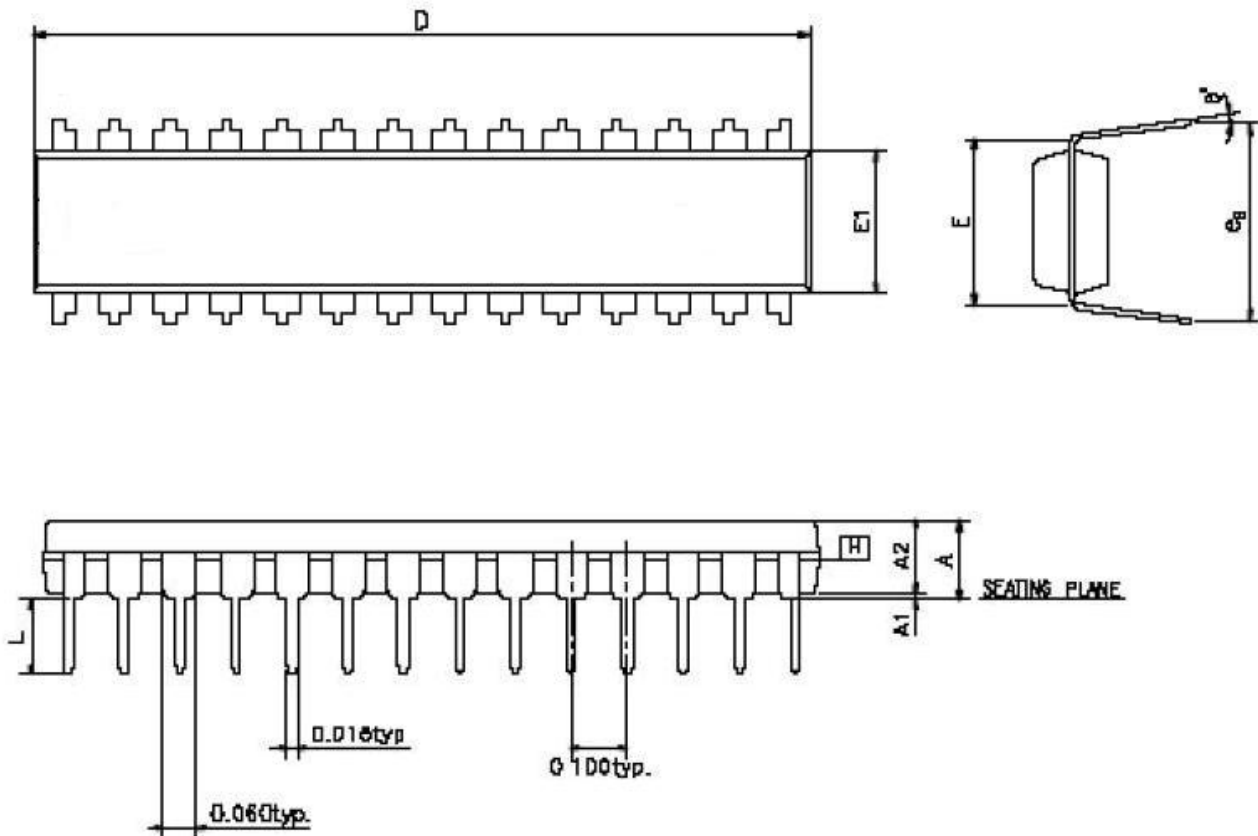
PACKAGE OUTLINE DIMENSION

28 pin 600 mil P-DIP Package Outline Dimension



SYM.	NIT	INCH.(BASE)	MM(REF)
A1		0.015(MIN)	0.381(MIN)
A2		0.155±0.005	3.937±0.127
B		0.020(MAX)	0.508(MAX)
B1		0.060(TYP)	1.524(TYP)
c		0.012(MAX)	0.304(MAX)
D		1.470(MAX)	37.338(MAX)
E		0.6(TYP)	15.24(TYP)
E1		0.55(MAX)	13.970(MAX)
e		0.100(TYP)	2.540(TYP)
eB		0.650±0.020	16.510±0.508
L		0.200(MAX)	5.080(MAX)
S		0.06(MAX)	1.524(MAX)
Q1		0.08(MAX)	2.032(MAX)
Θ		15°(MAX)	15°(MAX)

28 pin 300 mil P-DIP Package Outline Dimension



SYMBOLS	MIN.	NOR.	MAX.
A	—	—	0.210
A1	0.015	—	—
A2	0.125	0.130	0.135
D	1.385	1.390	1.400
E	0.310 BSC		
E1	0.283	0.288	0.293
L	0.115	0.130	0.150
ϕ_B	0.330	0.350	0.370
θ°	0	7	15

UNIT : INCH

NOTE:

1. JEDEC OUTLINE : MS-D15 AH



ORDERING INFORMATION

[Production Status: M/P]

Package Type	Access Time (Speed)(ns)	Power Type	Temperature Range(°C)	Packing Type	Lyontek Item No.
28-pin 600mil P-DIP	55	Ultra Low Power	0°C~70°C	Tube	LY62256PL-55LL
			-20°C~80°C	Tube	LY62256PL-55LLE
			-40°C~85°C	Tube	LY62256PL-55LLI
		Special Ultra Low Power	0°C~70°C	Tube	LY62256PL-55SL
			-20°C~80°C	Tube	LY62256PL-55SLE
			-40°C~85°C	Tube	LY62256PL-55SLI
	70	Ultra Low Power	0°C~70°C	Tube	LY62256PL-70LL
			-20°C~80°C	Tube	LY62256PL-70LLE
			-40°C~85°C	Tube	LY62256PL-70LLI
		Special Ultra Low Power	0°C~70°C	Tube	LY62256PL-70SL
			-20°C~80°C	Tube	LY62256PL-70SLE
			-40°C~85°C	Tube	LY62256PL-70SLI



ORDERING INFORMATION

[Production Status: M/P]

Package Type	Access Time (Speed)(ns)	Power Type	Temperature Range(°C)	Packing Type	Lyontek Item No.
28-pin 300mil P-DIP	55	Ultra Low Power	0°C~70°C	Tube	LY62256DL-55LL
			-20°C~80°C	Tube	LY62256DL-55LLE
			-40°C~85°C	Tube	LY62256DL-55LLI
		Special Ultra Low Power	0°C~70°C	Tube	LY62256DL-55SL
			-20°C~80°C	Tube	LY62256DL-55SLE
			-40°C~85°C	Tube	LY62256DL-55SLI
	70	Ultra Low Power	0°C~70°C	Tube	LY62256DL-70LL
			-20°C~80°C	Tube	LY62256DL-70LLE
			-40°C~85°C	Tube	LY62256DL-70LLI
		Special Ultra Low Power	0°C~70°C	Tube	LY62256DL-70SL
			-20°C~80°C	Tube	LY62256DL-70SLE
			-40°C~85°C	Tube	LY62256DL-70SLI



ORDERING INFORMATION

[Production Status: **EOL**]

Package Type	Access Time (Speed)(ns)	Power Type	Temperature Range(°C)	Packing Type	Lyontek Item No.	Substitute Product
28-pin 300mil SOP	35	Ultra Low Power	0°C~70°C	Tube	LY62256SL-35LL	LY62256BSL-45SLI
				Tape Reel	LY62256SL-35LLT	LY62256BSL-45SLIT
			-20°C~80°C	Tube	LY62256SL-35LLE	LY62256BSL-45SLI
				Tape Reel	LY62256SL-35LLET	LY62256BSL-45SLIT
			-40°C~85°C	Tube	LY62256SL-35LLI	LY62256BSL-45SLI
				Tape Reel	LY62256SL-35LLIT	LY62256BSL-45SLIT
		Special Ultra Low Power	0°C~70°C	Tube	LY62256SL-35SL	LY62256BSL-45SLI
				Tape Reel	LY62256SL-35SLT	LY62256BSL-45SLIT
			-20°C~80°C	Tube	LY62256SL-35SLE	LY62256BSL-45SLI
				Tape Reel	LY62256SL-35SLET	LY62256BSL-45SLIT
			-40°C~85°C	Tube	LY62256SL-35SLI	LY62256BSL-45SLI
				Tape Reel	LY62256SL-35SLIT	LY62256BSL-45SLIT
	55	Ultra Low Power	0°C~70°C	Tube	LY62256SL-55LL	LY62256BSL-45SLI
				Tape Reel	LY62256SL-55LLT	LY62256BSL-45SLIT
			-20°C~80°C	Tube	LY62256SL-55LLE	LY62256BSL-45SLI
				Tape Reel	LY62256SL-55LLET	LY62256BSL-45SLIT
			-40°C~85°C	Tube	LY62256SL-55LLI	LY62256BSL-45SLI
				Tape Reel	LY62256SL-55LLIT	LY62256BSL-45SLIT
		Special Ultra Low Power	0°C~70°C	Tube	LY62256SL-55SL	LY62256BSL-45SLI
				Tape Reel	LY62256SL-55SLT	LY62256BSL-45SLIT
			-20°C~80°C	Tube	LY62256SL-55SLE	LY62256BSL-45SLI
				Tape Reel	LY62256SL-55SLET	LY62256BSL-45SLIT
			-40°C~85°C	Tube	LY62256SL-55SLI	LY62256BSL-45SLI
				Tape Reel	LY62256SL-55SLIT	LY62256BSL-45SLIT
	70	Ultra Low Power	0°C~70°C	Tube	LY62256SL-70LL	LY62256BSL-45SLI
				Tape Reel	LY62256SL-70LLT	LY62256BSL-45SLIT
			-20°C~80°C	Tube	LY62256SL-70LLE	LY62256BSL-45SLI
				Tape Reel	LY62256SL-70LLET	LY62256BSL-45SLIT
			-40°C~85°C	Tube	LY62256SL-70LLI	LY62256BSL-45SLI
				Tape Reel	LY62256SL-70LLIT	LY62256BSL-45SLIT
		Special Ultra Low Power	0°C~70°C	Tube	LY62256SL-70SL	LY62256BSL-45SLI
				Tape Reel	LY62256SL-70SLT	LY62256BSL-45SLIT
			-20°C~80°C	Tube	LY62256SL-70SLE	LY62256BSL-45SLI
				Tape Reel	LY62256SL-70SLET	LY62256BSL-45SLIT
			-40°C~85°C	Tube	LY62256SL-70SLI	LY62256BSL-45SLI
				Tape Reel	LY62256SL-70SLIT	LY62256BSL-45SLIT



ORDERING INFORMATION

[Production Status: **EOL**]

Package Type	Access Time (Speed)(ns)	Power Type	Temperature Range(°C)	Packing Type	Lyontek Item No.	Substitute Product
28-pin 8mmx13.4mm STSOP	35	Ultra Low Power	0°C~70°C	Tray	LY62256RL-35LL	LY62256BRL-45SLI
				Tape Reel	LY62256RL-35LLT	LY62256BRL-45SLIT
			-20°C~80°C	Tray	LY62256RL-35LLE	LY62256BRL-45SLI
				Tape Reel	LY62256RL-35LLET	LY62256BRL-45SLIT
			-40°C~85°C	Tray	LY62256RL-35LLI	LY62256BRL-45SLI
				Tape Reel	LY62256RL-35LLIT	LY62256BRL-45SLIT
		Special Ultra Low Power	0°C~70°C	Tray	LY62256RL-35SL	LY62256BRL-45SLI
				Tape Reel	LY62256RL-35SLT	LY62256BRL-45SLIT
			-20°C~80°C	Tray	LY62256RL-35SLE	LY62256BRL-45SLI
				Tape Reel	LY62256RL-35SLET	LY62256BRL-45SLIT
			-40°C~85°C	Tray	LY62256RL-35SLI	LY62256BRL-45SLI
				Tape Reel	LY62256RL-35SLIT	LY62256BRL-45SLIT
	55	Ultra Low Power	0°C~70°C	Tray	LY62256RL-55LL	LY62256BRL-45SLI
				Tape Reel	LY62256RL-55LLT	LY62256BRL-45SLIT
			-20°C~80°C	Tray	LY62256RL-55LLE	LY62256BRL-45SLI
				Tape Reel	LY62256RL-55LLET	LY62256BRL-45SLIT
			-40°C~85°C	Tray	LY62256RL-55LLI	LY62256BRL-45SLI
				Tape Reel	LY62256RL-55LLIT	LY62256BRL-45SLIT
		Special Ultra Low Power	0°C~70°C	Tray	LY62256RL-55SL	LY62256BRL-45SLI
				Tape Reel	LY62256RL-55SLT	LY62256BRL-45SLIT
			-20°C~80°C	Tray	LY62256RL-55SLE	LY62256BRL-45SLI
				Tape Reel	LY62256RL-55SLET	LY62256BRL-45SLIT
			-40°C~85°C	Tray	LY62256RL-55SLI	LY62256BRL-45SLI
				Tape Reel	LY62256RL-55SLIT	LY62256BRL-45SLIT
	70	Ultra Low Power	0°C~70°C	Tray	LY62256RL-70LL	LY62256BRL-45SLI
				Tape Reel	LY62256RL-70LLT	LY62256BRL-45SLIT
			-20°C~80°C	Tray	LY62256RL-70LLE	LY62256BRL-45SLI
				Tape Reel	LY62256RL-70LLET	LY62256BRL-45SLIT
			-40°C~85°C	Tray	LY62256RL-70LLI	LY62256BRL-45SLI
				Tape Reel	LY62256RL-70LLIT	LY62256BRL-45SLIT
		Special Ultra Low Power	0°C~70°C	Tray	LY62256RL-70SL	LY62256BRL-45SLI
				Tape Reel	LY62256RL-70SLT	LY62256BRL-45SLIT
			-20°C~80°C	Tray	LY62256RL-70SLE	LY62256BRL-45SLI
				Tape Reel	LY62256RL-70SLET	LY62256BRL-45SLIT
			-40°C~85°C	Tray	LY62256RL-70SLI	LY62256BRL-45SLI
				Tape Reel	LY62256RL-70SLIT	LY62256BRL-45SLIT



Lyontek Inc.

LY62256

Rev. 3.0

32K X 8 BIT LOW POWER CMOS SRAM

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