



REVISION HISTORY

<u>Revision</u>	<u>Description</u>	<u>Issue Date</u>
Rev. 1.0	Initial Issue	Sep.28.2022
Rev. 1.1	Deleted the Extended grade (Page3&Page7); Revised Vih & Tightened DC Parameters (Page3)	Jan.30.2024
Rev. 1.2	1.Revised <u>DC ELECTRICAL CHARACTERISTICS</u> :ICC TEST CONDITION& Deleted ISB SYMBOL---Page3 2. Deleted Package : 28-pin 600 mil P-DIP ---Page1 3. Deleted <u>PACKAGE OUTLINE DIMENSION</u> :28 pin 600 mil P-DIP Package Outline Dimension --- Page 8 4. Revised <u>ORDERING INFORMATION</u> ---Page10	Mar.27.2024
Rev. 1.3	1. Revised <u>FEATURES</u> : Low power consumption: Operating current : 12/10 mA →9/8 mA --- Page1 2. Revised <u>PRODUCT FAMILY</u> :Power Dissipation :Operating(Icc,TYP.) 12/10 mA→9/8 mA --- Page1 3. Revised <u>DC ELECTRICAL CHARACTERISTICS</u> : Average Operating Power supply Current : ICC: TYP. *4 :12→9 , 10→8 , MAX.: 18→16,15→13, --- Page3 4. Revised <u>ORDERING INFORMATION</u> Packing Type :Tape Reel ---Page10	May.26.2025
Rev. 1.4	Revised <u>ORDERING INFORMATION</u> : 32 Pin(450mil) SOP PackingType : Tube→Tray in page 10	Aug.13.2025

FEATURES

- Fast access time : 45/55ns
- Low power consumption:
Operating current : 9/8mA (TYP.)
Standby current : 1 μ A (TYP.)
- Single 2.7~5.5V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data retention voltage : 1.5V (MIN.)
- **Green package available**
- Package : 28-pin 330 mil SOP
28-pin 8mm x 13.4mm sTSP

GENERAL DESCRIPTION

The LY62256B is a 262,144-bit low power CMOS static random access memory organized as 32,768 words by 8 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

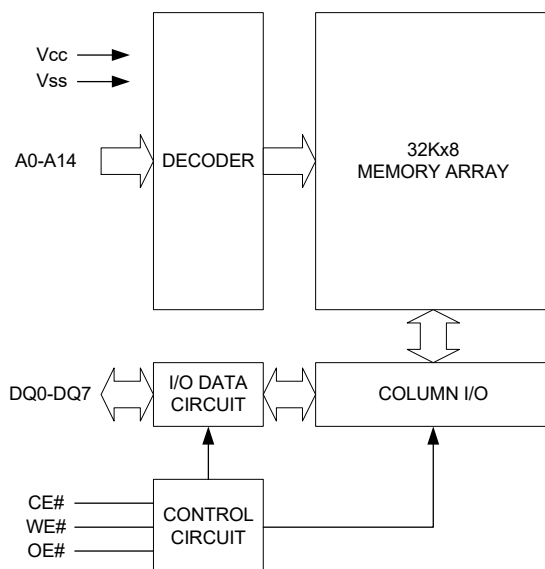
The LY62256B is well designed for low power application, and particularly well suited for battery back-up nonvolatile memory application.

The LY62256B operates from a single power supply of 2.7~5.5V and all inputs and outputs are fully TTL compatible

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation	
				Standby(I _{SB1} ,TYP.)	Operating(I _{CC} ,TYP.)
LY62256B(I)	-40 ~ 85°C	2.7 ~ 5.5V	45/55ns	1 μ A	9/8mA

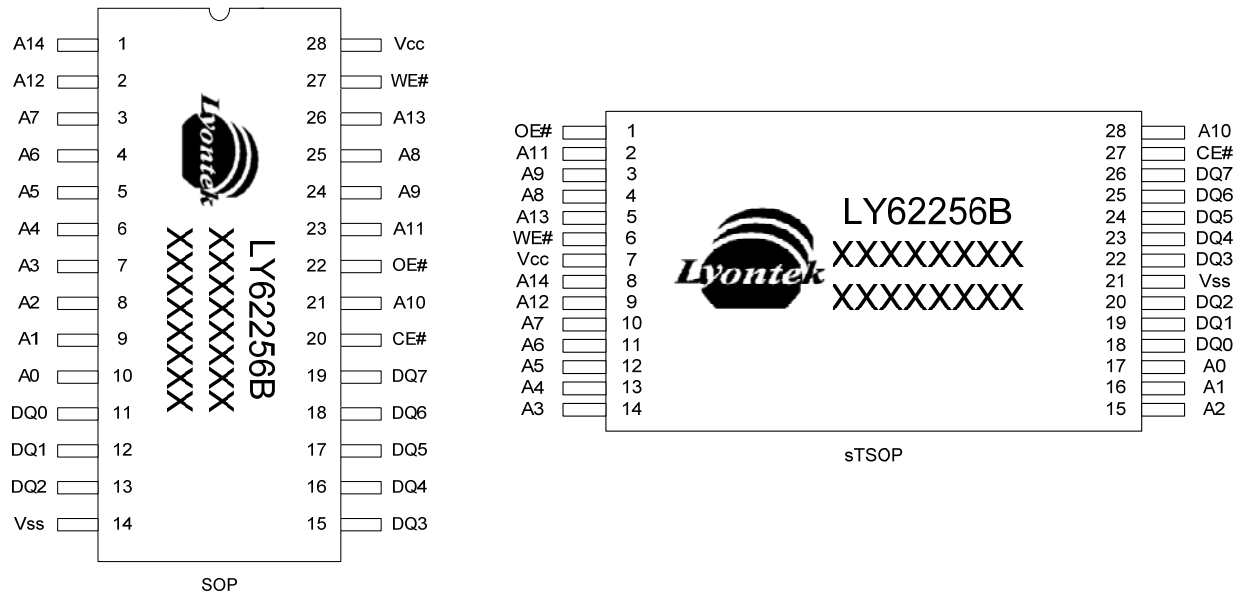
FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A14	Address Inputs
DQ0 – DQ7	Data Inputs/Outputs
CE#	Chip Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
Vcc	Power Supply
Vss	Ground

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on Vcc relative to Vss	V _{T1}	-0.5 to 6.5	V
Voltage on any other pin relative to Vss	V _{T2}	-0.5 to Vcc+0.5	V
Operating Temperature	T _A	0 to 70(C grade)	°C
		-20 to 80(E grade)	
		-40 to 85(I grade)	
Storage Temperature	T _{STG}	-65 to 150	°C
Power Dissipation	P _D	1	W
DC Output Current	I _{OUT}	50	mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE#	OE#	WE#	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	High-Z	I _{SB} , I _{SB1}
Output Disable	L	H	H	High-Z	I _{CC} , I _{CC1}
Read	L	L	H	D _{OUT}	I _{CC} , I _{CC1}
Write	L	X	L	D _{IN}	I _{CC} , I _{CC1}

Note: H = V_{IH}, L = V_{IL}, X = Don't care.



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP. ^{*4}	MAX.	UNIT	
Supply Voltage	V _{CC}			2.7	3.3	5.5	V	
Input High Voltage	V _{IH} ^{*1}	V _{CC} =2.7~3.6V		2.2	-	V _{CC} +0.5	V	
		V _{CC} =4.5~5.5V		0.5V _{CC}		V _{CC} +0.5		
Input Low Voltage	V _{IL} ^{*2}	V _{CC} =2.7~3.6V		- 0.5	-	0.6	V	
		V _{CC} =4.5~5.5V		- 0.5	-	0.8	V	
Input Leakage Current	I _{LI}	V _{CC} ≥ V _{IN} ≥ V _{SS}		- 1	-	1	μA	
Output Leakage Current	I _{LO}	V _{CC} ≥ V _{OUT} ≥ V _{SS} , Output Disabled		- 1	-	1	μA	
Output High Voltage	V _{OH}	I _{OH} = -1mA		2.4	3.0	-	V	
Output Low Voltage	V _{OL}	I _{OL} = 2mA		-	-	0.4	V	
Average Operating Power supply Current	I _{CC}	Cycle time = Min. CE# ≤ 0.2V , I _{I/O} = 0mA Other pins at 0.2V or V _{CC} -0.2V		-45	-	9	16	mA
				-55	-	8	13	mA
	I _{CC1}	Cycle time = 1μs CE# ≤ 0.2V and I _{I/O} = 0mA Other pins at 0.2V or V _{CC} -0.2V		-	2	4	mA	
Standby Power Supply Current	I _{SB1}	CE# ≥ V _{CC} -0.2V Others at 0.2V or V _{CC} - 0.2V	SL ^{*5}	25℃	-	1	3	μA
			SLI ^{*5}	40℃	-	1.5	3.5	μA
			SL		-	1	7	μA
			SLI		-	1	12	μA

Notes:

1. V_{IH}(max) = V_{CC} + 3.0V for pulse width less than 10ns.
2. V_{IL}(min) = V_{SS} - 3.0V for pulse width less than 10ns.
3. Over/Undershoot specifications are characterized, not 100% tested.
4. Typical values are included for reference only and are not guaranteed or tested.
Typical values are measured at V_{CC} = V_{CC}(TYP.) and T_A = 25°C
5. This parameter is measured at V_{CC} = 3.0V

CAPACITANCE (T_A = 25°C, f = 1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C _{IN}	-	6	pF
Input/Output Capacitance	C _{I/O}	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0.2V to V _{CC} - 0.2V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	C _L = 50pF + 1TTL, I _{OH} /I _{OL} = -1mA/2mA



AC ELECTRICAL CHARACTERISTICS

(1) READ CYCLE

PARAMETER	SYM.	LY62256B-45		LY62256B-55		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t _{RC}	45	-	55	-	ns
Address Access Time	t _{AA}	-	45	-	55	ns
Chip Enable Access Time	t _{ACE}	-	45	-	55	ns
Output Enable Access Time	t _{OE}	-	20	-	25	ns
Chip Enable to Output in Low-Z	t _{CLZ} *	10	-	10	-	ns
Output Enable to Output in Low-Z	t _{OLZ} *	5	-	5	-	ns
Chip Disable to Output in High-Z	t _{CHZ} *	-	15	-	20	ns
Output Disable to Output in High-Z	t _{OHZ} *	-	15	-	20	ns
Output Hold from Address Change	t _{OH}	10	-	10	-	ns

(2) WRITE CYCLE

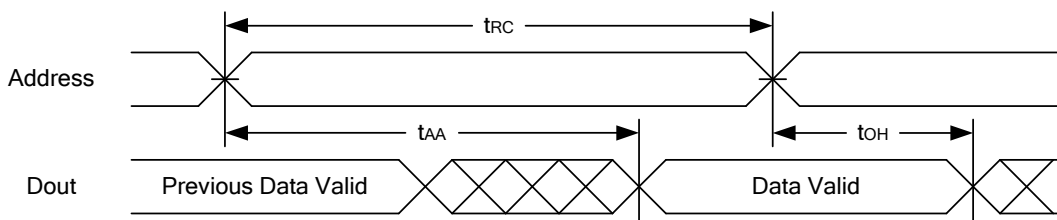
PARAMETER	SYM.	LY62256B-45		LY62256B-55		UNIT
		MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t _{WC}	45	-	55	-	ns
Address Valid to End of Write	t _{AW}	40	-	50	-	ns
Chip Enable to End of Write	t _{CW}	40	-	50	-	ns
Address Set-up Time	t _{AS}	0	-	0	-	ns
Write Pulse Width	t _{WP}	35	-	45	-	ns
Write Recovery Time	t _{WR}	0	-	0	-	ns
Data to Write Time Overlap	t _{DW}	20	-	25	-	ns
Data Hold from End of Write Time	t _{DH}	0	-	0	-	ns
Output Active from End of Write	t _{OW} *	5	-	5	-	ns
Write to Output in High-Z	t _{WHZ} *	-	15	-	20	ns

*These parameters are guaranteed by device characterization, but not production tested.

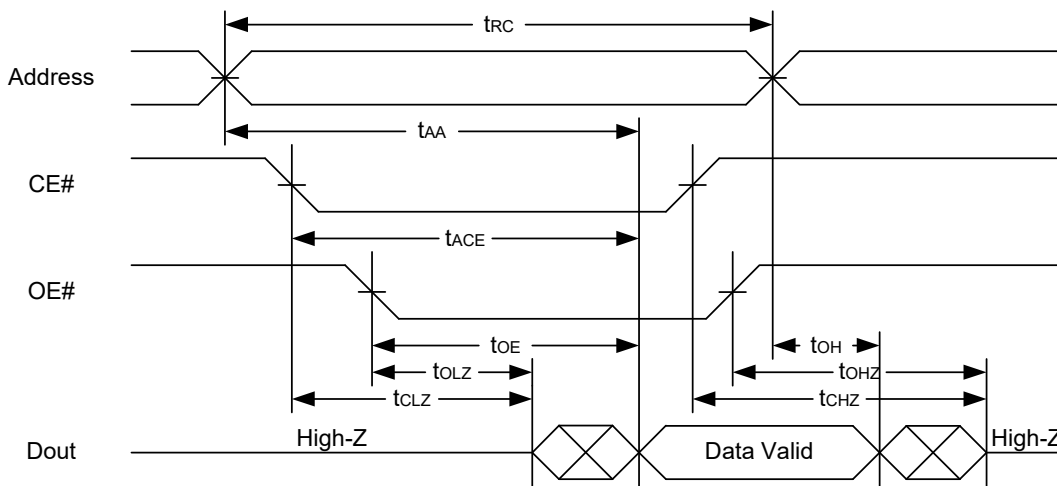


TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)



READ CYCLE 2 (CE# and OE# Controlled) (1,3,4,5)

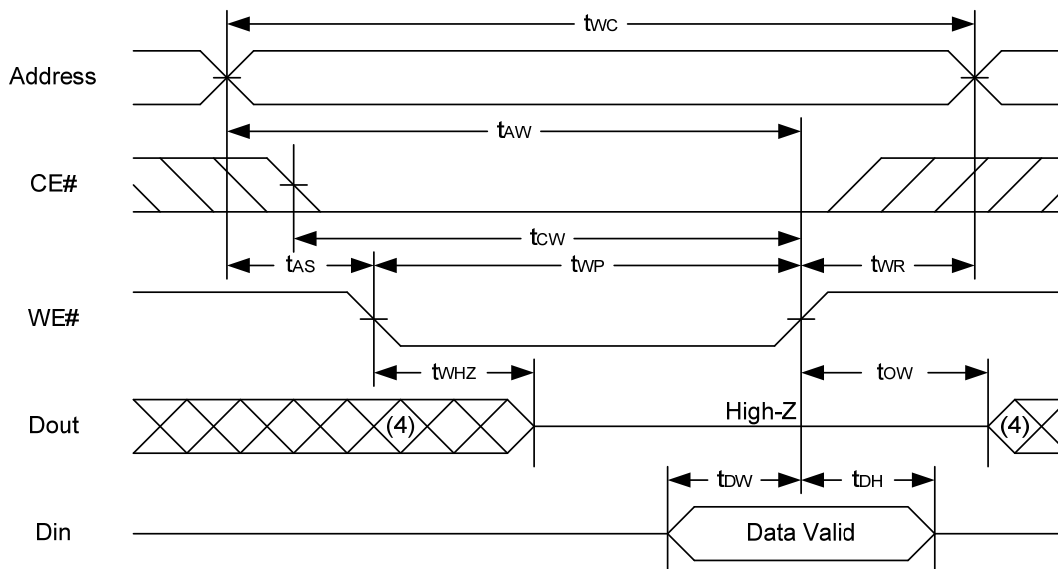


Notes :

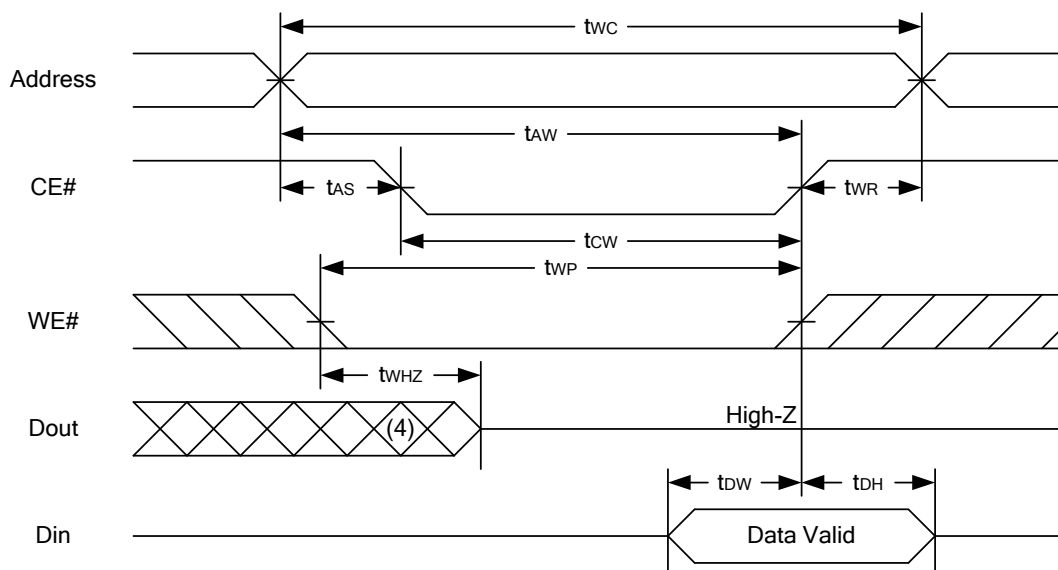
1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low.
3. Address must be valid prior to or coincident with CE# = low.; otherwise t_{AA} is the limiting parameter.
4. t_{CLZ} , t_{OLZ} , t_{CHZ} and t_{OHZ} are specified with $C_L = 5\text{pF}$. Transition is measured $\pm 500\text{mV}$ from steady state.
5. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{OHZ} is less than t_{OLZ} .



WRITE CYCLE 1 (WE# Controlled) (1,2,4,5)



WRITE CYCLE 2 (CE# Controlled) (1,4,5)



Notes :

- 1.A write occurs during the overlap of a low CE#, low WE#.
- 2.During a WE# controlled write cycle with OE# low, tWP must be greater than tWHZ + tDW to allow the drivers to turn off and data to be placed on the bus.
- 3.During this period, I/O pins are in the output state, and input signals must not be applied.
- 4.If the CE# low transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
- 5.tOW and tWHZ are specified with $C_L = 5\text{pF}$. Transition is measured $\pm 500\text{mV}$ from steady state.

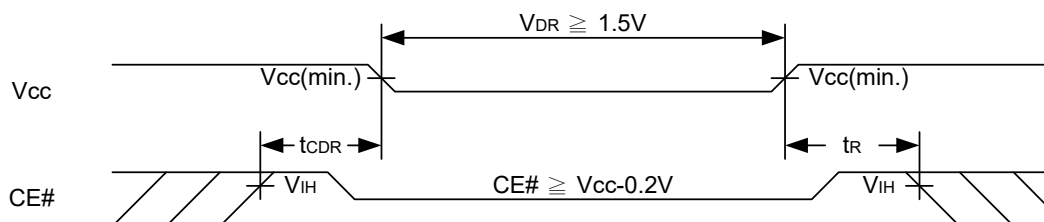


DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
V _{CC} for Data Retention	V _{DR}	CE# ≥ V _{CC} - 0.2V			1.5	-	5.5	V
Data Retention Current	I _{DR}	V _{CC} = 1.5V CE# ≥ V _{CC} - 0.2V Others at 0.2V or V _{CC} -0.2V	SL	25°C	-	1	3	μA
			SLI	40°C	-	1	3.5	μA
			SL		-	1	8	μA
			SLI		-	1	15	μA
Chip Disable to Data Retention Time	t _{CDR}	See Data Retention Waveforms (below)			0	-	-	ns
Recovery Time	t _R				t _{RC} *	-	-	ns

t_{RC}* = Read Cycle Time

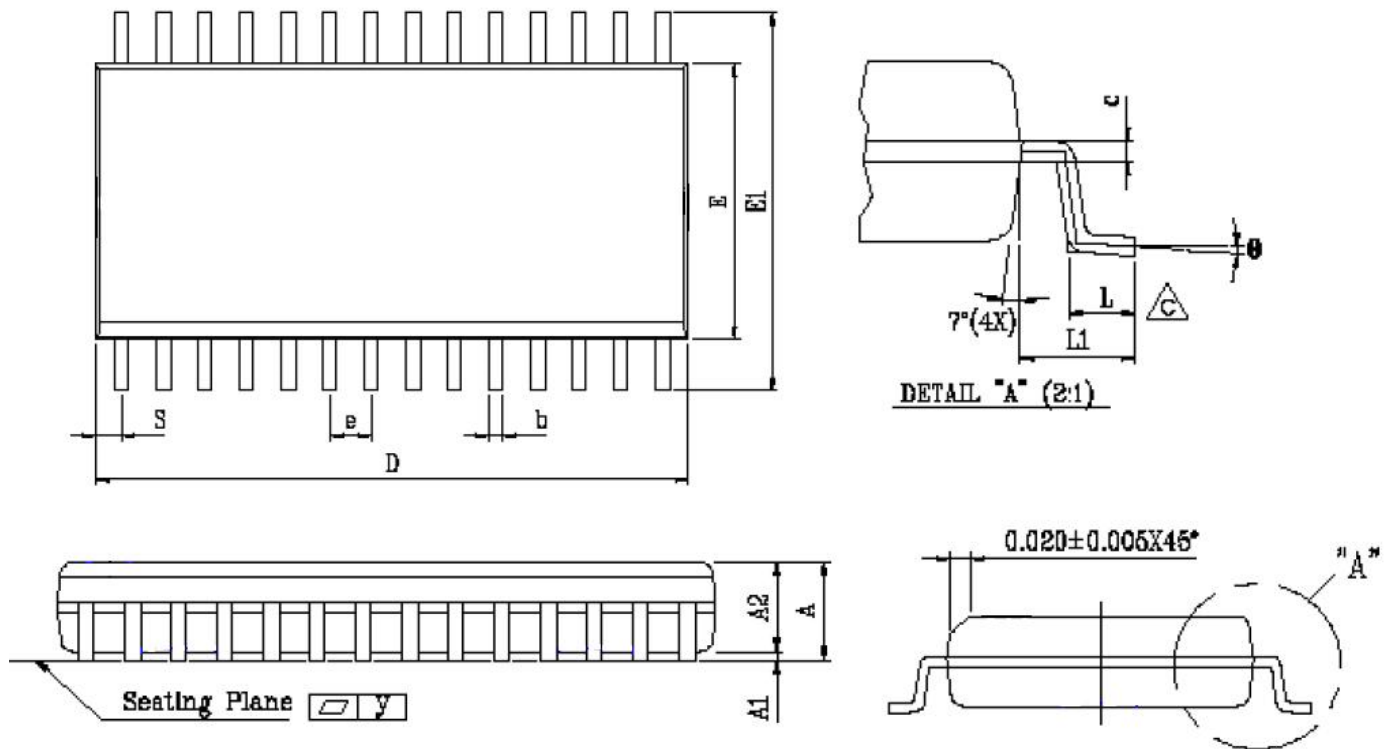
DATA RETENTION WAVEFORM





PACKAGE OUTLINE DIMENSION

28 pin 330 mil SOP Package Outline Dimension

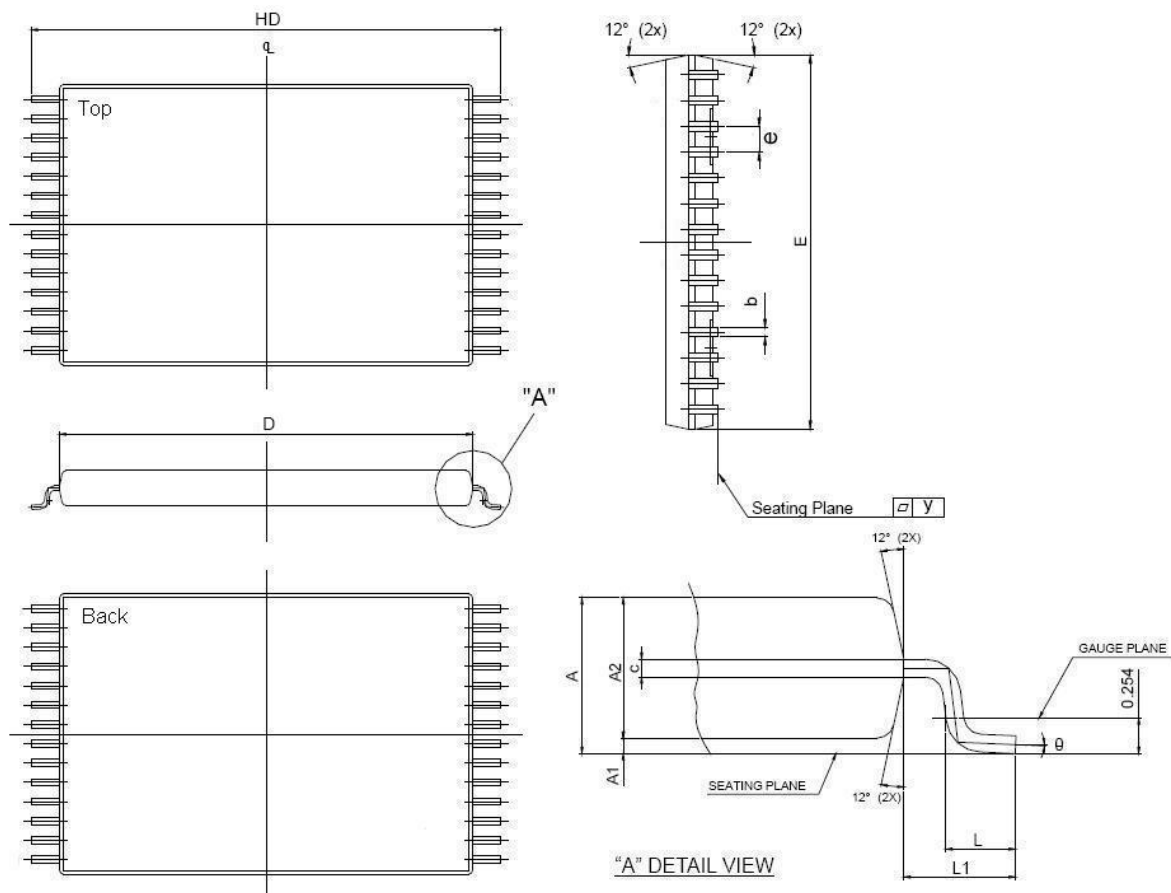


SYM.	UNIT	INCH(BASE)	MM(REF)
A		0.120(MAX)	3.048(MAX)
A1		0.002(MIN)	0.05(MIN)
A2		0.098±0.005	2.489±0.127
b		0.016(TYP)	0.406(TYP)
c		0.010(TYP)	0.254(TYP)
D		0.728(MAX)	18.491(MAX)
E		0.340(MAX)	8.636(MAX)
E1		0.465±0.012	11.811±0.305
e		0.050(TYP)	1.270(TYP)
L		0.038(MAX)	0.965(MAX)
L1		0.067±0.008	1.702 ±0.203
S		0.047(MAX)	1.194(MAX)
y		0.004(MAX)	0.102(MAX)
Θ		0°~10°	0°~10°



PACKAGE OUTLINE DIMENSION

28 pin 8x13.4mm sTSP Package Outline Dimension



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.00	1.10	1.20	0.040	0.043	0.047
A1	0.05	-	0.15	0.002	-	0.006
A2	0.91	1.00	1.05	0.036	0.039	0.041
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.07	0.15	0.23	0.003	0.006	0.009
HD	13.20	13.40	13.60	0.520	0.528	0.535
D	11.60	11.80	12.00	0.457	0.465	0.472
E	7.80	8.00	8.20	0.307	0.315	0.323
e	-	0.55	-	-	0.0216	-
L	0.30	0.50	0.70	0.012	0.020	0.028
L1	0.675	-	-	0.027	-	-
Y	0.00	-	0.076	0.000	-	0.003
θ	0°	3°	5°	0°	3°	5°



Lyontek Inc.

LY62256B

Rev. 1.4

32K X 8 BIT LOW POWER CMOS SRAM

ORDERING INFORMATION

Package Type	Access Time (Speed)(ns)	Power Type	Temperature Range(°C)	Packing Type	Lyontek Item No.
28-pin 330mil SOP	45	Special Ultra Low Power	-40°C ~85°C	Tray	LY62256BSL-45SLI
				Tape Reel	LY62256BSL-45SLIT
28-pin 8mmx13.4mm sTSP	45	Special Ultra Low Power	-40°C ~85°C	Tray	LY62256BRL-45SLI
				Tape Reel	LY62256BRL-45SLIT



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LY62256B

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32K X 8 BIT LOW POWER CMOS SRAM

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