



#### REVISION HISTORY

<u>Revision</u>	<u>Description</u>	<u>Issue Date</u>
Rev. 1.0	Initial Issue	Jul.25.2004
Rev. 2.0	Revised Vcc Range 4.5~5.5V => 2.7~5.5V	May.3.2005
Rev. 2.1	Revised I <sub>SB1</sub>	May.13.2005
Rev. 2.2	Adding PKG type : skinny P-DIP	Aug.29.2005
Rev. 2.3	Revised V <sub>IH</sub> (min)=2.4V, V <sub>IL</sub> (max)=0.6V	Feb.24.2006
Rev. 2.4	Revised V <sub>IH</sub> (min)=2.4V, V <sub>IL</sub> (max)=0.6V (VCC=2.7~3.6V) V <sub>IH</sub> (min)=2.4V, V <sub>IL</sub> (max)=0.8V (VCC=4.5~5.5V)	Jul.31.2006
Rev. 2.5	Revised <b>STSOP Package Outline Dimension</b>	Mar.26.2008
Rev. 2.6	Added SL grade Added I <sub>SB1</sub> /I <sub>DR</sub> values when T <sub>A</sub> = 25°C and T <sub>A</sub> = 40°C Revised <b>FEATURES &amp; ORDERING INFORMATION</b> <b>Lead free</b> <b>and green package available</b> to <b>Green package available</b> Added packing type in <b>ORDERING INFORMATION</b> Revised I <sub>SB1(MAX)</sub> Revised V <sub>TERM</sub> to V <sub>T1</sub> and V <sub>T2</sub> Revised Test Condition of I <sub>SB1</sub> /I <sub>DR</sub> Deleted T <sub>SOLDER</sub> in <b>ABSOLUTE MAXIMUM RATINGS</b>	Mar.30.2009
Rev. 2.7	Revised <b>PACKAGE OUTLINE DIMENSION</b> in page 10	May.7.2010
Rev. 2.8	Revised <b>ORDERING INFORMATION</b> in page 12 Revised <b>PACKAGE OUTLINE DIMENSION</b> in page 9	Aug.25.2010
Rev. 2.9	Deleted <b>WRITE CYCLE</b> Notes : 1. WE#, CE# must be high or CE2 must be low during all address transitions in page 6	Jun.28.2016
Rev. 2.10	Corrected <b>ORDERING INFORMATION</b> Typo in page 13.	Jul.21.2016
Rev. 2.11	Revised <b>PACKAGE OUTLINE DIMENSION</b> in page 8	Jan.08.2025

## FEATURES

- Fast access time : 35/55/70ns
- Low power consumption:  
Operating current : 20/15/10mA (TYP.)  
Standby current : 1 $\mu$ A (TYP.)
- Single 2.7~5.5V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data retention voltage : 1.5V (MIN.)
- **Green package available**
- Package : 28-pin 600 mil PDIP  
28-pin 330 mil SOP  
28-pin 8mm x 13.4mm sTSSOP  
28-pin 300 mil Skinny PDIP

## GENERAL DESCRIPTION

The LY6264 is a 65,536-bit low power CMOS static random access memory organized as 8,192 words by 8 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

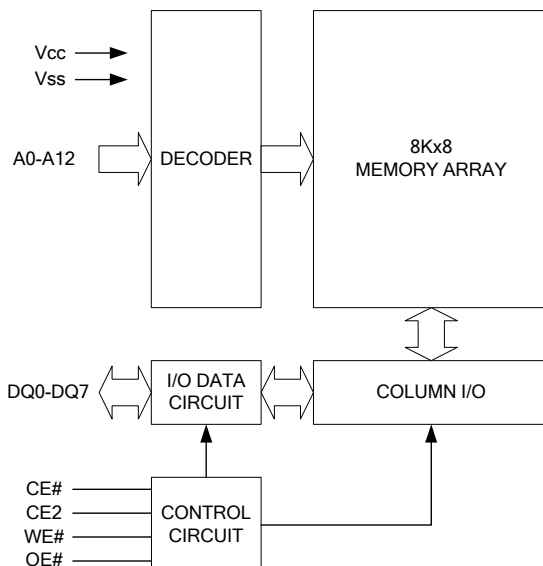
The LY6264 is well designed for very low power system applications, and particularly well suited for battery back-up nonvolatile memory application.

The LY6264 operates from a single power supply of 2.7~5.5V and all inputs and outputs are fully TTL compatible

## PRODUCT FAMILY

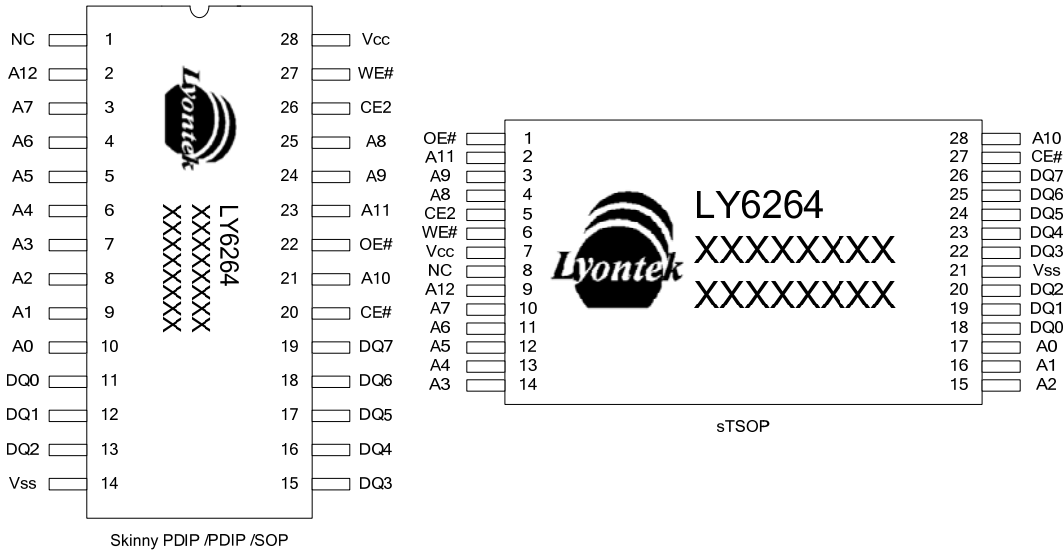
Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation	
				Standby(I <sub>SB1</sub> ,TYP.)	Operating(I <sub>CC</sub> ,TYP.)
LY6264	0 ~ 70°C	2.7 ~ 5.5V	35/55/70ns	1 $\mu$ A	20/15/10mA
LY6264(E)	-20 ~ 80°C	2.7 ~ 5.5V	35/55/70ns	1 $\mu$ A	20/15/10mA
LY6264(I)	-40 ~ 85°C	2.7 ~ 5.5V	35/55/70ns	1 $\mu$ A	20/15/10mA

## FUNCTIONAL BLOCK DIAGRAM



## PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A12	Address Inputs
DQ0 - DQ7	Data Inputs/Outputs
CE#, CE2	Chip Enable Inputs
WE#	Write Enable Input
OE#	Output Enable Input
Vcc	Power Supply
Vss	Ground
NC	No Connection

**PIN CONFIGURATION**

**ABSOLUTE MAXIMUN RATINGS\***

PARAMETER	SYMBOL	RATING	UNIT
Voltage on Vcc relative to Vss	V <sub>T1</sub>	-0.5 to 6.5	V
Voltage on any other pin relative to Vss	V <sub>T2</sub>	-0.5 to Vcc+0.5	V
Operating Temperature	T <sub>A</sub>	0 to 70(C grade)	°C
		-20 to 80(E grade)	
		-40 to 85(I grade)	
Storage Temperature	T <sub>STG</sub>	-65 to 150	°C
Power Dissipation	P <sub>D</sub>	1	W
DC Output Current	I <sub>OUT</sub>	50	mA

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

**TRUTH TABLE**

MODE	CE#	CE2	OE#	WE#	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	X	High-Z	I <sub>SB</sub> , I <sub>SB1</sub>
	X	L	X	X	High-Z	I <sub>SB</sub> , I <sub>SB1</sub>
Output Disable	L	H	H	H	High-Z	I <sub>CC</sub> , I <sub>CC1</sub>
Read	L	H	L	H	D <sub>OUT</sub>	I <sub>CC</sub> , I <sub>CC1</sub>
Write	L	H	X	L	D <sub>IN</sub>	I <sub>CC</sub> , I <sub>CC1</sub>

Note: H = V<sub>IH</sub>, L = V<sub>IL</sub>, X = Don't care.



#### DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.*4	MAX.	UNIT		
Supply Voltage	V <sub>CC</sub>		2.7	3.3	5.5	V		
Input High Voltage	V <sub>IH</sub> *1		2.4	-	V <sub>CC</sub> +0.5	V		
Input Low Voltage	V <sub>IL</sub> *2	V <sub>CC</sub> =2.7~3.6V	-0.5	-	0.6	V		
		V <sub>CC</sub> =4.5~5.5V	-0.5	-	0.8	V		
Input Leakage Current	I <sub>LI</sub>	V <sub>CC</sub> ≥ V <sub>IN</sub> ≥ V <sub>SS</sub>	-1	-	1	μA		
Output Leakage Current	I <sub>LO</sub>	V <sub>CC</sub> ≥ V <sub>OUT</sub> ≥ V <sub>SS</sub> , Output Disabled	-1	-	1	μA		
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -1mA	2.4	3.0	-	V		
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2mA	-	-	0.4	V		
Average Operating Power supply Current	I <sub>CC</sub>	Cycle time = Min. CE# = V <sub>IL</sub> and CE2 = V <sub>IH</sub> , I <sub>I/O</sub> = 0mA Other pins at V <sub>IL</sub> or V <sub>IH</sub>	-35	-	20	50	mA	
			-55	-	15	45	mA	
			-70	-	10	40	mA	
	I <sub>CC1</sub>	Cycle time = 1μs CE# ≤ 0.2V and CE2 ≥ V <sub>CC</sub> -0.2V,, I <sub>I/O</sub> = 0mA other pins at 0.2V or V <sub>CC</sub> -0.2V	-	3	10	mA		
Standby Power Supply Current	I <sub>SB</sub>	CE# = V <sub>IH</sub> or CE2 = V <sub>IL</sub> Other pins at V <sub>IL</sub> or V <sub>IH</sub>	-	1	3	mA		
			I <sub>SB1</sub>	CE# ≥ V <sub>CC</sub> -0.2V or CE2 ≤ 0.2V Others at 0.2V or V <sub>CC</sub> - 0.2V	LL	-	1	20
	LLE/LLI	-			1	30	μA	
	SL*5	25°C			-	1	3	μA
	SLE*5				-	1	3	μA
	SLI*5	40°C			-	1.5	4	μA
	SL		-	1	10	μA		
SLE/SLI	-	1	20	μA				

Notes:

- V<sub>IH</sub>(max) = V<sub>CC</sub> + 3.0V for pulse width less than 10ns.
- V<sub>IL</sub>(min) = V<sub>SS</sub> - 3.0V for pulse width less than 10ns.
- Over/Undershoot specifications are characterized, not 100% tested.
- Typical values are included for reference only and are not guaranteed or tested.  
Typical valued are measured at V<sub>CC</sub> = V<sub>CC</sub>(TYP.) and T<sub>A</sub> = 25°C
- This parameter is measured at V<sub>CC</sub> = 3.0V



### CAPACITANCE (TA = 25°C, f = 1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C <sub>IN</sub>	-	6	pF
Input/Output Capacitance	C <sub>I/O</sub>	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

### AC TEST CONDITIONS

Input Pulse Levels	0.2V to V <sub>CC</sub> - 0.2V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	C <sub>L</sub> = 50pF + 1TTL, I <sub>OH</sub> /I <sub>OL</sub> = -1mA/2mA

### AC ELECTRICAL CHARACTERISTICS

#### (1) READ CYCLE

PARAMETER	SYM.	LY6264-35		LY6264-55		LY6264-70		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t <sub>RC</sub>	35	-	55	-	70	-	ns
Address Access Time	t <sub>AA</sub>	-	35	-	55	-	70	ns
Chip Enable Access Time	t <sub>ACE</sub>	-	35	-	55	-	70	ns
Output Enable Access Time	t <sub>OE</sub>	-	25	-	30	-	35	ns
Chip Enable to Output in Low-Z	t <sub>CLZ</sub> *	10	-	10	-	10	-	ns
Output Enable to Output in Low-Z	t <sub>OLZ</sub> *	5	-	5	-	5	-	ns
Chip Disable to Output in High-Z	t <sub>CHZ</sub> *	-	15	-	20	-	25	ns
Output Disable to Output in High-Z	t <sub>OHZ</sub> *	-	15	-	20	-	25	ns
Output Hold from Address Change	t <sub>OH</sub>	10	-	10	-	10	-	ns

#### (2) WRITE CYCLE

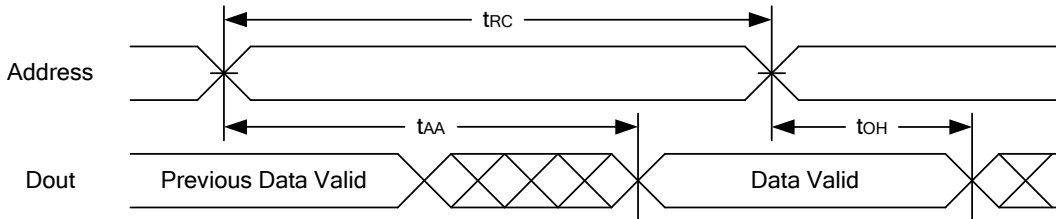
PARAMETER	SYM.	LY6264-35		LY6264-55		LY6264-70		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t <sub>WC</sub>	35	-	55	-	70	-	ns
Address Valid to End of Write	t <sub>AW</sub>	30	-	50	-	60	-	ns
Chip Enable to End of Write	t <sub>CW</sub>	30	-	50	-	60	-	ns
Address Set-up Time	t <sub>AS</sub>	0	-	0	-	0	-	ns
Write Pulse Width	t <sub>WP</sub>	25	-	45	-	55	-	ns
Write Recovery Time	t <sub>WR</sub>	0	-	0	-	0	-	ns
Data to Write Time Overlap	t <sub>DW</sub>	20	-	25	-	30	-	ns
Data Hold from End of Write Time	t <sub>DH</sub>	0	-	0	-	0	-	ns
Output Active from End of Write	t <sub>OW</sub> *	5	-	5	-	5	-	ns
Write to Output in High-Z	t <sub>WHZ</sub> *	-	15	-	20	-	25	ns

\*These parameters are guaranteed by device characterization, but not production tested.

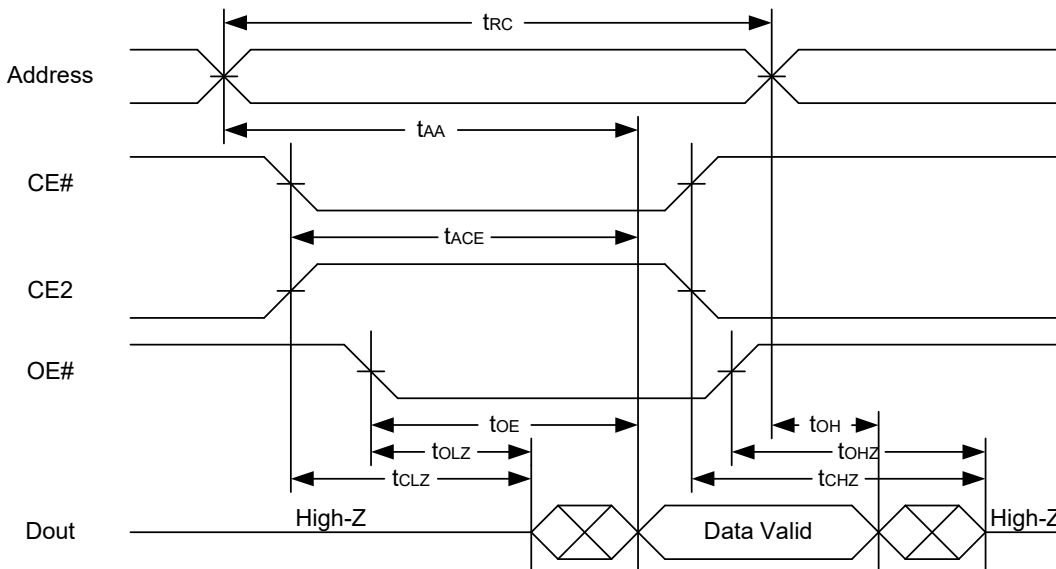


### TIMING WAVEFORMS

#### READ CYCLE 1 (Address Controlled) (1,2)

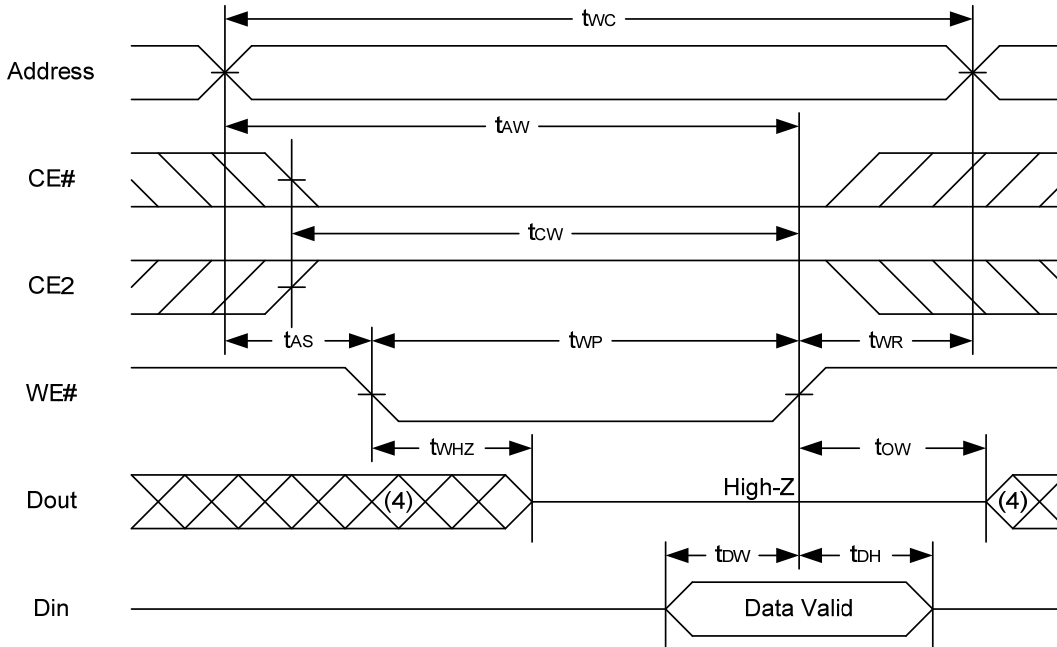
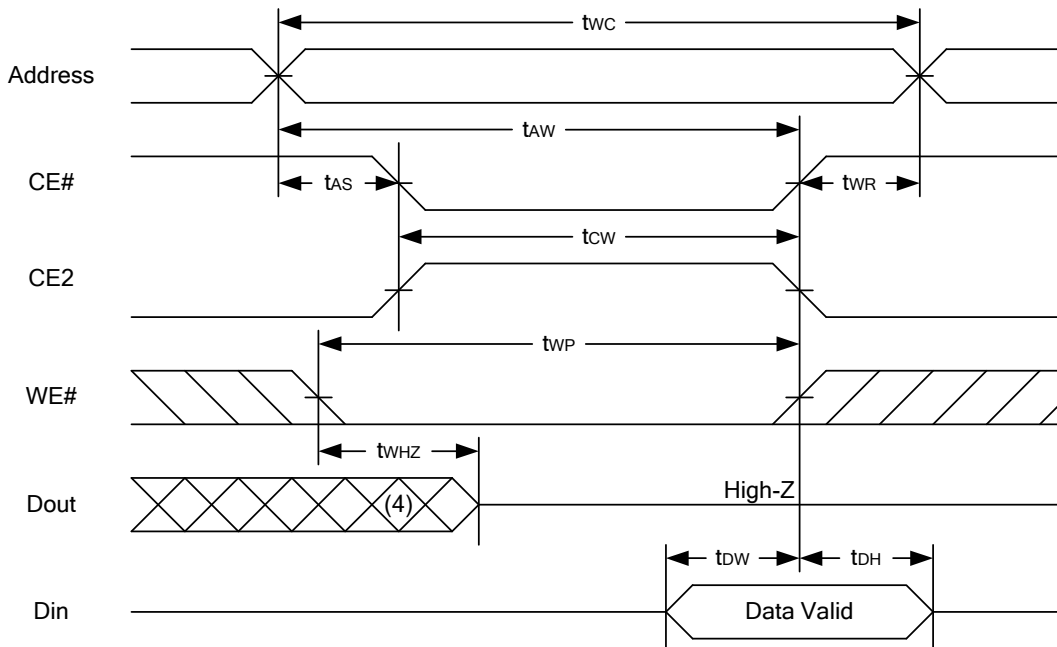


#### READ CYCLE 2 (CE# and CE2 and OE# Controlled) (1,3,4,5)



Notes :

1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low., CE2 = high.
3. Address must be valid prior to or coincident with CE# = low, CE2 = high; otherwise  $t_{AA}$  is the limiting parameter.
4.  $t_{CLZ}$ ,  $t_{OLZ}$ ,  $t_{CHZ}$  and  $t_{OHZ}$  are specified with  $C_L = 5pF$ . Transition is measured  $\pm 500mV$  from steady state.
5. At any given temperature and voltage condition,  $t_{CHZ}$  is less than  $t_{CLZ}$ ,  $t_{OHZ}$  is less than  $t_{OLZ}$ .

**WRITE CYCLE 1 (WE# Controlled) (1,2,4,5)**

**WRITE CYCLE 2 (CE# and CE2 Controlled) (1,4,5)**

**Notes :**

1. A write occurs during the overlap of a low CE#, high CE2, low WE#.
2. During a WE#-controlled write cycle with OE# low, twp must be greater than twhz + tdw to allow the drivers to turn off and data to be placed on the bus.
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the CE# low transition and CE2 high transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
5. tow and twhz are specified with CL = 5pF. Transition is measured ±500mV from steady state.

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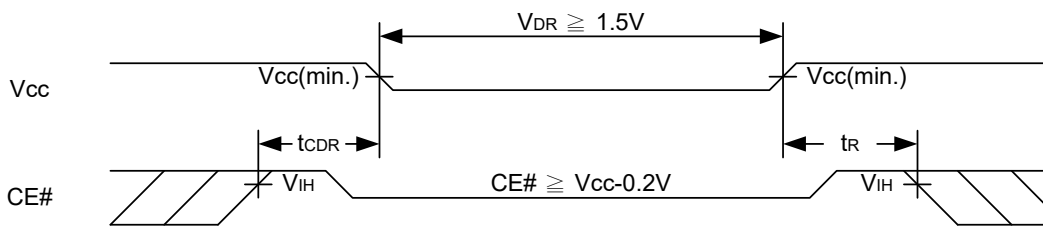
### DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT		
V <sub>CC</sub> for Data Retention	V <sub>DR</sub>	CE# ≥ V <sub>CC</sub> - 0.2V or CE2 ≤ 0.2V	1.5	-	5.5	V		
Data Retention Current	I <sub>DR</sub>	V <sub>CC</sub> = 1.5V CE# ≥ V <sub>CC</sub> - 0.2V or CE2 ≤ 0.2V Othersat 0.2V or V <sub>CC</sub> -0.2V	LL/LLE/LLI	-	0.5	20	μA	
			SL	25°C	-	0.5	2	μA
			SLE	40°C	-	1	3	μA
			SLI	-	-	0.5	8	μA
			SLE/SLI	-	-	0.5	15	μA
Chip Disable to Data Retention Time	t <sub>CDR</sub>	See Data Retention Waveforms (below)	0	-	-	ns		
Recovery Time	t <sub>R</sub>		t <sub>RC</sub> *	-	-	ns		

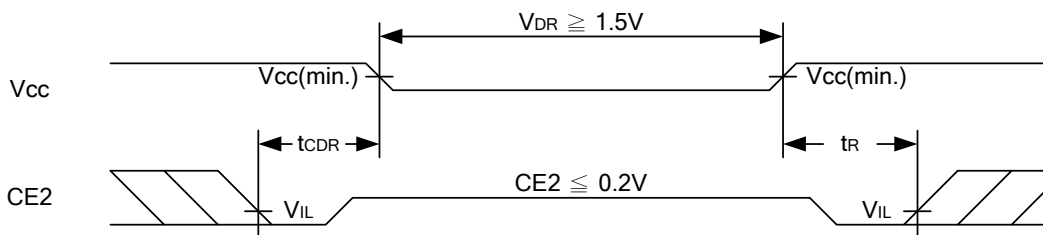
t<sub>RC</sub>\* = Read Cycle Time

### DATA RETENTION WAVEFORM

#### Low V<sub>CC</sub> Data Retention Waveform (1) (CE# controlled)



#### Low V<sub>CC</sub> Data Retention Waveform (2) (CE2 controlled)

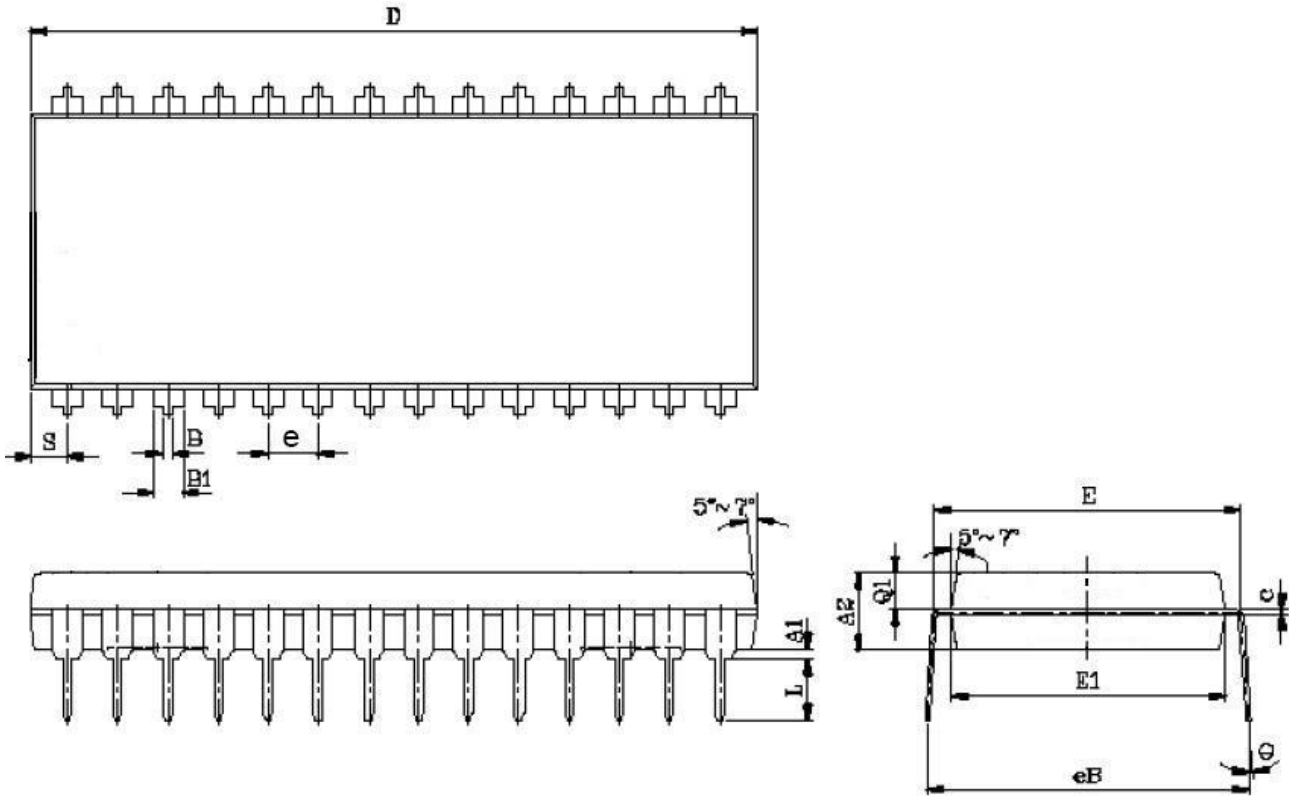






### PACKAGE OUTLINE DIMENSION

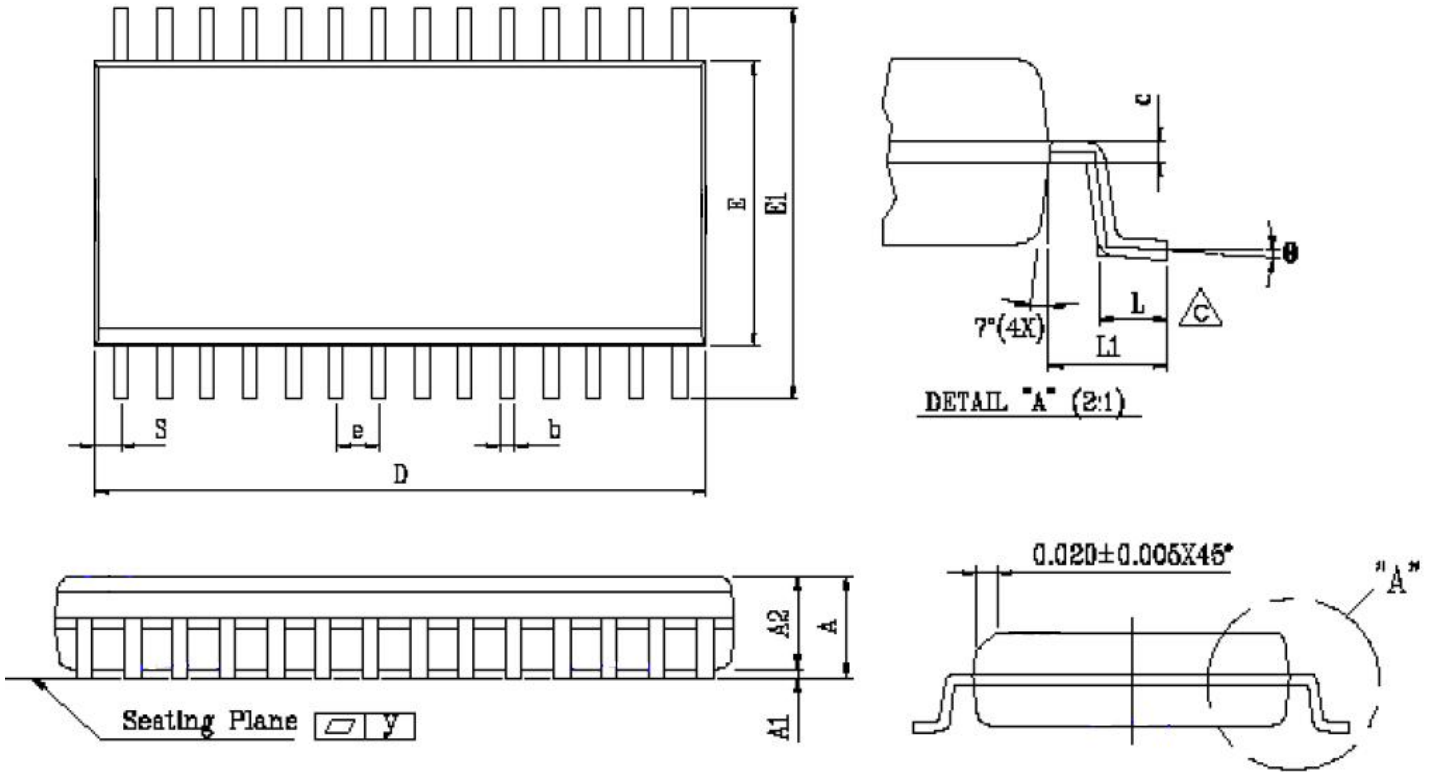
28 pin 600 mil PDIP Package Outline Dimension



SYM.	UNIT	INCH.(BASE)	MM(REF)
A1		0.015(MIN)	0.381(MIN)
A2		0.155±0.005	3.937±0.127
B		0.020(MAX)	0.508(MAX)
B1		0.060(TYP)	1.524(TYP)
c		0.012(MAX)	0.304(MAX)
D		1.470(MAX)	37.338(MAX)
E		0.6(TYP)	15.24(TYP)
E1		0.55(MAX)	13.970(MAX)
e		0.100(TYP)	2.540(TYP)
eB		0.650±0.020	16.510±0.508
L		0.200(MAX)	5.080(MAX)
S		0.06(MAX)	1.524(MAX)
Q1		0.08(MAX)	2.032(MAX)
θ		15°(MAX)	15°(MAX)



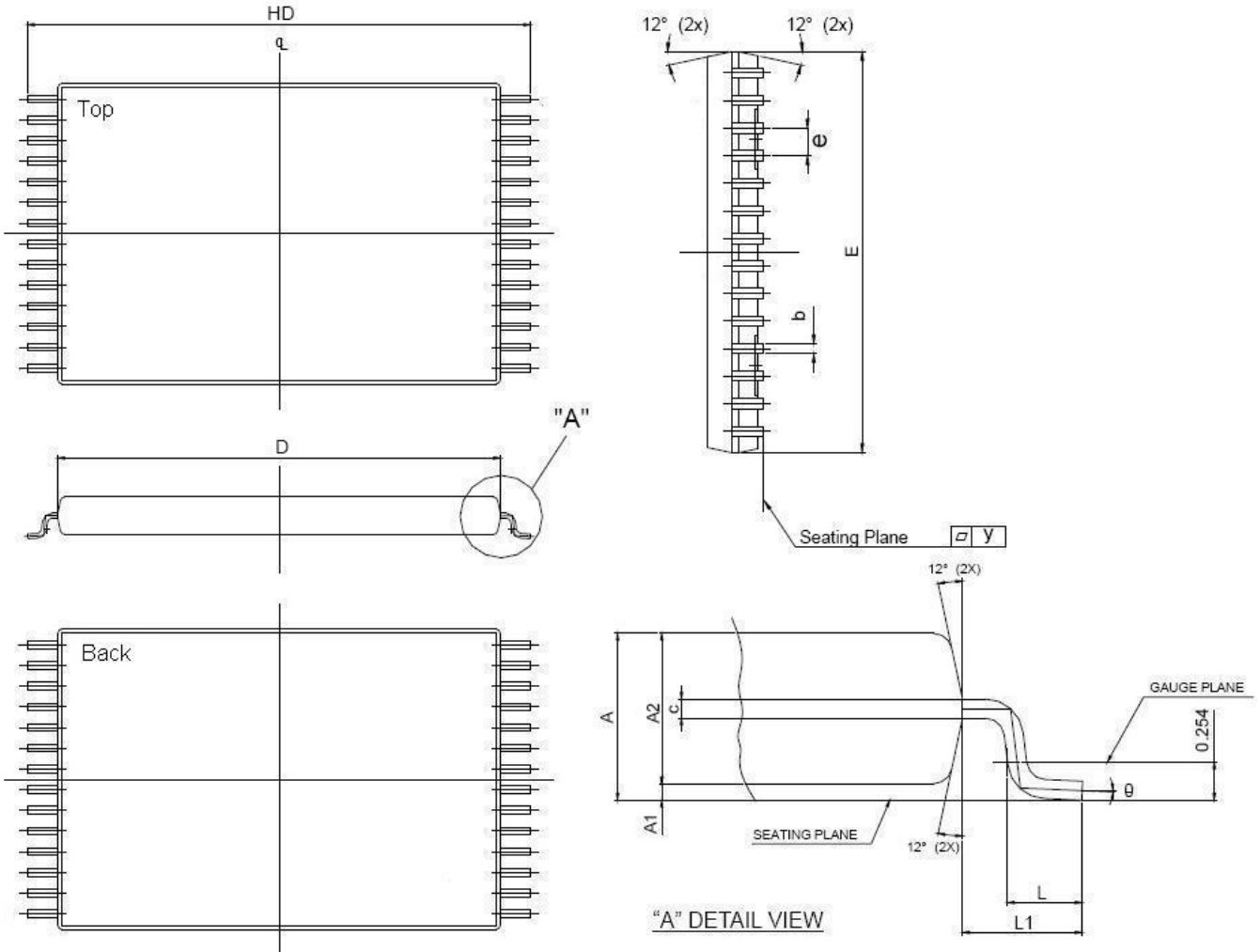
**28 pin 330 mil SOP Package Outline Dimension**



SYM.	UNIT	
	INCH(BASE)	MM(REF)
A	0.120(MAX)	3.048(MAX)
A1	0.002(MIN)	0.05(MIN)
A2	0.098±0.005	2.489±0.127
b	0.016(TYP)	0.406(TYP)
c	0.010(TYP)	0.254(TYP)
D	0.728(MAX)	18.491(MAX)
E	0.340(MAX)	8.636(MAX)
E1	0.465±0.012	11.811±0.305
e	0.050(TYP)	1.270(TYP)
L	0.038(MAX)	0.965(MAX)
L1	0.067±0.008	1.702 ±0.203
S	0.047(MAX)	1.194(MAX)
y	0.004(MAX)	0.102(MAX)
∅	0°~10°	0°~10°

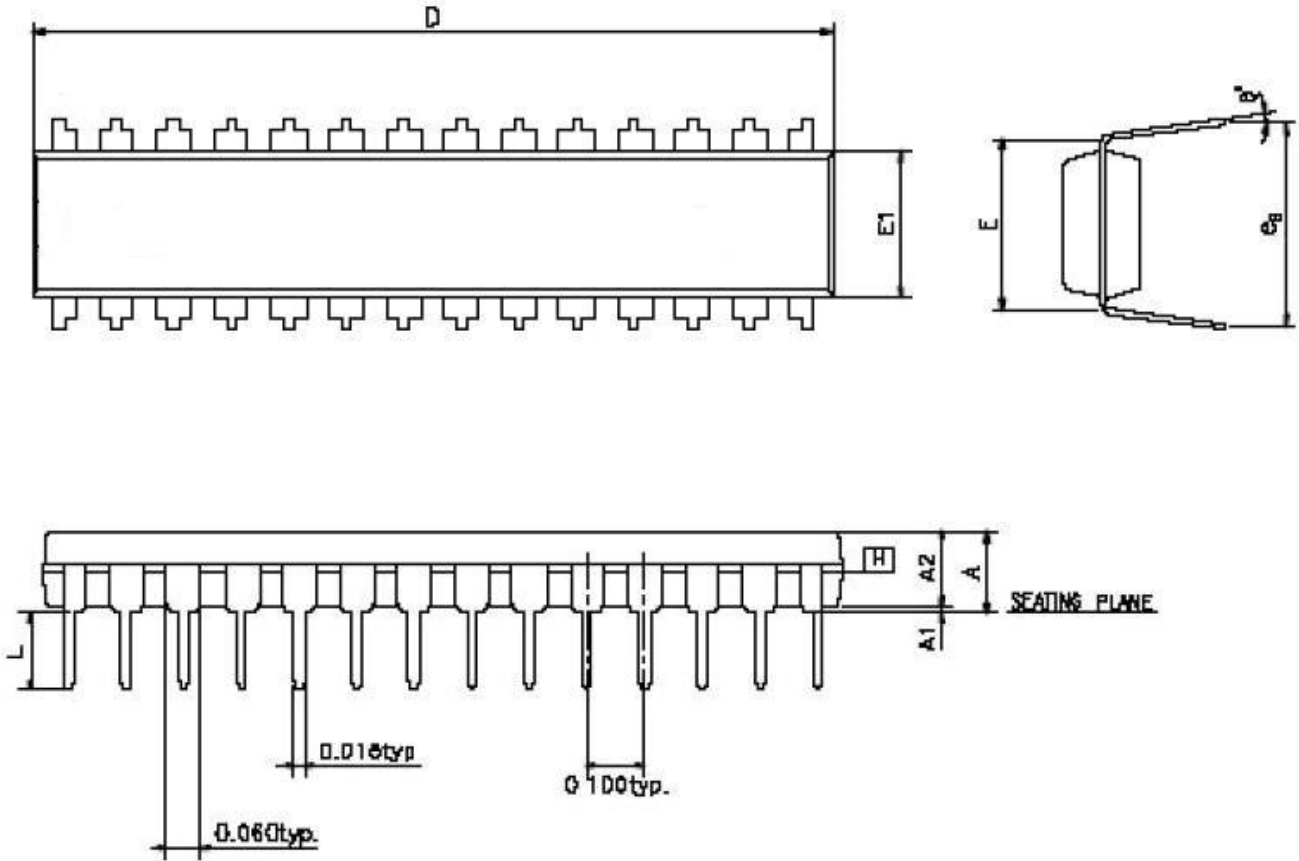


**28 pin 8x13.4mm sTSP Package Outline Dimension**



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.00	1.10	1.20	0.040	0.043	0.047
A1	0.05	-	0.15	0.002	-	0.006
A2	0.91	1.00	1.05	0.036	0.039	0.041
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.07	0.15	0.23	0.003	0.006	0.009
HD	13.20	13.40	13.60	0.520	0.528	0.535
D	11.60	11.80	12.00	0.457	0.465	0.472
E	7.80	8.00	8.20	0.307	0.315	0.323
e	-	0.55	-	-	0.0216	-
L	0.30	0.50	0.70	0.012	0.020	0.028
L1	0.675	-	-	0.027	-	-
Y	0.00	-	0.076	0.000	-	0.003
θ	0°	3°	5°	0°	3°	5°

#### 28 pin 300 mil PDIP Package Outline Dimension



SYMBOLS	MIN.	NOR.	MAX.
A	—	—	0.210
A1	0.015	—	—
A2	0.125	0.130	0.135
D	1.385	1.390	1.400
E	0.310 BSC		
E1	0.283	0.288	0.293
L	0.115	0.130	0.150
eB	0.330	0.350	0.370
θ°	0	7	15

UNIT : INCH

NOTE:

1. JEDEC OUTLINE : MS-D15 AH



#### ORDERING INFORMATION

Package Type	Access Time (Speed)(ns)	Power Type	Temperature Range(°C)	Packing Type	Lyontek Item No.
28-pin 600mil PDIP	35	Ultra Low Power	0°C~70°C	Tube	LY6264PL-35LL
			-20°C~80°C	Tube	LY6264PL-35LLE
			-40°C~85°C	Tube	LY6264PL-35LLI
		Special Ultra Low Power	0°C~70°C	Tube	LY6264PL-35SL
			-20°C~80°C	Tube	LY6264PL-35SLE
			-40°C~85°C	Tube	LY6264PL-35SLI
	55	Ultra Low Power	0°C~70°C	Tube	LY6264PL-55LL
			-20°C~80°C	Tube	LY6264PL-55LLE
			-40°C~85°C	Tube	LY6264PL-55LLI
		Special Ultra Low Power	0°C~70°C	Tube	LY6264PL-55SL
			-20°C~80°C	Tube	LY6264PL-55SLE
			-40°C~85°C	Tube	LY6264PL-55SLI
	70	Ultra Low Power	0°C~70°C	Tube	LY6264PL-70LL
			-20°C~80°C	Tube	LY6264PL-70LLE
			-40°C~85°C	Tube	LY6264PL-70LLI
Special Ultra Low Power		0°C~70°C	Tube	LY6264PL-70SL	
		-20°C~80°C	Tube	LY6264PL-70SLE	
		-40°C~85°C	Tube	LY6264PL-70SLI	

**ORDERING INFORMATION**

Package Type	Access Time (Speed)(ns)	Power Type	Temperature Range(°C)	Packing Type	Lyontek Item No.
28-pin 330mil SOP	35	Ultra Low Power	0°C~70°C	Tube	LY6264SL-35LL
				Tape Reel	LY6264SL-35LLT
			-20°C~80°C	Tube	LY6264SL-35LLE
				Tape Reel	LY6264SL-35LLET
			-40°C~85°C	Tube	LY6264SL-35LLI
				Tape Reel	LY6264SL-35LLIT
		Special Ultra Low Power	0°C~70°C	Tube	LY6264SL-35SL
				Tape Reel	LY6264SL-35SLT
			-20°C~80°C	Tube	LY6264SL-35SLE
				Tape Reel	LY6264SL-35SLET
			-40°C~85°C	Tube	LY6264SL-35SLI
				Tape Reel	LY6264SL-35SLIT
	55	Ultra Low Power	0°C~70°C	Tube	LY6264SL-55LL
				Tape Reel	LY6264SL-55LLT
			-20°C~80°C	Tube	LY6264SL-55LLE
				Tape Reel	LY6264SL-55LLET
			-40°C~85°C	Tube	LY6264SL-55LLI
				Tape Reel	LY6264SL-55LLIT
		Special Ultra Low Power	0°C~70°C	Tube	LY6264SL-55SL
				Tape Reel	LY6264SL-55SLT
			-20°C~80°C	Tube	LY6264SL-55SLE
				Tape Reel	LY6264SL-55SLET
			-40°C~85°C	Tube	LY6264SL-55SLI
				Tape Reel	LY6264SL-55SLIT
70	Ultra Low Power	0°C~70°C	Tube	LY6264SL-70LL	
			Tape Reel	LY6264SL-70LLT	
		-20°C~80°C	Tube	LY6264SL-70LLE	
			Tape Reel	LY6264SL-70LLET	
		-40°C~85°C	Tube	LY6264SL-70LLI	
			Tape Reel	LY6264SL-70LLIT	
	Special Ultra Low Power	0°C~70°C	Tube	LY6264SL-70SL	
			Tape Reel	LY6264SL-70SLT	
		-20°C~80°C	Tube	LY6264SL-70SLE	
			Tape Reel	LY6264SL-70SLET	
		-40°C~85°C	Tube	LY6264SL-70SLI	
			Tape Reel	LY6264SL-70SLIT	



#### ORDERING INFORMATION

Package Type	Access Time (Speed)(ns)	Power Type	Temperature Range(°C)	Packing Type	Lyontek Item No.
28-pin 8mmx13.4mm sTSOP	35	Ultra Low Power	0°C~70°C	Tray	LY6264RL-35LL
				Tape Reel	LY6264RL-35LLT
			-20°C~80°C	Tray	LY6264RL-35LLE
				Tape Reel	LY6264RL-35LLET
			-40°C~85°C	Tray	LY6264RL-35LLI
				Tape Reel	LY6264RL-35LLIT
		Special Ultra Low Power	0°C~70°C	Tray	LY6264RL-35SL
				Tape Reel	LY6264RL-35SLT
			-20°C~80°C	Tray	LY6264RL-35SLE
				Tape Reel	LY6264RL-35SLET
			-40°C~85°C	Tray	LY6264RL-35SLI
				Tape Reel	LY6264RL-35SLIT
	55	Ultra Low Power	0°C~70°C	Tray	LY6264RL-55LL
				Tape Reel	LY6264RL-55LLT
			-20°C~80°C	Tray	LY6264RL-55LLE
				Tape Reel	LY6264RL-55LLET
			-40°C~85°C	Tray	LY6264RL-55LLI
				Tape Reel	LY6264RL-55LLIT
		Special Ultra Low Power	0°C~70°C	Tray	LY6264RL-55SL
				Tape Reel	LY6264RL-55SLT
			-20°C~80°C	Tray	LY6264RL-55SLE
				Tape Reel	LY6264RL-55SLET
			-40°C~85°C	Tray	LY6264RL-55SLI
				Tape Reel	LY6264RL-55SLIT
70	Ultra Low Power	0°C~70°C	Tray	LY6264RL-70LL	
			Tape Reel	LY6264RL-70LLT	
		-20°C~80°C	Tray	LY6264RL-70LLE	
			Tape Reel	LY6264RL-70LLET	
		-40°C~85°C	Tray	LY6264RL-70LLI	
			Tape Reel	LY6264RL-70LLIT	
	Special Ultra Low Power	0°C~70°C	Tray	LY6264RL-70SL	
			Tape Reel	LY6264RL-70SLT	
		-20°C~80°C	Tray	LY6264RL-70SLE	
			Tape Reel	LY6264RL-70SLET	
		-40°C~85°C	Tray	LY6264RL-70SLI	
			Tape Reel	LY6264RL-70SLIT	



#### ORDERING INFORMATION

Package Type	Access Time (Speed)(ns)	Power Type	Temperature Range(°C)	Packing Type	Lyontek Item No.
28-pin 300mil PDIP	35	Ultra Low Power	0°C~70°C	Tube	LY6264DL-35LL
			-20°C~80°C	Tube	LY6264DL-35LLE
			-40°C~85°C	Tube	LY6264DL-35LLI
		Special Ultra Low Power	0°C~70°C	Tube	LY6264DL-35SL
			-20°C~80°C	Tube	LY6264DL-35SLE
			-40°C~85°C	Tube	LY6264DL-35SLI
	55	Ultra Low Power	0°C~70°C	Tube	LY6264DL-55LL
			-20°C~80°C	Tube	LY6264DL-55LLE
			-40°C~85°C	Tube	LY6264DL-55LLI
		Special Ultra Low Power	0°C~70°C	Tube	LY6264DL-55SL
			-20°C~80°C	Tube	LY6264DL-55SLE
			-40°C~85°C	Tube	LY6264DL-55SLI
	70	Ultra Low Power	0°C~70°C	Tube	LY6264DL-70LL
			-20°C~80°C	Tube	LY6264DL-70LLE
			-40°C~85°C	Tube	LY6264DL-70LLI
Special Ultra Low Power		0°C~70°C	Tube	LY6264DL-70SL	
		-20°C~80°C	Tube	LY6264DL-70SLE	
		-40°C~85°C	Tube	LY6264DL-70SLI	





**Lyontek Inc.**

**LY6264**

Rev. 2.11

**8K X 8 BIT LOW POWER CMOS SRAM**

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