



### REVISION HISTORY

<u>Revision</u>	<u>Description</u>	<u>Issue Date</u>
Rev. 1.0	Initial Issue	Oct.6.2024
Rev. 1.1	1.Revised Low power consumption: Operating current : 10/8mA (TYP.)→9 mA (TYP.) ---Page1 2. <b><u>PRODUCT FAMILY</u></b> : Power Dissipation: Operating(Icc,TYP.) 10/8mA→9 mA 3. <b><u>DC ELECTRICAL CHARACTERISTICS</u></b> : Average Operating Power supply Current : ICC --- Page3	Mar.9.2026

### FEATURES

- Fast access time : 45ns
- Low power consumption:  
Operating current : 9 mA (TYP.)  
Standby current : 1 $\mu$ A (TYP.)
- Single 2.7~5.5V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data retention voltage : 1.5V (MIN.)
- **Green package available**
- Package : 28-pin 330 mil SOP  
28-pin 8mm x 13.4mm sTSSOP

### GENERAL DESCRIPTION

The LY6264B is a 65,536-bit low power CMOS static random access memory organized as 8,192 words by 8 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

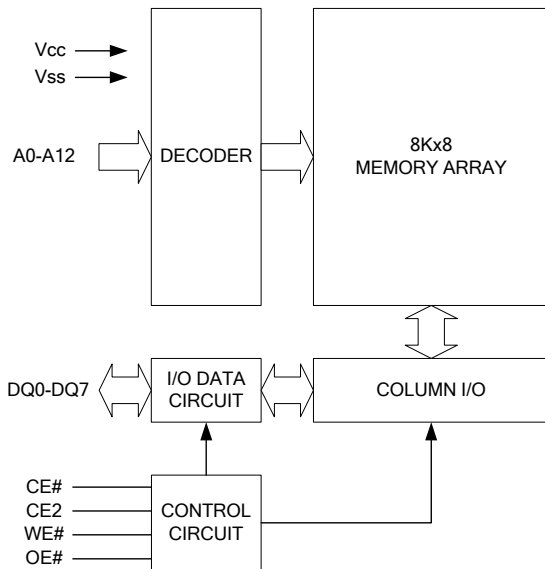
The LY6264B is well designed for very low power system applications, and particularly well suited for battery back-up nonvolatile memory application.

The LY6264B operates from a single power supply of 2.7~5.5V and all inputs and outputs are fully TTL compatible

### PRODUCT FAMILY

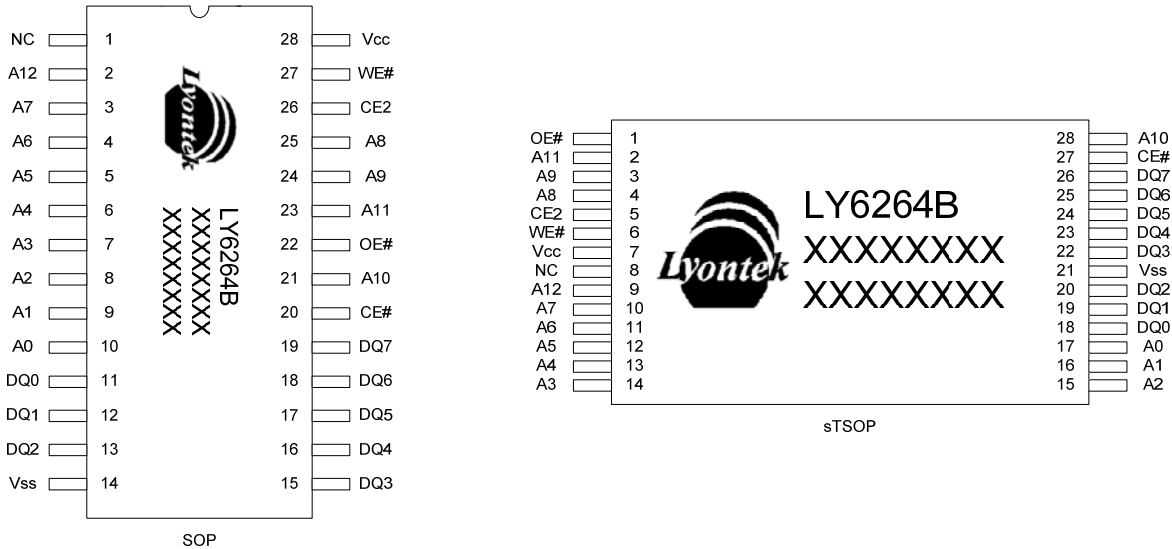
Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation	
				Standby( $I_{SB1}$ , TYP.)	Operating( $I_{CC}$ , TYP.)
LY6264B(I)	-40 ~ 85°C	2.7 ~ 5.5V	45ns	1 $\mu$ A	9 mA

### FUNCTIONAL BLOCK DIAGRAM



### PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A12	Address Inputs
DQ0 - DQ7	Data Inputs/Outputs
CE#, CE2	Chip Enable Inputs
WE#	Write Enable Input
OE#	Output Enable Input
Vcc	Power Supply
Vss	Ground
NC	No Connection

**PIN CONFIGURATION**

**ABSOLUTE MAXIMUM RATINGS\***

PARAMETER	SYMBOL	RATING	UNIT
Voltage on Vcc relative to Vss	V <sub>T1</sub>	-0.5 to 6.5	V
Voltage on any other pin relative to Vss	V <sub>T2</sub>	-0.5 to Vcc+0.5	V
Operating Temperature	T <sub>A</sub>	-40 to 85(I grade)	°C
Storage Temperature	T <sub>STG</sub>	-65 to 150	°C
Power Dissipation	P <sub>D</sub>	1	W
DC Output Current	I <sub>OUT</sub>	50	mA

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

**TRUTH TABLE**

MODE	CE#	CE2	OE#	WE#	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	X	High-Z	I <sub>SB</sub> , I <sub>SB1</sub>
	X	L	X	X	High-Z	I <sub>SB</sub> , I <sub>SB1</sub>
Output Disable	L	H	H	H	High-Z	I <sub>CC</sub> , I <sub>CC1</sub>
Read	L	H	L	H	D <sub>OUT</sub>	I <sub>CC</sub> , I <sub>CC1</sub>
Write	L	H	X	L	D <sub>IN</sub>	I <sub>CC</sub> , I <sub>CC1</sub>

Note: H = V<sub>IH</sub>, L = V<sub>IL</sub>, X = Don't care.



### DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP. <sup>*4</sup>	MAX.	UNIT	
Supply Voltage	V <sub>CC</sub>			2.7	3.3	5.5	V	
Input High Voltage	V <sub>IH</sub> <sup>*1</sup>	V <sub>CC</sub> =2.7~3.6V		2.2	-	V <sub>CC</sub> +0.5	V	
		V <sub>CC</sub> =4.5~5.5V		0.5V <sub>CC</sub>		V <sub>CC</sub> +0.5		
Input Low Voltage	V <sub>IL</sub> <sup>*2</sup>	V <sub>CC</sub> =2.7~3.6V		-0.5	-	0.6	V	
		V <sub>CC</sub> =4.5~5.5V		-0.5	-	0.8	V	
Input Leakage Current	I <sub>LI</sub>	V <sub>CC</sub> ≥ V <sub>IN</sub> ≥ V <sub>SS</sub>		-1	-	1	μA	
Output Leakage Current	I <sub>LO</sub>	V <sub>CC</sub> ≥ V <sub>OUT</sub> ≥ V <sub>SS</sub> , Output Disabled		-1	-	1	μA	
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -1mA		2.4	3.0	-	V	
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2mA		-	-	0.4	V	
Average Operating Power supply Current	I <sub>CC</sub>	Cycle time = Min. CE# = V <sub>IL</sub> and CE2 = V <sub>IH</sub> , I <sub>I/O</sub> = 0mA Other pins at V <sub>IL</sub> or V <sub>IH</sub>	-45	-	9	16	mA	
	I <sub>CC1</sub>	Cycle time = 1μs CE# ≤ 0.2V and CE2 ≥ V <sub>CC</sub> -0.2V,, I <sub>I/O</sub> = 0mA other pins at 0.2V or V <sub>CC</sub> -0.2V		-	2	4	mA	
Standby Power Supply Current	I <sub>SB1</sub>	CE# ≥ V <sub>CC</sub> -0.2V or CE2 ≤ 0.2V Others at 0.2V or V <sub>CC</sub> - 0.2V	SL <sup>*5</sup>	25°C	-	1	3	μA
			SLI <sup>*5</sup>	40°C	-	1.5	3.5	μA
			SL		-	1	5	μA
			SLI		-	1	10	μA

**Notes:**

- V<sub>IH</sub>(max) = V<sub>CC</sub> + 3.0V for pulse width less than 10ns.
- V<sub>IL</sub>(min) = V<sub>SS</sub> - 3.0V for pulse width less than 10ns.
- Over/Undershoot specifications are characterized, not 100% tested.
- Typical values are included for reference only and are not guaranteed or tested.  
Typical values are measured at V<sub>CC</sub> = V<sub>CC</sub>(TYP.) and T<sub>A</sub> = 25°C
- This parameter is measured at V<sub>CC</sub> = 3.0V

**CAPACITANCE** ( $T_A = 25^\circ\text{C}$ ,  $f = 1.0\text{MHz}$ )

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	$C_{IN}$	-	6	pF
Input/Output Capacitance	$C_{I/O}$	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

**AC TEST CONDITIONS**

Input Pulse Levels	0.2V to $V_{CC} - 0.2V$
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	$C_L = 50\text{pF} + 1\text{TTL}$ , $I_{OH}/I_{OL} = -1\text{mA}/2\text{mA}$

**AC ELECTRICAL CHARACTERISTICS****(1) READ CYCLE**

PARAMETER	SYM.	LY6264B-45		UNIT
		MIN.	MAX.	
Read Cycle Time	$t_{RC}$	45	-	ns
Address Access Time	$t_{AA}$	-	45	ns
Chip Enable Access Time	$t_{ACE}$	-	45	ns
Output Enable Access Time	$t_{OE}$	-	20	ns
Chip Enable to Output in Low-Z	$t_{CLZ}^*$	10	-	ns
Output Enable to Output in Low-Z	$t_{OLZ}^*$	5	-	ns
Chip Disable to Output in High-Z	$t_{CHZ}^*$	-	15	ns
Output Disable to Output in High-Z	$t_{OHZ}^*$	-	15	ns
Output Hold from Address Change	$t_{OH}$	10	-	ns

**(2) WRITE CYCLE**

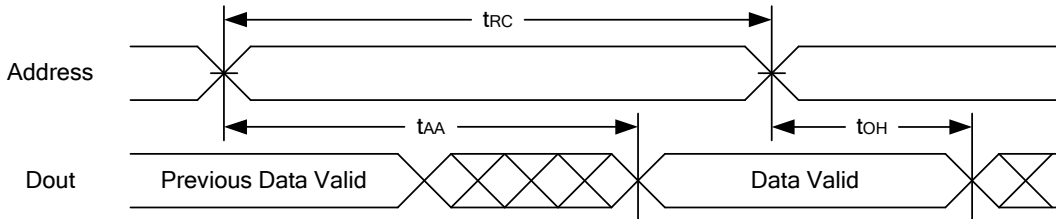
PARAMETER	SYM.	LY6264B-45		UNIT
		MIN.	MAX.	
Write Cycle Time	$t_{WC}$	45	-	ns
Address Valid to End of Write	$t_{AW}$	40	-	ns
Chip Enable to End of Write	$t_{CW}$	40	-	ns
Address Set-up Time	$t_{AS}$	0	-	ns
Write Pulse Width	$t_{WP}$	35	-	ns
Write Recovery Time	$t_{WR}$	0	-	ns
Data to Write Time Overlap	$t_{DW}$	20	-	ns
Data Hold from End of Write Time	$t_{DH}$	0	-	ns
Output Active from End of Write	$t_{OW}^*$	5	-	ns
Write to Output in High-Z	$t_{WHZ}^*$	-	15	ns

\*These parameters are guaranteed by device characterization, but not production tested.

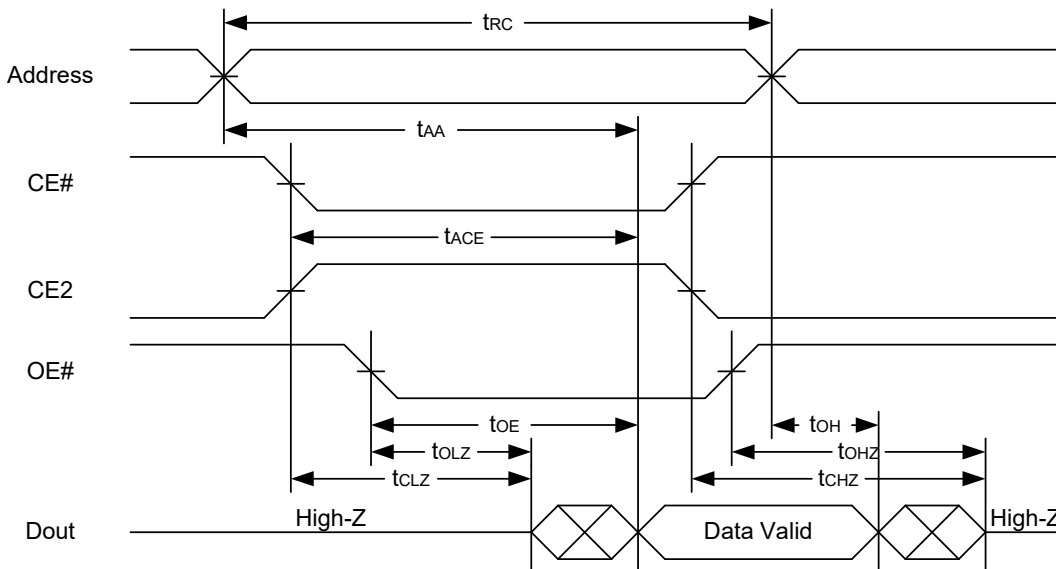


### TIMING WAVEFORMS

#### READ CYCLE 1 (Address Controlled) (1,2)

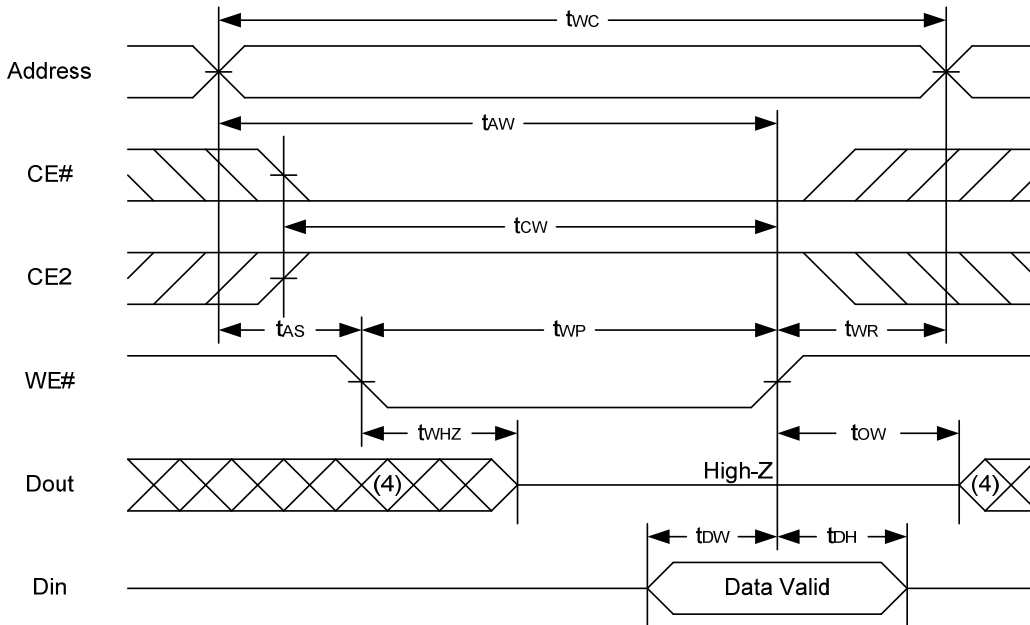
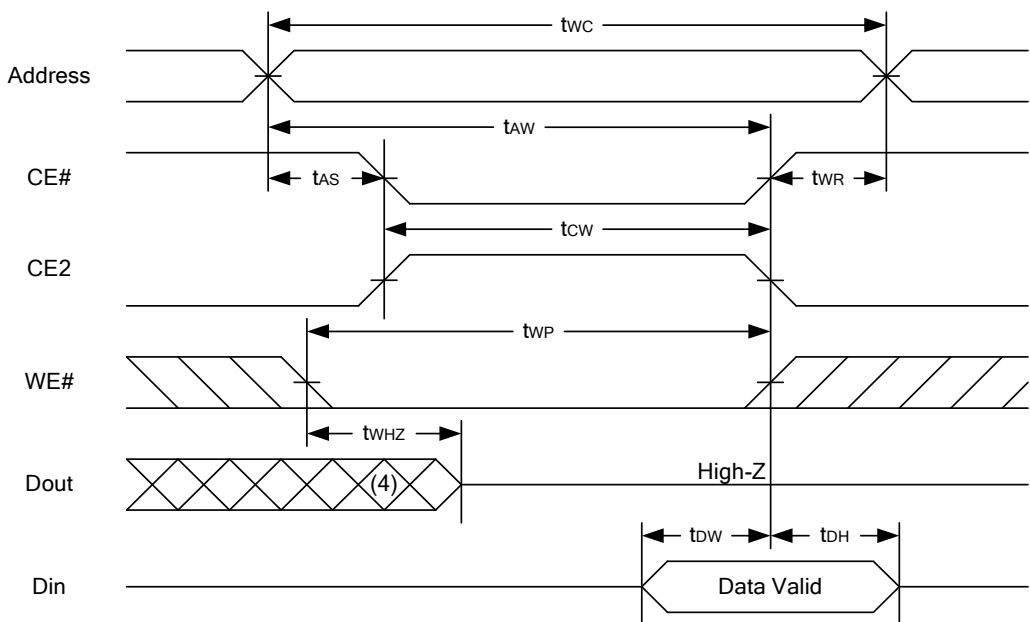


#### READ CYCLE 2 (CE# and CE2 and OE# Controlled) (1,3,4,5)



Notes :

1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low., CE2 = high.
3. Address must be valid prior to or coincident with CE# = low, CE2 = high; otherwise  $t_{AA}$  is the limiting parameter.
4.  $t_{CLZ}$ ,  $t_{OLZ}$ ,  $t_{CHZ}$  and  $t_{OHZ}$  are specified with  $C_L = 5pF$ . Transition is measured  $\pm 500mV$  from steady state.
5. At any given temperature and voltage condition,  $t_{CHZ}$  is less than  $t_{CLZ}$ ,  $t_{OHZ}$  is less than  $t_{OLZ}$ .

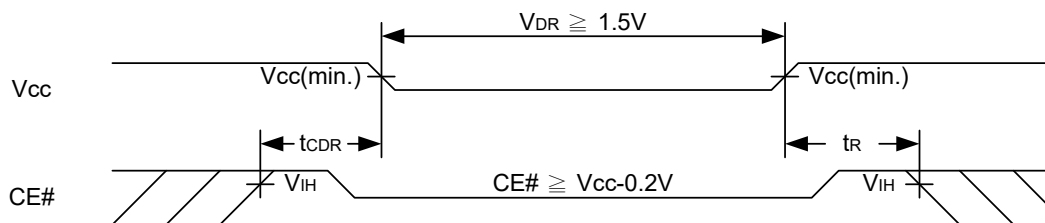
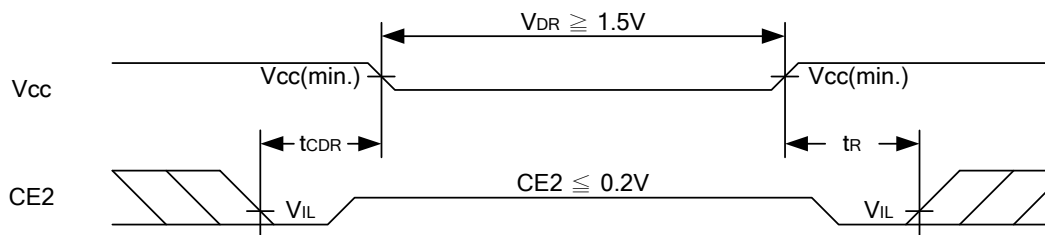
**WRITE CYCLE 1 (WE# Controlled) (1,2,4,5)**

**WRITE CYCLE 2 (CE# and CE2 Controlled) (1,4,5)**

**Notes :**

1. A write occurs during the overlap of a low CE#, high CE2, low WE#.
2. During a WE#-controlled write cycle with OE# low,  $t_{WP}$  must be greater than  $t_{WHZ} + t_{DW}$  to allow the drivers to turn off and data to be placed on the bus.
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the CE# low transition and CE2 high transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
5.  $t_{OW}$  and  $t_{WHZ}$  are specified with  $C_L = 5\text{pF}$ . Transition is measured  $\pm 500\text{mV}$  from steady state.

**DATA RETENTION CHARACTERISTICS**

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT			
V <sub>CC</sub> for Data Retention	V <sub>DR</sub>	CE# ≥ V <sub>CC</sub> - 0.2V or CE2 ≤ 0.2V	1.5	-	5.5	V			
Data Retention Current	I <sub>DR</sub>	V <sub>CC</sub> = 1.5V CE# ≥ V <sub>CC</sub> - 0.2V or CE2 ≤ 0.2V	SL	25°C	-	1	3	μA	
			SLI	40°C	-	1.5	3.5	μA	
		Others at 0.2V or V <sub>CC</sub> -0.2V		SL		-	1	5	μA
				SLI		-	1	10	μA
Chip Disable to Data Retention Time	t <sub>CDR</sub>	See Data Retention Waveforms (below)	0	-	-	ns			
Recovery Time	t <sub>R</sub>		t <sub>RC</sub> *	-	-	ns			

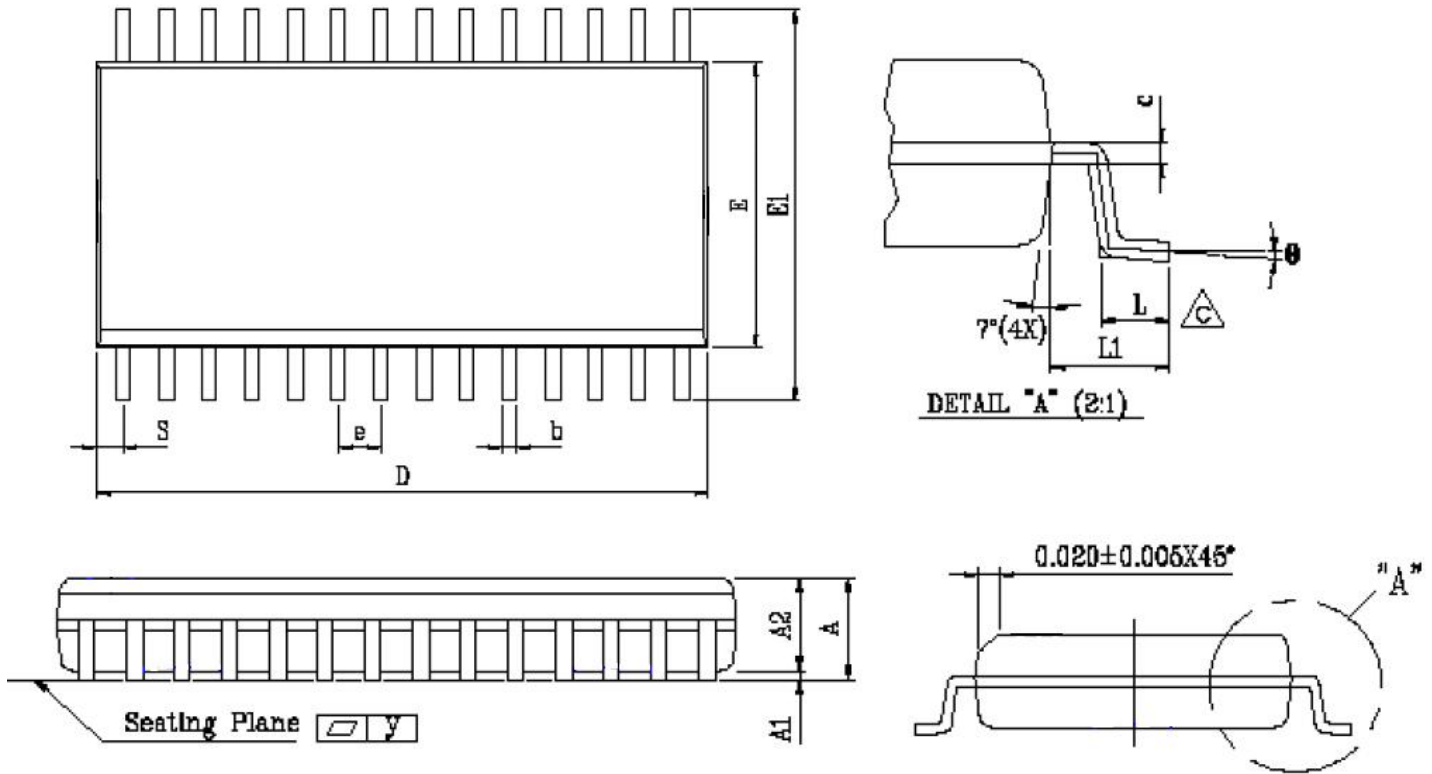
 t<sub>RC</sub>\* = Read Cycle Time

**DATA RETENTION WAVEFORM**
**Low V<sub>CC</sub> Data Retention Waveform (1) (CE# controlled)**

**Low V<sub>CC</sub> Data Retention Waveform (2) (CE2 controlled)**




**PACKAGE OUTLINE DIMENSION**

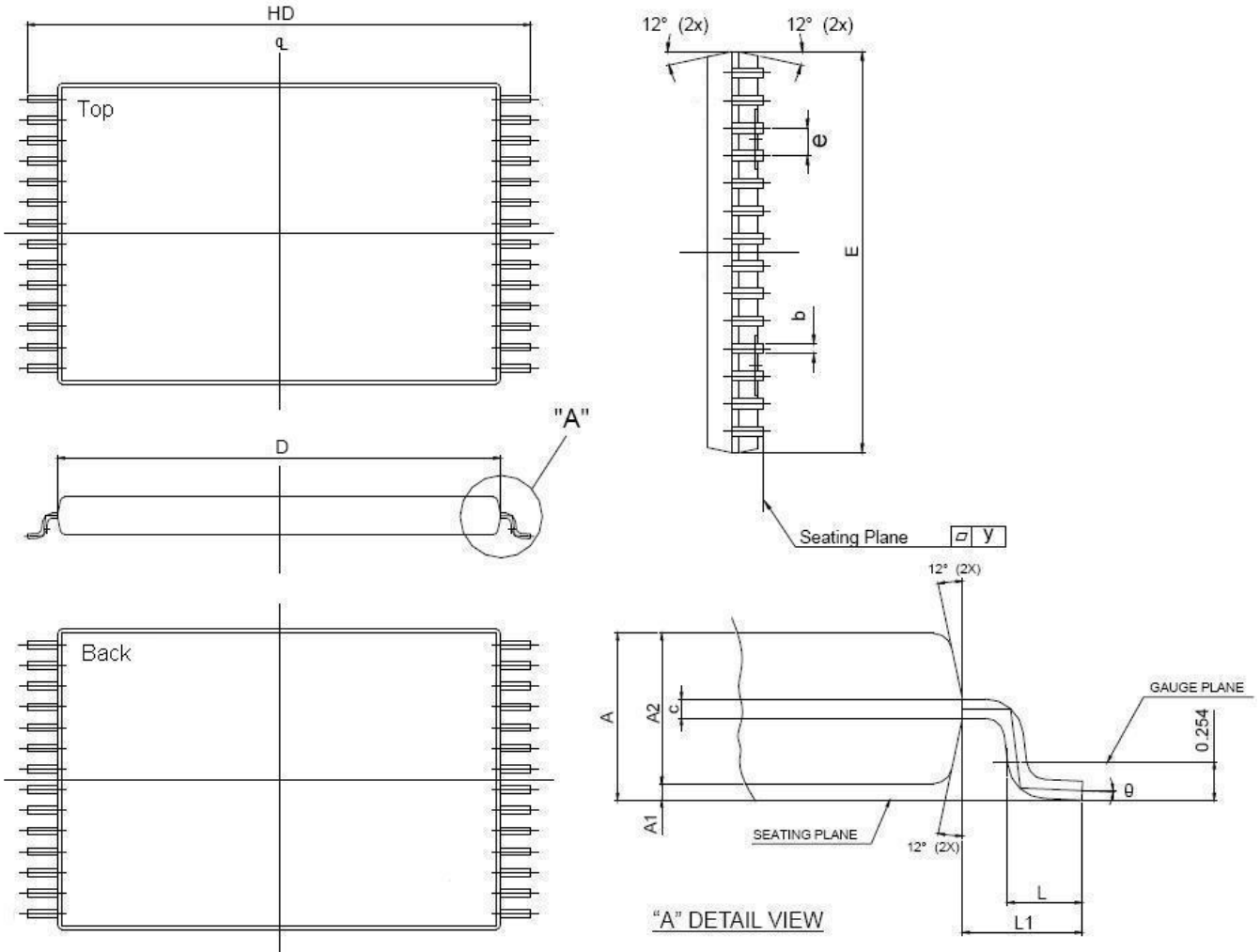
**28 pin 330 mil SOP Package Outline Dimension**



SYMBOL \ UNIT	INCH(BASE)	MM(REF)
A	0.120(MAX)	3.048(MAX)
A1	0.002(MIN)	0.05(MIN)
A2	0.098±0.005	2.489±0.127
b	0.016(TYP)	0.406(TYP)
c	0.010(TYP)	0.254(TYP)
D	0.728(MAX)	18.491(MAX)
E	0.340(MAX)	8.636(MAX)
E1	0.465±0.012	11.811±0.305
e	0.050(TYP)	1.255(TYP)
L	0.038(MAX)	0.965(MAX)
L1	0.067±0.008	1.552 ±0.203
S	0.047(MAX)	1.194(MAX)
y	0.004(MAX)	0.102(MAX)
Θ	0°~10°	0°~10°



**28 pin 8x13.4mm sTSP Package Outline Dimension**



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.00	1.10	1.20	0.040	0.043	0.047
A1	0.05	-	0.15	0.002	-	0.006
A2	0.91	1.00	1.05	0.036	0.039	0.041
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.07	0.15	0.23	0.003	0.006	0.009
HD	13.20	13.40	13.60	0.520	0.528	0.535
D	11.60	11.80	12.00	0.457	0.465	0.472
E	7.80	8.00	8.20	0.307	0.315	0.323
e	-	0.55	-	-	0.0216	-
L	0.30	0.50	0.55	0.012	0.020	0.028
L1	0.675	-	-	0.027	-	-
Y	0.00	-	0.076	0.000	-	0.003
θ	0°	3°	5°	0°	3°	5°



### ORDERING INFORMATION

Package Type	Access Time (Speed)(ns)	Power Type	Temperature Range(°C)	Packing Type	Lyontek Item No.
28-pin 330mil SOP	45	Special Ultra Low Power	-40°C~85°C	Tube	LY6264BSL-45SLI
				Tape Reel	LY6264BSL-45SLIT
28-pin 8mm x 13.4mm sTSOP	45	Special Ultra Low Power	-40°C~85°C	Tray	LY6264BRL-45SLI
				Tape Reel	LY6264BRL-45SLIT



**Lyontek Inc.**

**LY6264B**

Rev. 1.1

**8K X 8 BIT LOW POWER CMOS SRAM**

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