



REVISION HISTORY

<u>Revision</u>	<u>Description</u>	<u>Issue Date</u>
Rev. 1.0	Initial Issue	Sep.09.2020
Rev. 1.1	1.Revised DC ELECTRICAL CHARACTERISTICS Notes: 1. $V_{IH}(\max) = V_{CC} + 3.0V$ for pulse width less than <u>6ns.</u> → <u>10ns</u> 2. $V_{IL}(\min) = V_{SS} - 3.0V$ for pulse width less than <u>6ns.</u> → <u>10ns</u> in page 4 2.Revised 48-ball 6mm × 8mm TFBGA Package Outline Dimension in page 11 A:1.4mm→1.2mm	Mar.26.2021
Rev. 1.2	Added ordering information for 48-ball 6mm × 8mm TFBGA Package in page 12	Jul.01.2022
Rev. 1.3	1.Revised DC ELECTRICAL CHARACTERISTICS :Standby Power Supply Current: I_{SB1} : SL(MAX.)10→7, SLI(MAX.)12→10 in page 4 2.Revised DATA RETENTION CHARACTERISTICS : Data Retention Current: I_{DR} : SL(MAX.)10→7, SLI(MAX.)12→10 in page 9	Apr.21.2025

FEATURES

- Fast access time : 45/55ns
- Low power consumption:
Operating current : 12mA (TYP.)
Standby current : 1.8μA (TYP.)
- Single 2.7V ~ 3.6V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data byte control : LB# (DQ0 ~ DQ7)
UB# (DQ8 ~ DQ15)
- Data retention voltage : 1.5V (MIN.)
- **Green package available**
- Package : 44-pin 400mil TSOP II
48-ball 6mm x 8mm TFBGA

GENERAL DESCRIPTION

The LY62L25716B is a 4,194,304-bit low power CMOS static random access memory organized as 262,144 words by 16 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

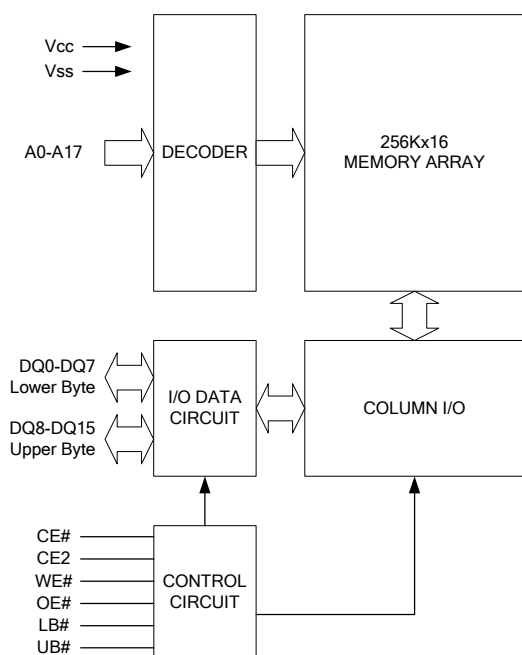
The LY62L25716B is well designed for low power application, and particularly well suited for battery back-up nonvolatile memory application.

The LY62L25716B operates from a single power supply of 2.7V ~ 3.6V and all inputs and outputs are fully TTL compatible

PRODUCT FAMILY

Product Family	Operating Temperature	V _{CC} Range	Speed	Power Dissipation	
				Standby(I _{SB1} , TYP.)	Operating(I _{CC} , TYP.)
LY62L25716B	0 ~ 70°C	2.7 ~ 3.6V	45/55ns	1.8μA	12mA
LY62L25716B(I)	-40 ~ 85°C	2.7 ~ 3.6V	45/55ns	1.8μA	12mA

FUNCTIONAL BLOCK DIAGRAM

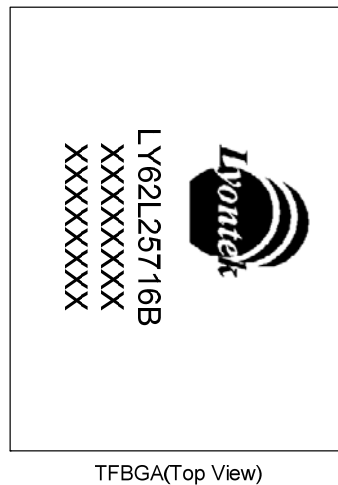
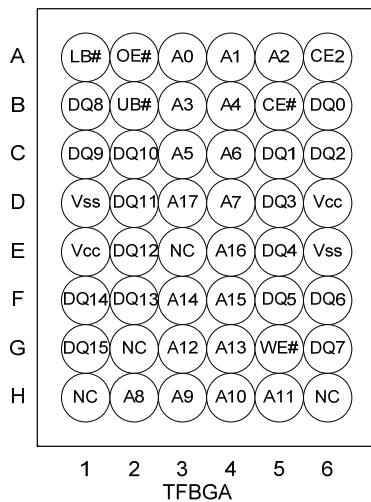
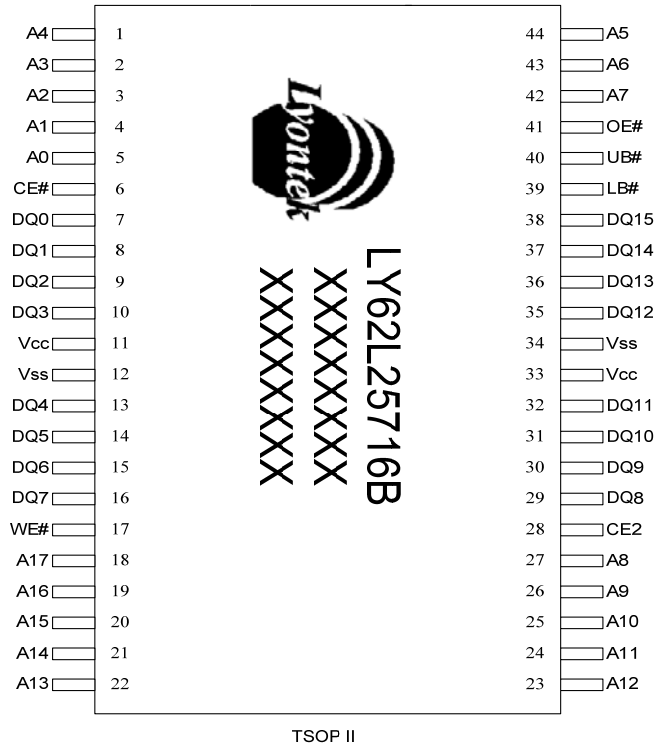


PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A17	Address Inputs
DQ0 - DQ15	Data Inputs/Outputs
CE#, CE2	Chip Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
LB#	Lower Byte Control
UB#	Upper Byte Control
V _{CC}	Power Supply
V _{SS}	Ground



PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on V_{CC} relative to V_{SS}	V_{T1}	-0.5 to 4.6	V
Voltage on any other pin relative to V_{SS}	V_{T2}	-0.5 to $V_{CC}+0.5$	V
Operating Temperature	T_A	0 to 70(C grade)	°C
		-40 to 85(I grade)	
Storage Temperature	T_{STG}	-65 to 150	°C
Power Dissipation	P_D	1	W
DC Output Current	I_{OUT}	50	mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE#	CE2	OE#	WE#	LB#	UB#	I/O OPERATION		SUPPLY CURRENT
							DQ0-DQ7	DQ8-DQ15	
Standby	H	X	X	X	X	X	High – Z	High – Z	I_{SB1}
	X	L	X	X	X	X	High – Z	High – Z	
	X	X	X	X	H	H	High – Z	High – Z	
Output Disable	L	H	H	H	L	X	High – Z	High – Z	I_{CC}, I_{CC1}
	L	H	H	H	X	L	High – Z	High – Z	
Read	L	H	L	H	L	H	D_{OUT}	High – Z	I_{CC}, I_{CC1}
	L	H	L	H	H	L	High – Z	D_{OUT}	
	L	H	L	H	L	L	D_{OUT}	D_{OUT}	
Write	L	H	X	L	L	H	D_{IN}	High – Z	I_{CC}, I_{CC1}
	L	H	X	L	H	L	High – Z	D_{IN}	
	L	H	X	L	L	L	D_{IN}	D_{IN}	

Note: H = V_{IH} , L = V_{IL} , X = Don't care.

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP. ^{*4}	MAX.	UNIT
Supply Voltage	V_{CC}		2.7	3.0	3.6	V
Input High Voltage	V_{IH}^{*1}		2.2	-	$V_{CC}+0.3$	V
Input Low Voltage	V_{IL}^{*2}		- 0.2	-	0.6	V
Input Leakage Current	I_{LI}	$V_{CC} \geq V_{IN} \geq V_{SS}$	- 1	-	1	μA
Output Leakage Current	I_{LO}	$V_{CC} \geq V_{OUT} \geq V_{SS}$, Output Disabled	- 1	-	1	μA
Output High Voltage	V_{OH}	$I_{OH} = -1mA$	2.2	2.7	-	V
Output Low Voltage	V_{OL}	$I_{OL} = 2mA$	-	-	0.4	V
Average Operating Power supply Current	I_{CC}	Cycle time = Min. $CE\# \leq 0.2V$ and $CE2 \geq V_{CC}-0.2V$ $I_{I/O} = 0mA$ Other pins at 0.2V or $V_{CC}-0.2V$	-	12	20	mA
	I_{CC1}	Cycle time = $1\mu s$ $CE\# \leq 0.2V$ and $CE2 \geq V_{CC}-0.2V$ $I_{I/O} = 0mA$ Other pins at 0.2V or $V_{CC} - 0.2V$	-	2	4	mA
Standby Power Supply Current	I_{SB1}	$CE\# \geq V_{CC} - 0.2V$ or $CE2 \leq 0.2V$ Others at 0.2V or $V_{CC} - 0.2V$	SL^{*5} 25°C	-	1.8	4 μA
			SLI^{*5} 40°C	-	2	4.5 μA
			SL	-	1.8	7 μA
			SLI	-	1.8	10 μA

Notes:

- $V_{IH}(\max) = V_{CC} + 3.0V$ for pulse width less than 10ns.
- $V_{IL}(\min) = V_{SS} - 3.0V$ for pulse width less than 10ns.
- Over/Undershoot specifications are characterized on engineering evaluation stage, not for mass production test.
- Typical values are included for reference only and are not guaranteed or tested.
Typical values are measured at $V_{CC} = V_{CC}(TYP.)$ and $T_A = 25^\circ C$
- This parameter is measured at $V_{CC} = 3.0V$

CAPACITANCE ($T_A = 25^\circ C$, $f = 1.0MHz$)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C_{IN}	-	6	pF
Input/Output Capacitance	$C_{I/O}$	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0.2V to $V_{CC} - 0.2V$
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	$C_L = 30pF + 1TTL$, $I_{OH}/I_{OL} = -1mA/2mA$



AC ELECTRICAL CHARACTERISTICS

(1) READ CYCLE

PARAMETER	SYM.	LY62L25716B-45		LY62L25716B-55		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t _{RC}	45	-	55	-	ns
Address Access Time	t _{AA}	-	45	-	55	ns
Chip Enable Access Time	t _{ACE}	-	45	-	55	ns
Output Enable Access Time	t _{OE}	-	25	-	30	ns
Chip Enable to Output in Low-Z	t _{CLZ} *	10	-	10	-	ns
Output Enable to Output in Low-Z	t _{OLZ} *	5	-	5	-	ns
Chip Disable to Output in High-Z	t _{CHZ} *	-	15	-	20	ns
Output Disable to Output in High-Z	t _{OHZ} *	-	15	-	20	ns
Output Hold from Address Change	t _{OH}	10	-	10	-	ns
LB#, UB# Access Time	t _{BA}	-	45	-	55	ns
LB#, UB# to High-Z Output	t _{BHZ} *	-	20	-	25	ns
LB#, UB# to Low-Z Output	t _{BLZ} *	10	-	10	-	ns

(2) WRITE CYCLE

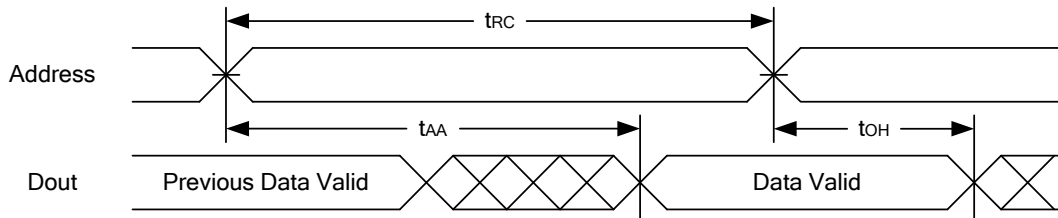
PARAMETER	SYM.	LY62L25716B-45		LY62L25716B-55		UNIT
		MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t _{WC}	45	-	55	-	ns
Address Valid to End of Write	t _{AW}	40	-	50	-	ns
Chip Enable to End of Write	t _{CW}	40	-	50	-	ns
Address Set-up Time	t _{AS}	0	-	0	-	ns
Write Pulse Width	t _{WP}	35	-	45	-	ns
Write Recovery Time	t _{WR}	0	-	0	-	ns
Data to Write Time Overlap	t _{DW}	20	-	25	-	ns
Data Hold from End of Write Time	t _{DH}	0	-	0	-	ns
Output Active from End of Write	t _{OW} *	5	-	5	-	ns
Write to Output in High-Z	t _{WHZ} *	-	15	-	20	ns
LB#, UB# Valid to End of Write	t _{BW}	35	-	45	-	ns

*These parameters are guaranteed by device characterization, but not production tested.

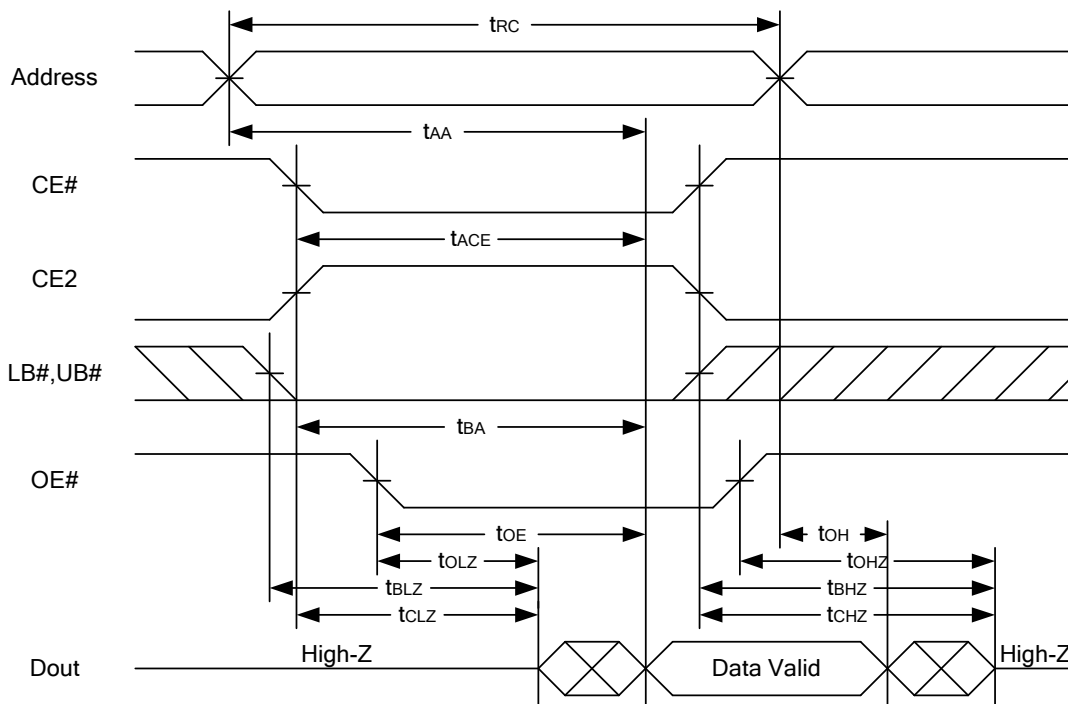


TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)



READ CYCLE 2 (CE# and CE2 and OE# Controlled) (1,3,4,5)

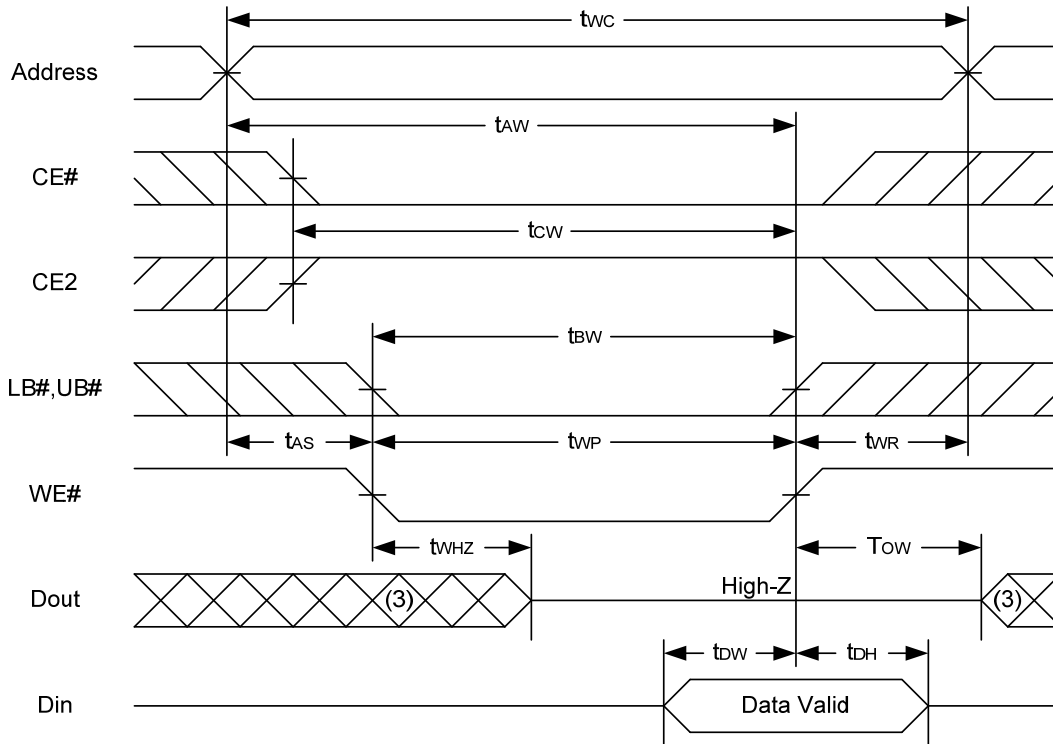


Notes :

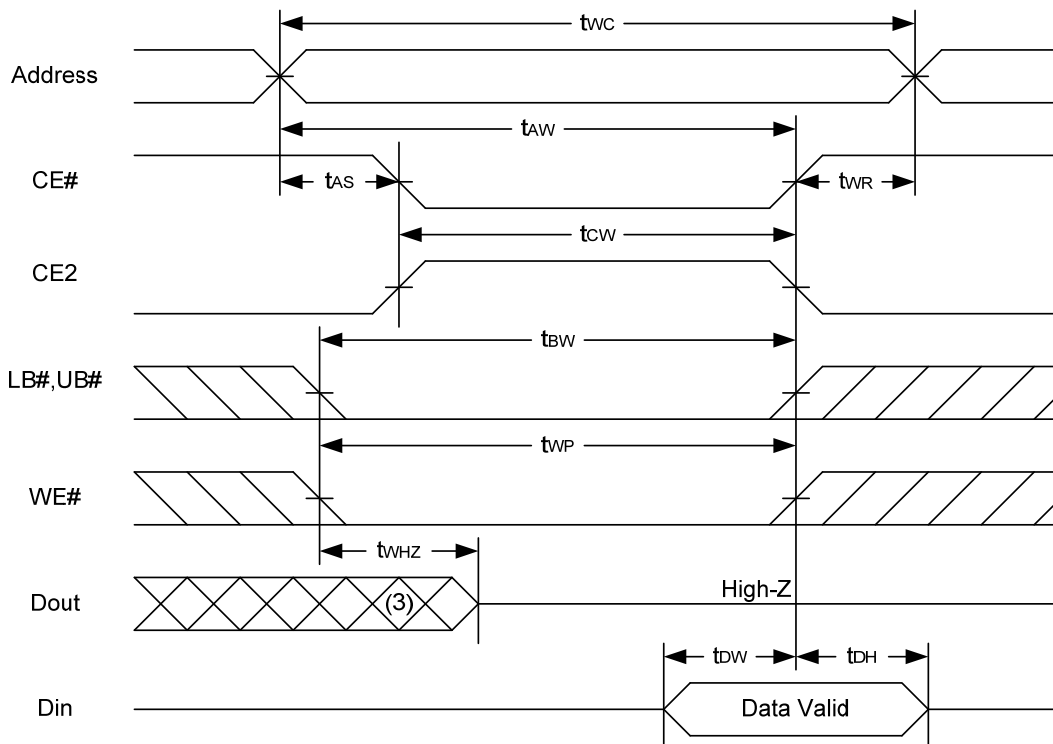
1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low, CE2 = high, LB# or UB# = low.
3. Address must be valid prior to or coincident with CE# = low, CE2 = high, LB# or UB# = low transition; otherwise t_{AA} is the limiting parameter.
4. t_{CLZ} , t_{BLZ} , t_{OLZ} , t_{CHZ} , t_{BHZ} and t_{OHZ} are specified with $C_L = 5pF$. Transition is measured $\pm 500mV$ from steady state.
5. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{BHZ} is less than t_{BLZ} , t_{OHZ} is less than t_{OLZ} .

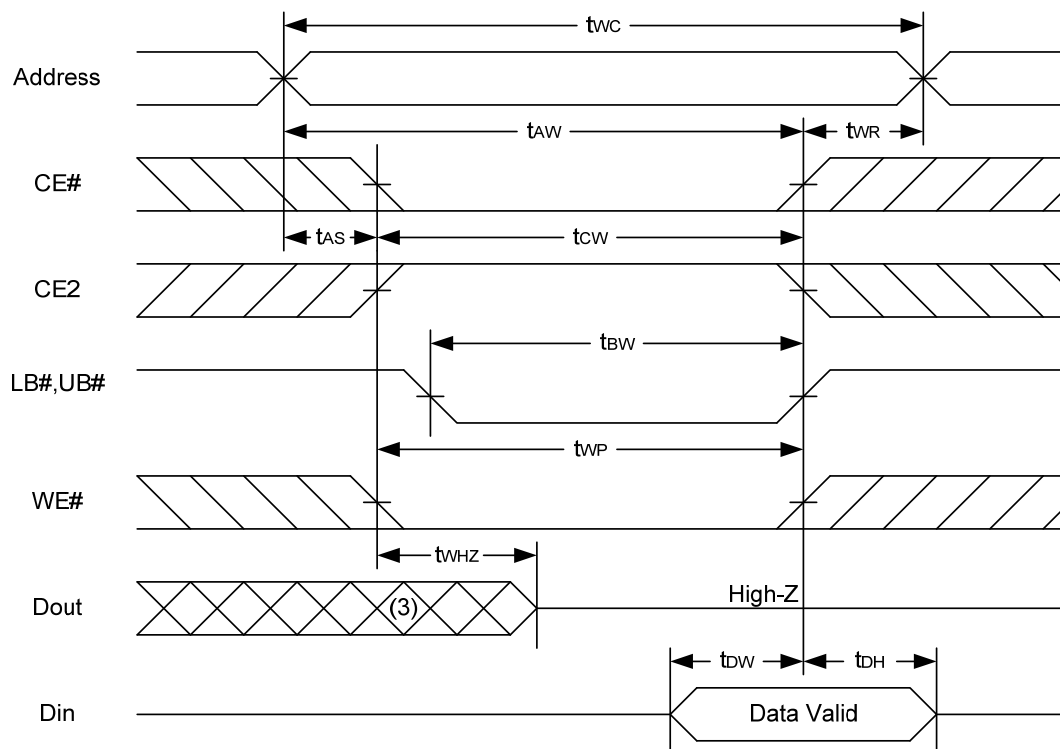


WRITE CYCLE 1 (WE# Controlled) (1,2,4,5)



WRITE CYCLE 2 (CE# and CE2 Controlled) (1,4,5)



WRITE CYCLE 3 (LB#,UB# Controlled) (1,4,5)

Notes :

1. A write occurs during the overlap of a low CE#, high CE2, low WE#, LB# or UB# = low.
2. During a WE# controlled write cycle with OE# low, tWP must be greater than tWHZ + tDW to allow the drivers to turn off and data to be placed on the bus.
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the CE#, LB#, UB# low transition and CE2 high transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
5. tOW and tWHZ are specified with CL = 5pF. Transition is measured $\pm 500\text{mV}$ from steady state.

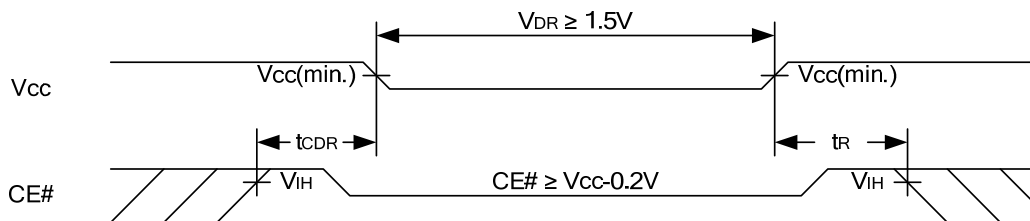
DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
V _{CC} for Data Retention	V _{DR}	CE# $\geq$ V _{CC} - 0.2V	1.5	-	3.6	V
Data Retention Current	I _{DR}	V _{CC} = 1.5V CE# $\geq$ V _{CC} - 0.2V or CE2 $\leq$ 0.2V Other pins at 0.2V or V _{CC} -0.2V	SL 25°C	-	1.8	4 μ A
			SLI 40°C	-	2	4.5 μ A
			SL	-	1.8	7 μ A
			SLI	-	1.8	10 μ A
Chip Disable to Data Retention Time	t _{CDR}	See Data Retention Waveforms (below)	0	-	-	ns
Recovery Time	t _R		t _{RC} *	-	-	ns

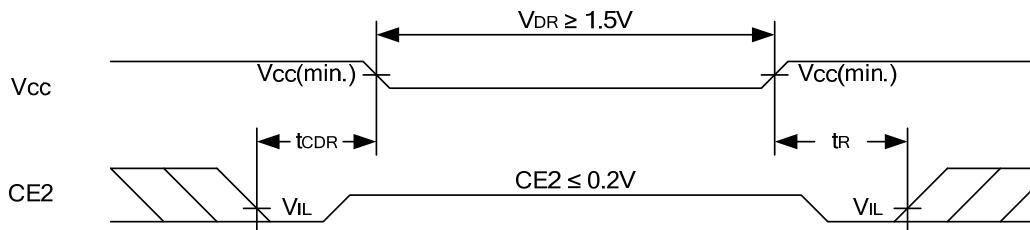
t_{RC}* = Read Cycle Time

DATA RETENTION WAVEFORM

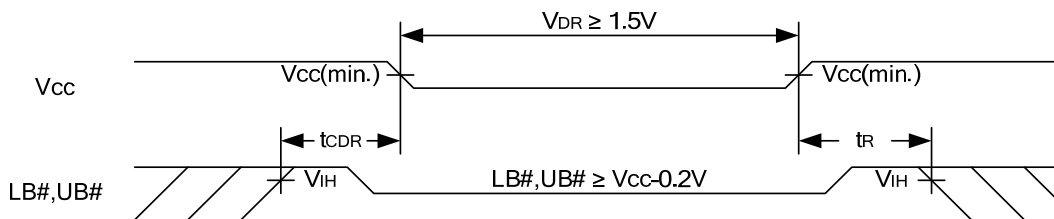
Low V_{CC} Data Retention Waveform (1) (CE# controlled)



Low V_{CC} Data Retention Waveform (2) (CE2 controlled)

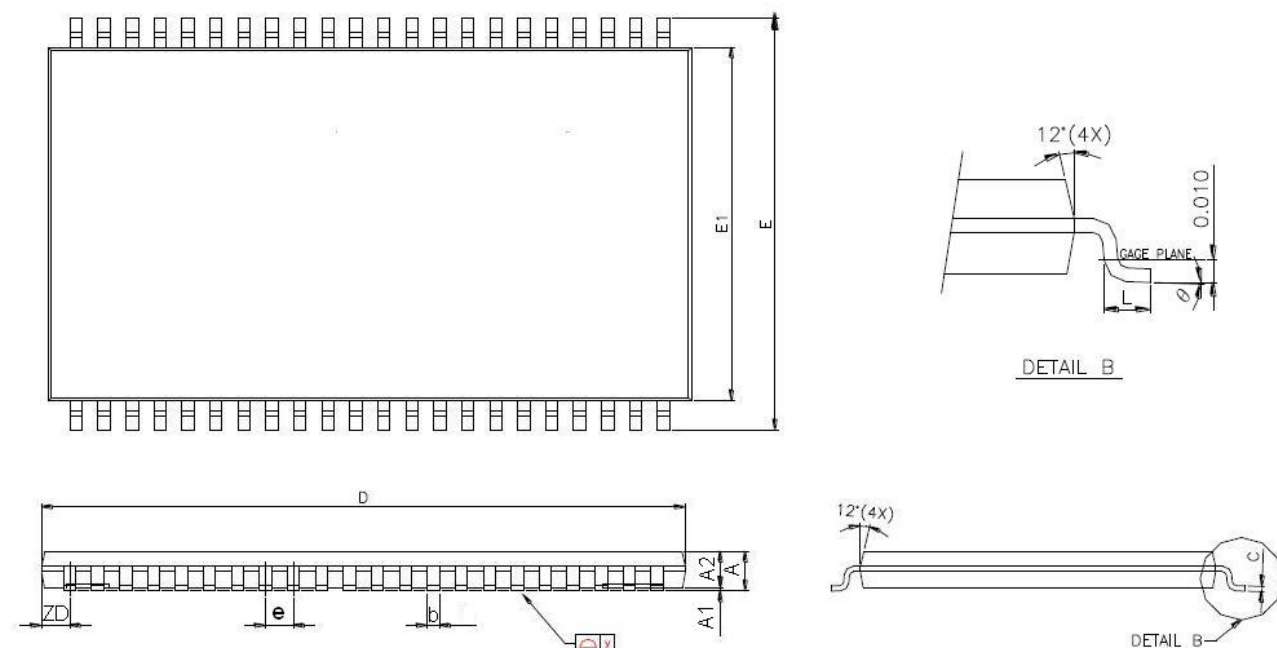


Low V_{CC} Data Retention Waveform (3) (LB#, UB# controlled)



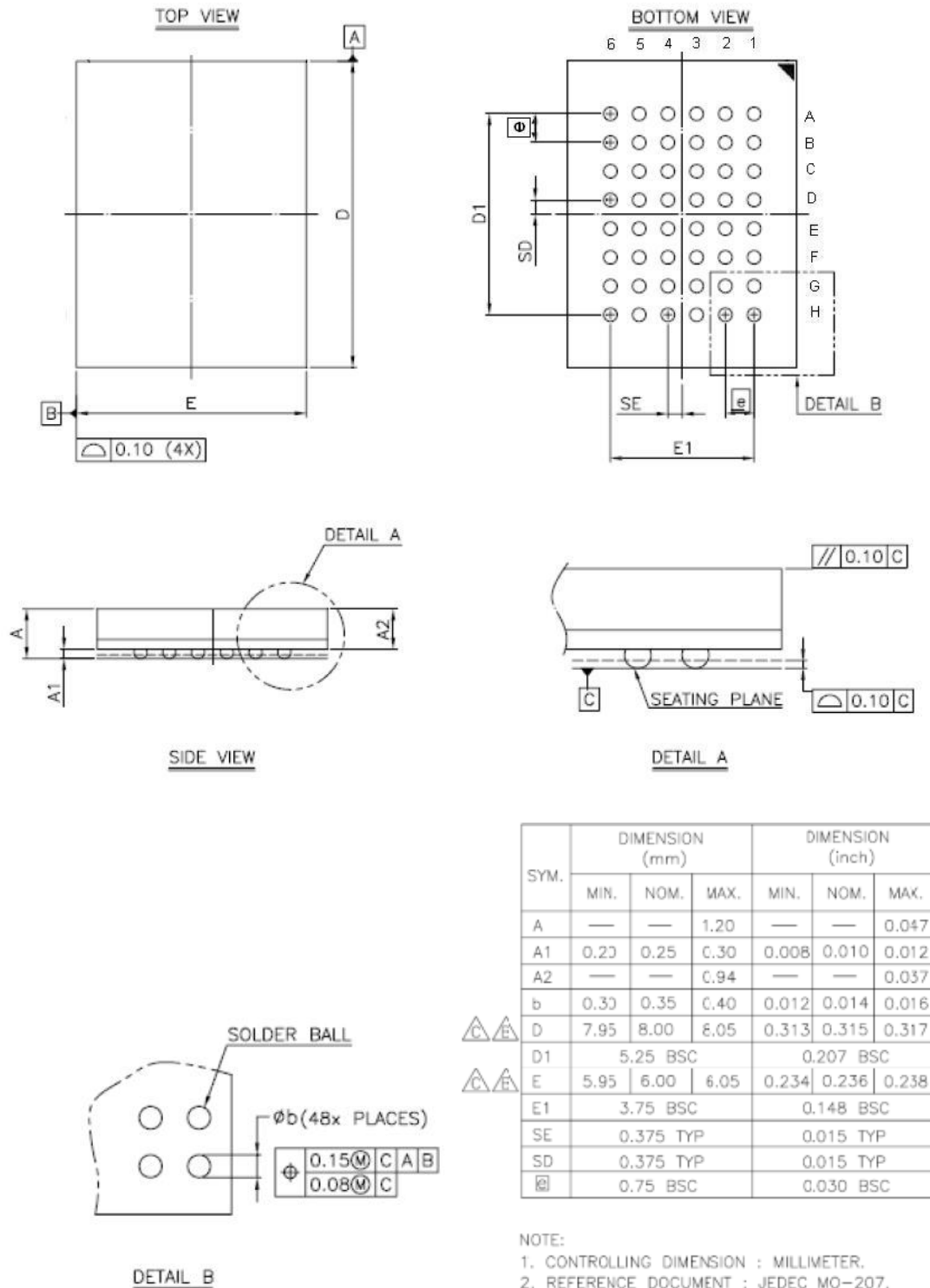
PACKAGE OUTLINE DIMENSION

44-pin 400mil TSOP II Package Outline Dimension



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN MILS		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	-	-	1.20	-	-	47.2
A1	0.05	0.10	0.15	2.0	3.9	5.9
A2	0.95	1.00	1.05	37.4	39.4	41.3
b	0.30	-	0.45	11.8	-	17.7
c	0.12	-	0.21	4.7	-	8.3
D	18.212	18.415	18.618	717	725	733
E	11.506	11.760	12.014	453	463	473
E1	9.957	10.160	10.363	392	400	408
e	-	0.800	-	-	31.5	-
L	0.40	0.50	0.60	15.7	19.7	23.6
ZD	-	0.805	-	-	31.7	-
y	-	-	0.076	-	-	3
Θ	0°	3°	6°	0°	3°	6°

48-ball 6mm × 8mm TFBGA Package Outline Dimension



**ORDERING INFORMATION**

Package Type	Access Time (Speed)(ns)	Power Type	Temperature Range(°C)	Packing Type	Lyontek Item No.
44Pin(400mil) TSOP II	45	Special Ultra Low Power	0°C~70°C	Tray	LY62L25716BML-45SL
				Tape Reel	LY62L25716BML-45SLT
			-40°C~85°C	Tray	LY62L25716BML-45SLI
				Tape Reel	LY62L25716BML-45SLIT
	55	Special Ultra Low Power	0°C~70°C	Tray	LY62L25716BML-55SL
				Tape Reel	LY62L25716BML-55SLT
			-40°C~85°C	Tray	LY62L25716BML-55SLI
				Tape Reel	LY62L25716BML-55SLIT
48Ball(6mm*8mm) TFBGA	45	Special Ultra Low Power	0°C~70°C	Tray	LY62L25716BGL-45SL
				Tape Reel	LY62L25716BGL-45SLT
			-40°C~85°C	Tray	LY62L25716BGL-45SLI
				Tape Reel	LY62L25716BGL-45SLIT
	55	Special Ultra Low Power	0°C~70°C	Tray	LY62L25716BGL-55SL
				Tape Reel	LY62L25716BGL-55SLT
			-40°C~85°C	Tray	LY62L25716BGL-55SLI
				Tape Reel	LY62L25716BGL-55SLIT



Lyontek Inc.

LY62L25716B

Rev. 1.3

256K X 16 BIT LOW POWER CMOS SRAM

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