REVISION HISTORY

Revision	Description	Issue Date
Rev. 1.0	Initial Issue	Jun.09.2026

LY62L819216A

Rev. 1.0

8M X 16 BITS LOW POWER CMOS SRAM

FEATURE

- Fast access time : 55ns
- Low power consumption:
  Operating current : 20mA (TYP.)
  Standby current : 18μA (TYP.)
- Single 2.7V ~ 3.6V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data byte control :
  DQ0 ~ DQ7 controlled by LB#,
  DQ8 ~ DQ15 controlled by UB#.
- Data retention voltage : 1.5V (MIN.)
- **Green package available**
- Package : 48-ball 9mm x 11mm TFBGA

GENERAL DESCRIPTION

The LY62L819216A is a 134,217,728-bit low power CMOS static random access memory organized as 8,388,608 words by 16 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

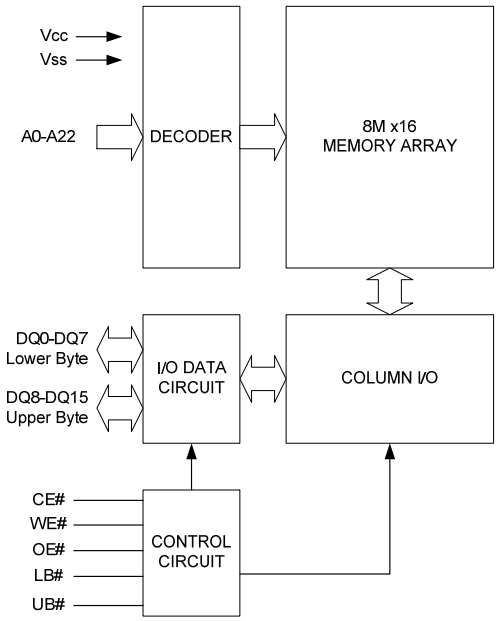
The LY62L819216A is well designed for low power application, and particularly well suited for battery back-up nonvolatile memory application.

The LY62L819216A operates from a single power supply of 2.7V ~ 3.6V and all inputs and outputs are fully TTL compatible

PRODUCT FAMILY

Product Family	Operating Temperature	V_{CC} Range	Speed	Power Dissipation	
				Standby(I_{SB1},TYP.)	Operating(I_{CC},TYP.)
LY62L819216A	0 ~ 70℃	2.7 ~ 3.6V	55ns	18μA	20mA
LY62L819216A(I)	-40 ~ 85℃	2.7 ~ 3.6V	55ns	18μA	20mA

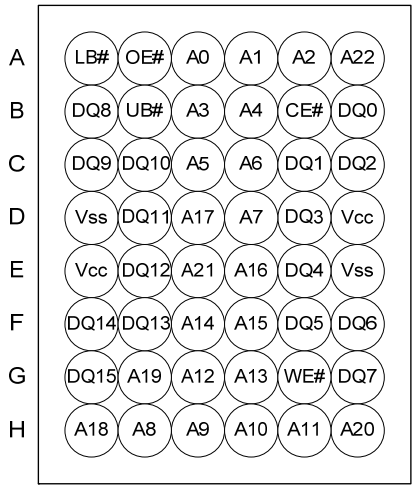
FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A22	Address Inputs
DQ0 - DQ15	Data Inputs/Outputs
CE#	Chip Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
LB#	Lower Byte Control
UB#	Upper Byte Control
V_{CC}	Power Supply
V_{SS}	Ground

PIN CONFIGURATION



TFBGA(See through with Top View)

TFBGA(Top View)

ABSOLUTE MAXIMUN RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on V_{CC} relative to V_{SS}	V_{T1}	-0.5 to 4.6	V
Voltage on any other pin relative to V_{SS}	V_{T2}	-0.5 to V_{CC}+0.5	V
Operating Temperature	T_A	0 to 70(C grade)	℃
		-40 to 85(I grade)	
Storage Temperature	T_{STG}	-65 to 150	℃
Power Dissipation	P_D	1	W
DC Output Current	I_{OUT}	50	mA

*Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE#	A22 *2	OE#	WE#	LB#	UB#	I/O OPERATION		SUPPLY CURRENT
							DQ0 - DQ7	DQ8 - DQ15	
Standby	H	L/H	X	X	X	X	High-Z	High-Z	I_{SB1}
	X	L/H	X	X	H	H	High-Z	High-Z	
Output Disable	L	L/H	H	H	L	X	High-Z	High-Z	I_{CC},I_{CC1}
	L	L/H	H	H	X	L	High-Z	High-Z	
Read	L	L/H	L	H	L	H	D_{OUT}	High-Z	I_{CC},I_{CC1}
	L	L/H	L	H	H	L	High-Z	D_{OUT}	
	L	L/H	L	H	L	L	D_{OUT}	D_{OUT}	
Write	L	L/H	X	L	L	H	D_{IN}	High-Z	I_{CC},I_{CC1}
	L	L/H	X	L	H	L	High-Z	D_{IN}	
	L	L/H	X	L	L	L	D_{IN}	D_{IN}	

Note: 1. H= V_{IH}, L= V_{IL}, X= Don't care.
2. The A22 pin must be Low or High at any mode, and can’t be Don’t care nor left floating.

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP. *4	MAX.	UNIT
Supply Voltage	V_{CC}			2.7	3.0	3.6	V
Input High Voltage	V_{IH} *1			2.2	-	V_{CC}+0.3	V
Input Low Voltage	V_{IL} *2			- 0.2	-	0.6	V
Input Leakage Current	I_{LI}	$V_{CC} \geqq V_{IN} \geqq V_{SS}$		- 1	-	1	µA
Output Leakage Current	I_{LO}	$V_{CC} \geqq V_{OUT} \geqq V_{SS}$ Output Disabled		- 1	-	1	µA
Output High Voltage	V_{OH}	I_{OH} = -1mA		2.2	2.7	-	V
Output Low Voltage	V_{OL}	I_{OL} = 2mA		-	-	0.4	V
Average Operating Power supply Current	I_{CC}	Cycle time = MIN.CE# ≦ 0.2V $I_{I/O}$ = 0mA Other pins at 0.2V or V_{CC}-0.2V		-	20	30	mA
	I_{CC1}	Cycle time = 1µs CE# ≦ 0.2V $I_{I/O}$ = 0mA Other pins at 0.2V or V_{CC}-0.2V		-	2	4	mA
Standby Power Supply Current	I_{SB1}	CE#≧ V_{CC}-0.2V Others at 0.2V or V_{CC}-0.2V	-SL *5 25℃	-	18	50	µA
			-SLI *5 40℃	-	22	60	µA
			-SL (70℃)	-	-	200	µA
			-SLI (85℃)	-	-	320	µA

Notes:
1. V_{IH}(max) = V_{CC} + 2.0V for pulse width less than 6ns.
2. V_{IL}(min) = V_{SS} - 2.0V for pulse width less than 6ns.
3. Over/Undershoot specifications are characterized on engineering evaluation stage, not for mass production test.
4. Typical values, measured at V_{CC} = $V_{CC(TYP.)}$ and T_A = 25℃, are included for reference only and are not guaranteed or tested.
5. This parameter is measured at V_{CC}=3.0V.

CAPACITANCE (T_A = 25℃, f = 1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Input Capacitance	C_{IN}	-	20	pF
Input/Output Capacitance	$C_{I/O}$	-	20	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0.2V to V_{CC} - 0.2V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	C_L = 30pF + 1TTL, I_{OH}/I_{OL} = -1mA/2mA

AC ELECTRICAL CHARACTERISTICS

(1) READ CYCLE

PARAMETER	SYM.	LY62L819216A-55		UNIT
		MIN.	MAX.	
Read Cycle Time	t_{RC}	55	-	ns
Address Access Time	t_{AA}	-	55	ns
Chip Enable Access Time	t_{ACE}	-	55	ns
Output Enable Access Time	t_{OE}	-	30	ns
Chip Enable to Output in Low-Z	t_{CLZ}*	10	-	ns
Output Enable to Output in Low-Z	t_{OLZ}*	5	-	ns
Chip Disable to Output in High-Z	t_{CHZ}*	-	20	ns
Output Disable to Output in High-Z	t_{OHZ}*	-	20	ns
Output Hold from Address Change	t_{OH}	10	-	ns
LB#, UB# Access Time	t_{BA}	-	55	ns
LB#, UB# to High-Z Output	t_{BHZ}*	-	20	ns
LB#, UB# to Low-Z Output	t_{BLZ}*	10	-	ns

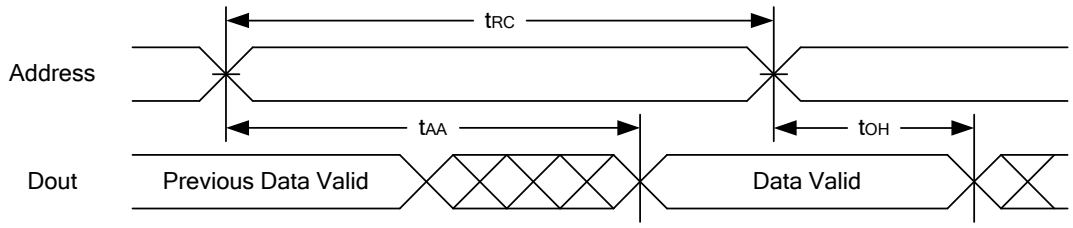
(2) WRITE CYCLE

PARAMETER	SYM.	LY62L819216A-55		UNIT
		MIN.	MAX.	
Write Cycle Time	t_{WC}	55	-	ns
Address Valid to End of Write	t_{AW}	50	-	ns
Chip Enable to End of Write	t_{CW}	50	-	ns
Address Set-up Time	t_{AS}	0	-	ns
Write Pulse Width	t_{WP}	45	-	ns
Write Recovery Time	t_{WR}	0	-	ns
Data to Write Time Overlap	t_{DW}	25	-	ns
Data Hold from End of Write Time	t_{DH}	0	-	ns
Output Active from End of Write	t_{OW}*	5	-	ns
Write to Output in High-Z	t_{WHZ}*	-	20	ns
LB#, UB# Valid to End of Write	t_{BW}	50	-	ns

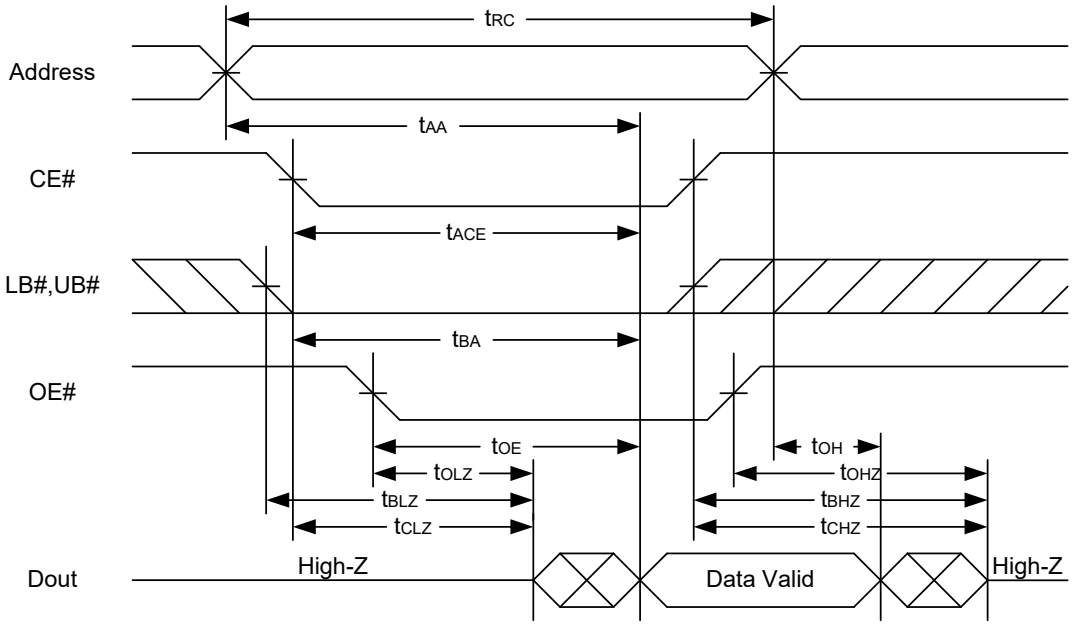
*These parameters are guaranteed by device characterization, but not production tested.

TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)

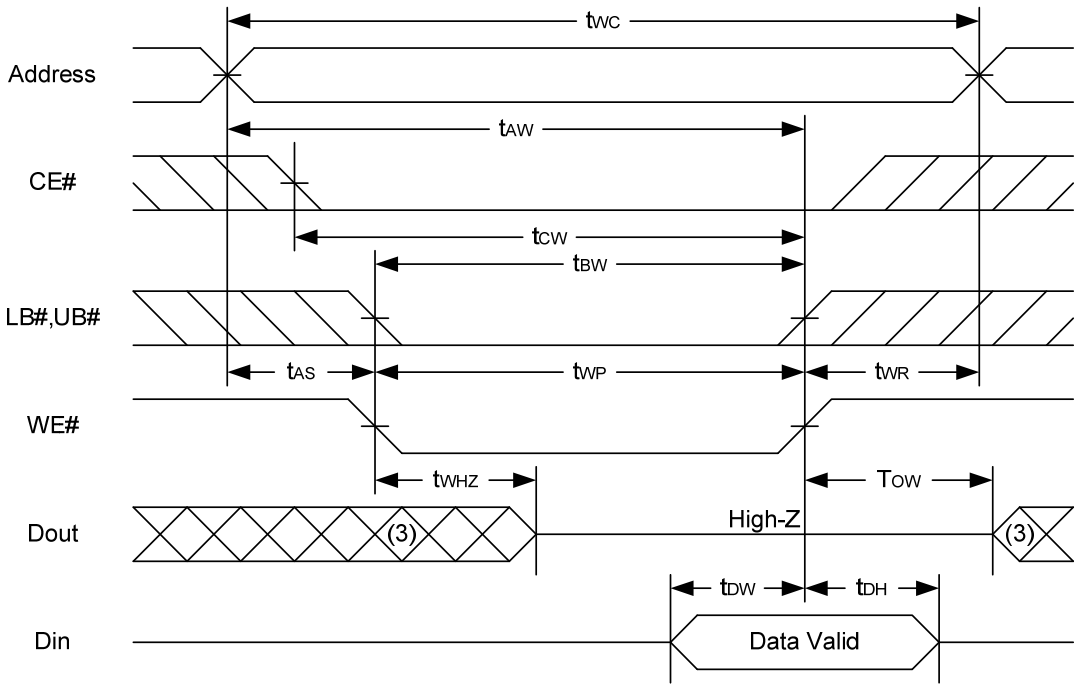


READ CYCLE 2 (CE# and OE# Controlled) (1,3,4,5)

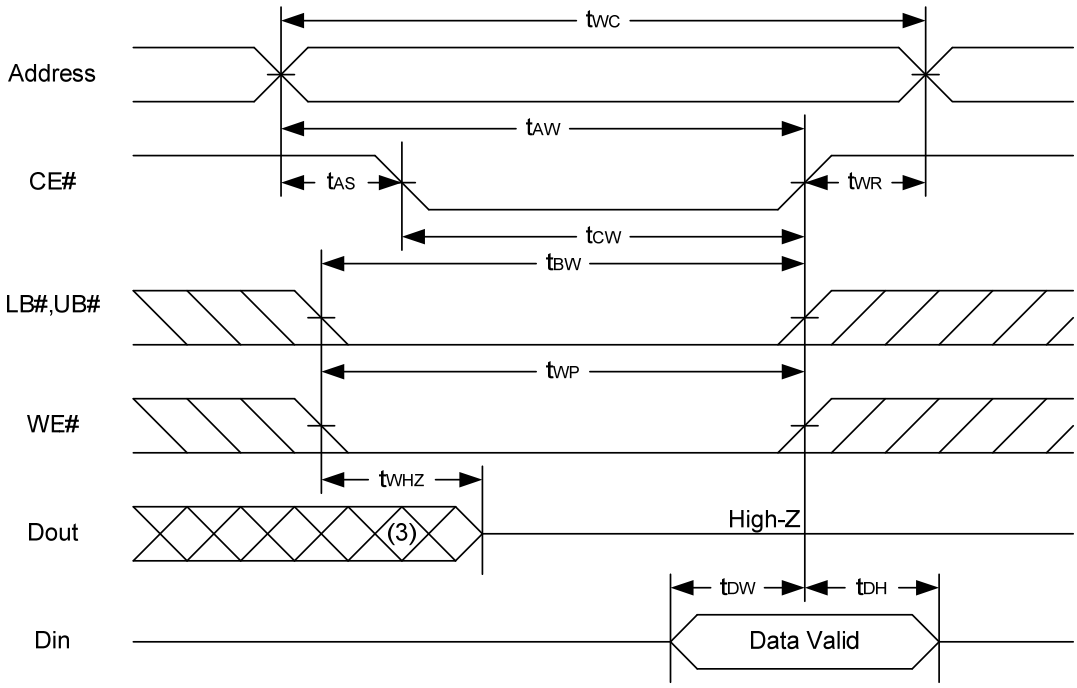


Notes :
1.WE# is high for read cycle.
2.Device is continuously selected OE# = low, CE# = low, LB# or UB# = low.
3.Address must be valid prior to or coincident with CE# = low, LB# or UB# = low transition; otherwise t_{AA} is the limiting parameter.
4.t_{CLZ}, t_{BLZ}, t_{OLZ}, t_{CHZ}, t_{BHZ} and t_{OHZ} are specified with C_L = 5pF. Transition is measured ±500mV from steady state.
5.At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{BHZ} is less than t_{BLZ}, t_{OHZ} is less than t_{OLZ}.

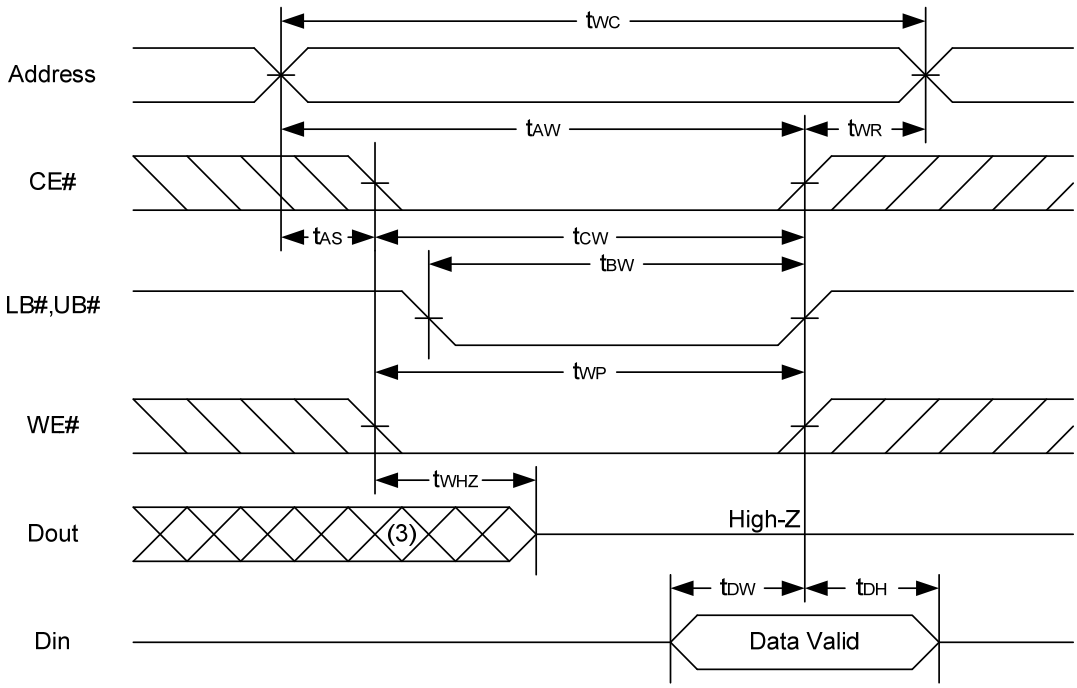
WRITE CYCLE 1 (WE# Controlled) (1,2,4,5)



WRITE CYCLE 2 (CE# Controlled) (1,4,5)



WRITE CYCLE 3 (LB#,UB# Controlled) (1,4,5)



Notes :
1. A write occurs during the overlap of a low CE#, low WE#, LB# or UB# = low.
2. During a WE# controlled write cycle with OE# low, t_{WP} must be greater than $t_{WHZ} + t_{DW}$ to allow the drivers to turn off and data to be placed on the bus.
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the CE#, LB#, UB# low transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
5. t_{OW} and t_{WHZ} are specified with C_L = 5pF. Transition is measured ±500mV from steady state.

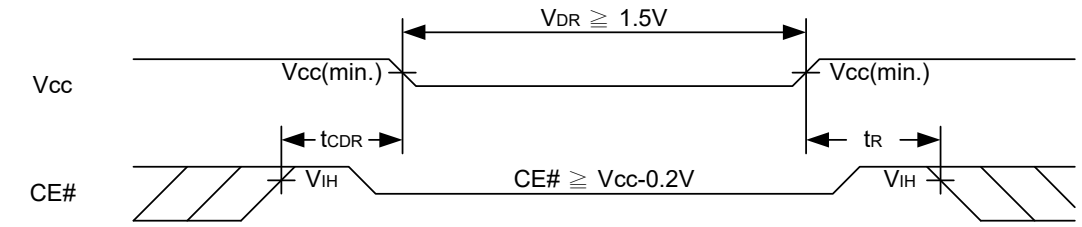
DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
V_{CC} for Data Retention	V_{DR}	CE#≧V_{CC} - 0.2V			1.5	-	3.6	V
Data Retention Current	I_{DR}	V_{CC} = 1.5V CE# ≧V_{CC}-0.2V Other pins at 0.2V or V_{CC}-0.2V	-SL	25℃	-	18	50	µA
			-SLI	40℃	-	22	60	µA
			-SL		-	-	200	µA
			-SLI		-	-	320	µA
Chip Disable to Data Retention Time	t_{CDR}	See Data Retention Waveforms (below)			0	-	-	ns
Recovery Time	t_R				t_{RC*}	-	-	ns

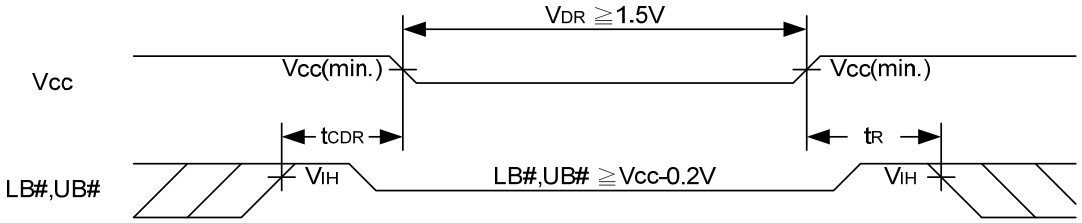
t_{RC*} = Read Cycle Time

DATA RETENTION WAVEFORM

Low V_{CC} Data Retention Waveform (1) (CE# controlled)

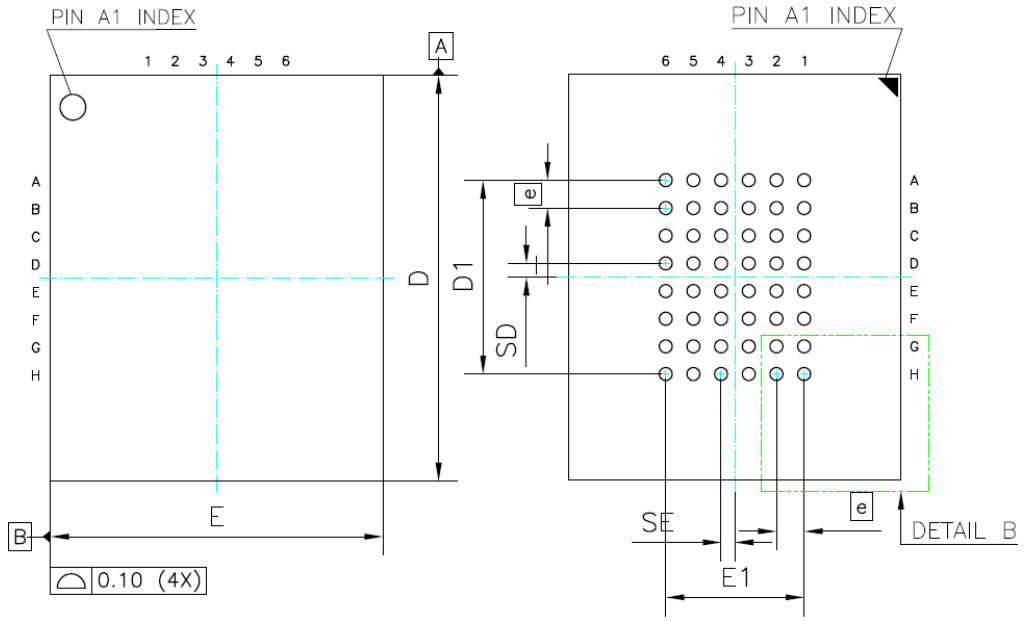


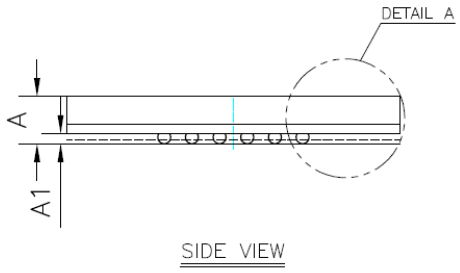
Low V_{CC} Data Retention Waveform (2) (LB#, UB# controlled)

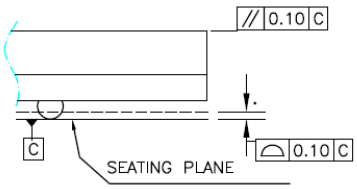


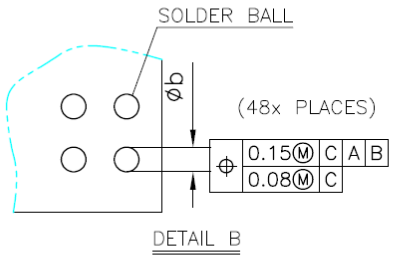
PACKAGE OUTLINE DIMENSION

48-ball 9mm × 11mm TFBGA Package Outline Dimension









SYM.	DIMENSION(mm)		
	MIN.	NOM.	MAX.
A	–	–	1.40
A1	0.22	0.27	0.32
A2	–	–	1.06
b	0.30	0.35	0.40
D	10.90	11.00	11.10
D1	5.25 BSC		
E	8.90	9.00	9.10
E1	3.75 BSC		
SD	0.375TYP		
SE	0.375TYP		
e	0.75 BSC		
Ball size pre–reflow			0.35

ORDERING INFORMATION

Package Type	Access Time (Speed)(ns)	Power Type	Temperature Range(℃)	Packing Type	Lyontek Item No.
48-ball (9mm x 11mm) TFBGA	55	Special Ultra Low Power	0℃~70℃	Tray	LY62L819216AGL-55SL
				Tape Reel	LY62L819216AGL-55SLT
			-40℃~85℃	Tray	LY62L819216AGL-55SLI
				Tape Reel	LY62L819216AGL-55SLIT

THIS PAGE IS LEFT BLANK INTENTIONASLY.