



REVISION HISTORY

<u>Revision</u>	<u>Description</u>	<u>Issue Date</u>
Rev. 1.0	Initial Issue	May.02.2023
Rev. 1.1	Revised <u>ORDERING INFORMATION</u> in page 11 32 Pin(450mil) SOP Packing Type : Tube→Tray	Aug.24.2023
Rev. 1.2	Revised Typo error of <u>PACKAGE OUTLINE DIMENSION</u> : 32 pin 8mm x 20mm TSOP I L1 in page 9	Aug.11.2025
Rev. 1.3	Deleted 32-pin 8mm x 20mm TSOP I in <u>FEATURES</u> --- Page1	Feb.25.2026

FEATURES

- Fast access time : 45/55/70ns
- Low power consumption:
Operating current : 15/12/10mA (TYP.)
Standby current : 1.5 μ A (TYP.)
- Single 2.7V ~ 5.5V power supply
- All outputs TTL compatible
- Fully static operation
- Tri-state output
- Data retention voltage : 1.5V (MIN.)
- **Green package available**
- Package : 32-pin 450 mil SOP
32-pin 8mm x 13.4mm sTSP

GENERAL DESCRIPTION

The LY62W2568B is a 2,097,152-bit low power CMOS static random access memory organized as 262,144 words by 8 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

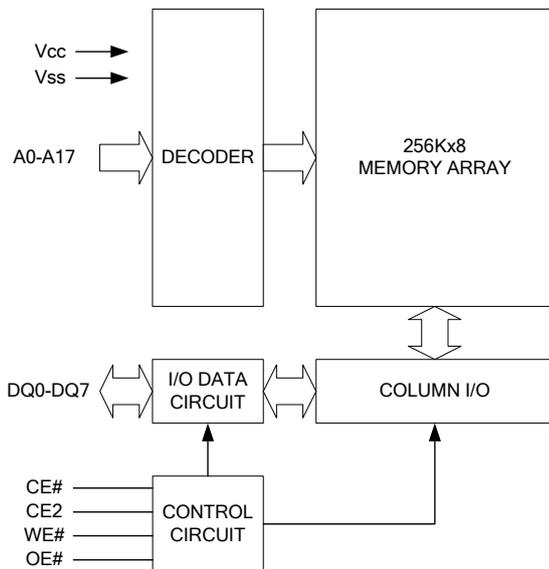
The LY62W2568B is well designed for very low power system applications, and particularly well suited for battery back-up nonvolatile memory application.

The LY62W2568B operates from a single power supply of 2.7V ~ 5.5V and all outputs are fully TTL compatible

PRODUCT FAMILY

Product Family	Operating Temperature	V _{CC} Range	Speed	Power Dissipation	
				Standby(I _{SB1} ,TYP.)	Operating(I _{CC} ,TYP.)
LY62W2568B	0 ~ 70°C	2.7 ~ 5.5V	45/55/70ns	1.5 μ A	15/12/10mA
LY62W2568B(I)	-40 ~ 85°C	2.7 ~ 5.5V	45/55/70ns	1.5 μ A	15/12/10mA

FUNCTIONAL BLOCK DIAGRAM

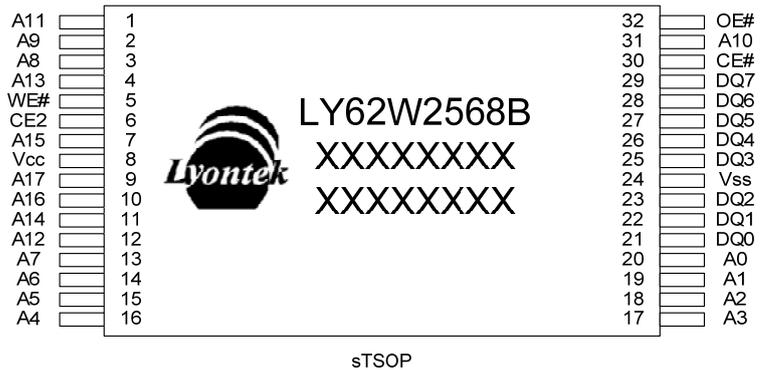
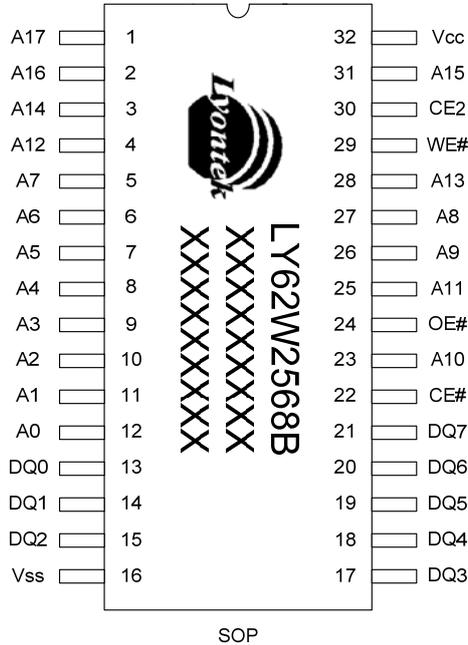


PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A17	Address Inputs
DQ0 – DQ7	Data Inputs/Outputs
CE#, CE2	Chip Enable Inputs
WE#	Write Enable Input
OE#	Output Enable Input
V _{CC}	Power Supply
V _{SS}	Ground
NC	No Connection



PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on V _{CC} relative to V _{SS}	V _{T1}	-0.5 to 6.5	V
Voltage on any other pin relative to V _{SS}	V _{T2}	-0.5 to V _{CC} +0.5	V
Operating Temperature	T _A	0 to 70(C grade)	°C
		-40 to 85(I grade)	
Storage Temperature	T _{STG}	-65 to 150	°C
Power Dissipation	P _D	1	W
DC Output Current	I _{OUT}	50	mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE#	CE2	OE#	WE#	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	X	High-Z	I _{SB1}
	X	L	X	X	High-Z	I _{SB1}
Output Disable	L	H	H	H	High-Z	I _{CC} , I _{CC1}
Read	L	H	L	H	D _{OUT}	I _{CC} , I _{CC1}
Write	L	H	X	L	D _{IN}	I _{CC} , I _{CC1}

Note: H = V_{IH}, L = V_{IL}, X = Don't care.

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DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP. ^{*4}	MAX.	UNIT	
Supply Voltage	V_{CC}		2.7	3.0	5.5	V	
Input High Voltage	V_{IH}^{*1}		$0.7 \cdot V_{CC}$	-	$V_{CC} + 0.3$	V	
Input Low Voltage	V_{IL}^{*2}		-0.2	-	0.6	V	
Input Leakage Current	I_{LI}	$V_{CC} \geq V_{IN} \geq V_{SS}$	-1	-	1	μA	
Output Leakage Current	I_{LO}	$V_{CC} \geq V_{OUT} \geq V_{SS}$, Output Disabled	-1	-	1	μA	
Output High Voltage	V_{OH}	$I_{OH} = -1mA$	2.4	2.7	-	V	
Output Low Voltage	V_{OL}	$I_{OL} = 2mA$	-	-	0.4	V	
Average Operating Power supply Current	I_{CC}	Cycle time = Min. $CE\# \leq 0.2V$ and $CE2 \geq V_{CC} - 0.2V$ $I_{I/O} = 0mA$ Other pins at 0.2V or $V_{CC} - 0.2V$	-45	15	25	mA	
			-55	12	20	mA	
			-70	10	18	mA	
	I_{CC1}	Cycle time = $1\mu s$ $CE\# \leq 0.2V$ and $CE2 \geq V_{CC} - 0.2V$ $I_{I/O} = 0mA$ Other pins at 0.2V or $V_{CC} - 0.2V$	-	2	4	mA	
Standby Power Supply Current	I_{SB1}	$CE\# \geq V_{CC} - 0.2V$ or $CE2 \leq 0.2V$ Others at 0.2V or $V_{CC} - 0.2V$	SL^{*5} 25°C	-	1.2	3.2	μA
			SLI^{*5} 40°C	-	1.5	3.5	μA
			SL	-	1.5	10	μA
			SLI	-	1.5	15	μA

Notes:

- $V_{IH}(\max) = V_{CC} + 3.0V$ for pulse width less than 10ns.
- $V_{IL}(\min) = V_{SS} - 3.0V$ for pulse width less than 10ns.
- Over/Undershoot specifications are characterized, not 100% tested.
- Typical values are included for reference only and are not guaranteed or tested.
Typical values are measured at $V_{CC} = V_{CC}(\text{TYP.})$ and $T_A = 25^\circ C$
- This parameter is measured at $V_{CC} = 3.0V$

CAPACITANCE ($T_A = 25^\circ C$, $f = 1.0MHz$)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C_{IN}	-	6	pF
Input/Output Capacitance	$C_{I/O}$	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0.2V to $V_{CC} - 0.2V$
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	$C_L = 30pF + 1TTL$, $I_{OH}/I_{OL} = -2mA/4mA$

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AC ELECTRICAL CHARACTERISTICS

(1) READ CYCLE

PARAMETER	SYM.	LY62W2568B-45		LY62W2568B-55		LY62W2568B-70		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t _{RC}	45	-	55	-	70	-	ns
Address Access Time	t _{AA}	-	45	-	55	-	70	ns
Chip Enable Access Time	t _{ACE}	-	45	-	55	-	70	ns
Output Enable Access Time	t _{OE}	-	25	-	30	-	35	ns
Chip Enable to Output in Low-Z	t _{CLZ} *	10	-	10	-	10	-	ns
Output Enable to Output in Low-Z	t _{OLZ} *	5	-	5	-	5	-	ns
Chip Disable to Output in High-Z	t _{CHZ} *	-	20	-	20	-	25	ns
Output Disable to Output in High-Z	t _{OHZ} *	-	20	-	20	-	25	ns
Output Hold from Address Change	t _{OH}	10	-	10	-	10	-	ns

(2) WRITE CYCLE

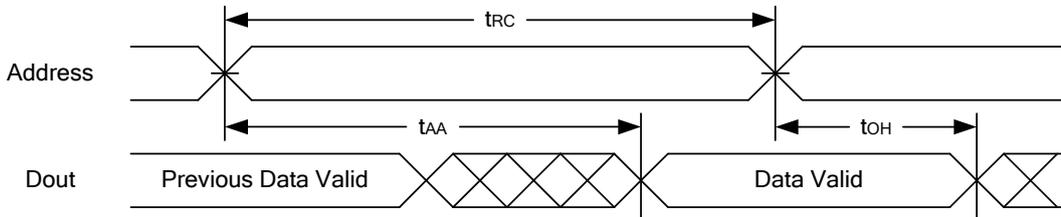
PARAMETER	SYM.	LY62W2568B-45		LY62W2568B-55		LY62W2568B-70		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t _{WC}	45	-	55	-	70	-	ns
Address Valid to End of Write	t _{AW}	40	-	50	-	60	-	ns
Chip Enable to End of Write	t _{CW}	40	-	50	-	60	-	ns
Address Set-up Time	t _{AS}	0	-	0	-	0	-	ns
Write Pulse Width	t _{WP}	35	-	45	-	55	-	ns
Write Recovery Time	t _{WR}	0	-	0	-	0	-	ns
Data to Write Time Overlap	t _{DW}	20	-	25	-	30	-	ns
Data Hold from End of Write Time	t _{DH}	0	-	0	-	0	-	ns
Output Active from End of Write	t _{OW} *	5	-	5	-	5	-	ns
Write to Output in High-Z	t _{WHZ} *	-	20	-	20	-	25	ns

*These parameters are guaranteed by device characterization, but not production tested.

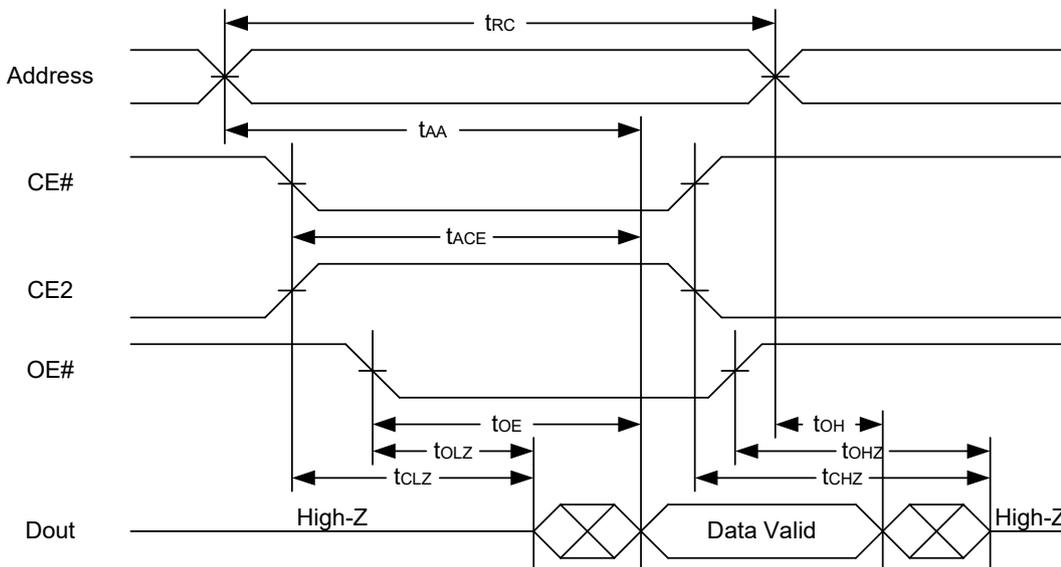


TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)



READ CYCLE 2 (CE# and CE2 and OE# Controlled) (1,3,4,5)

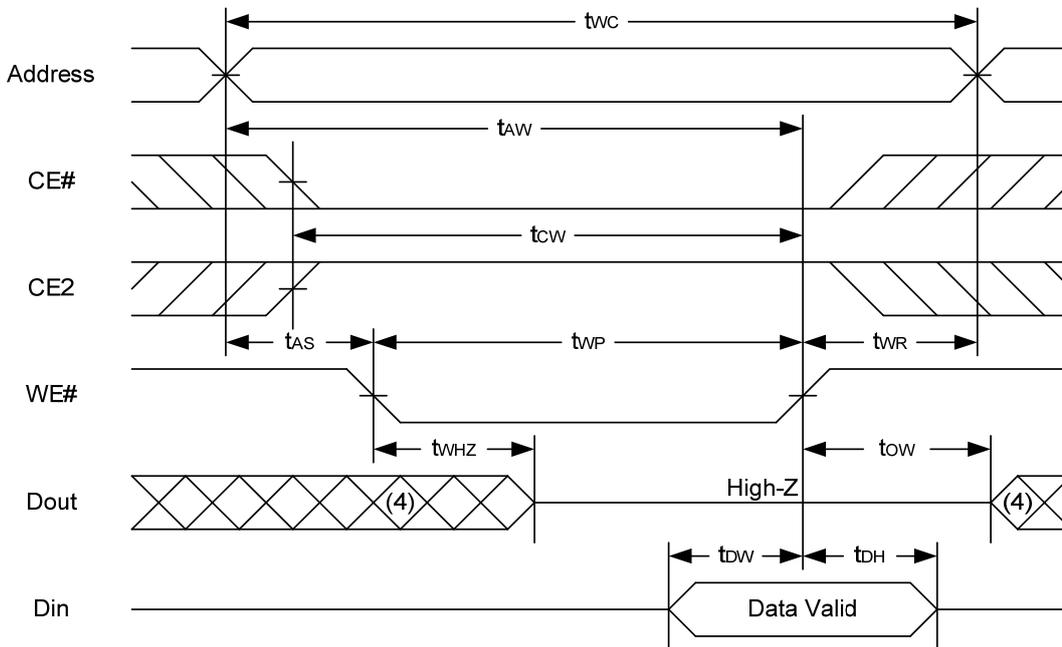


Notes :

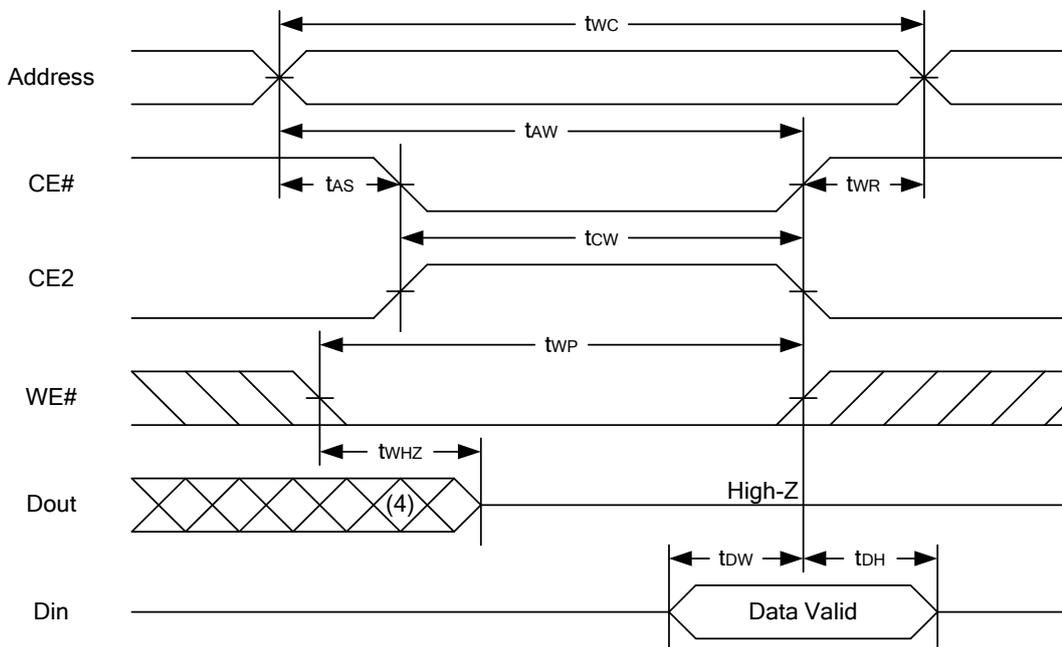
1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low, CE2 = high.
3. Address must be valid prior to or coincident with CE# = low, CE2 = high; otherwise t_{AA} is the limiting parameter.
4. t_{TCLZ} , t_{TOLZ} , t_{TCHZ} and t_{TOHZ} are specified with $C_L = 5pF$. Transition is measured $\pm 500mV$ from steady state.
5. At any given temperature and voltage condition, t_{TCHZ} is less than t_{TCLZ} , t_{TOHZ} is less than t_{TOLZ} .



WRITE CYCLE 1 (WE# Controlled) (1,2,4,5)



WRITE CYCLE 2 (CE# and CE2 Controlled) (1,4,5)



Notes :

1. A write occurs during the overlap of a low CE#, high CE2, low WE#.
2. During a WE# controlled write cycle with OE# low, t_{WP} must be greater than $t_{WHZ} + t_{DW}$ to allow the drivers to turn off and data to be placed on the bus.
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the CE# low transition and CE2 high transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
5. t_{OW} and t_{WHZ} are specified with $CL = 5pF$. Transition is measured $\pm 500mV$ from steady state.



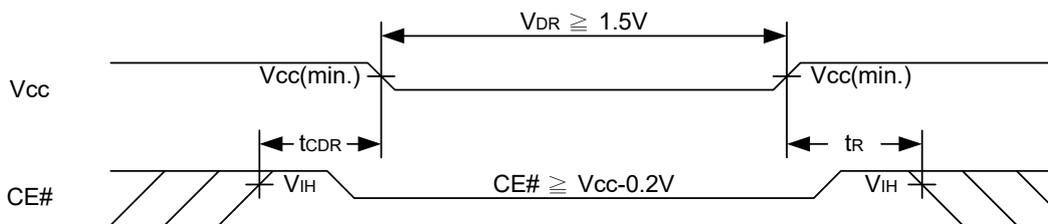
DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT		
V _{CC} for Data Retention	V _{DR}	CE# ≥ V _{CC} -0.2V or CE2 ≤ 0.2V	1.5	-	5.5	V		
Data Retention Current	I _{DR}	V _{CC} = 1.5V CE# ≥ V _{CC} -0.2V or CE2 ≤ 0.2V Other pins at 0.2V or V _{CC} -0.2V	SL	25°C	-	1.2	3.2	μA
			SLI	40°C	-	1.5	3.5	μA
			SL		-	1.5	10	μA
			SLI		-	1.5	15	μA
Chip Disable to Data Retention Time	t _{CDR}	See Data Retention Waveforms (below)	0	-	-	ns		
Recovery Time	t _R		t _{RC} *	-	-	ns		

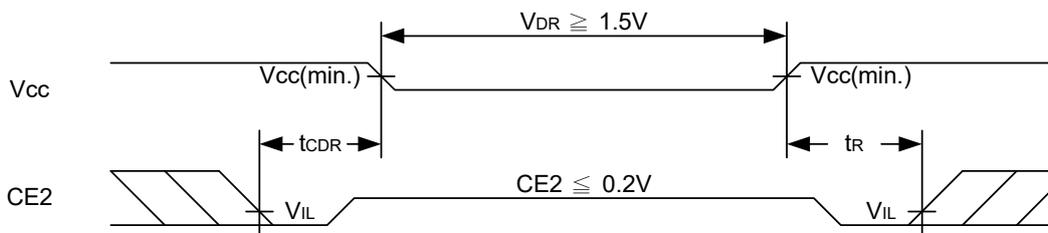
t_{RC}* = Read Cycle Time

DATA RETENTION WAVEFORM

Low V_{CC} Data Retention Waveform (1) (CE# controlled)



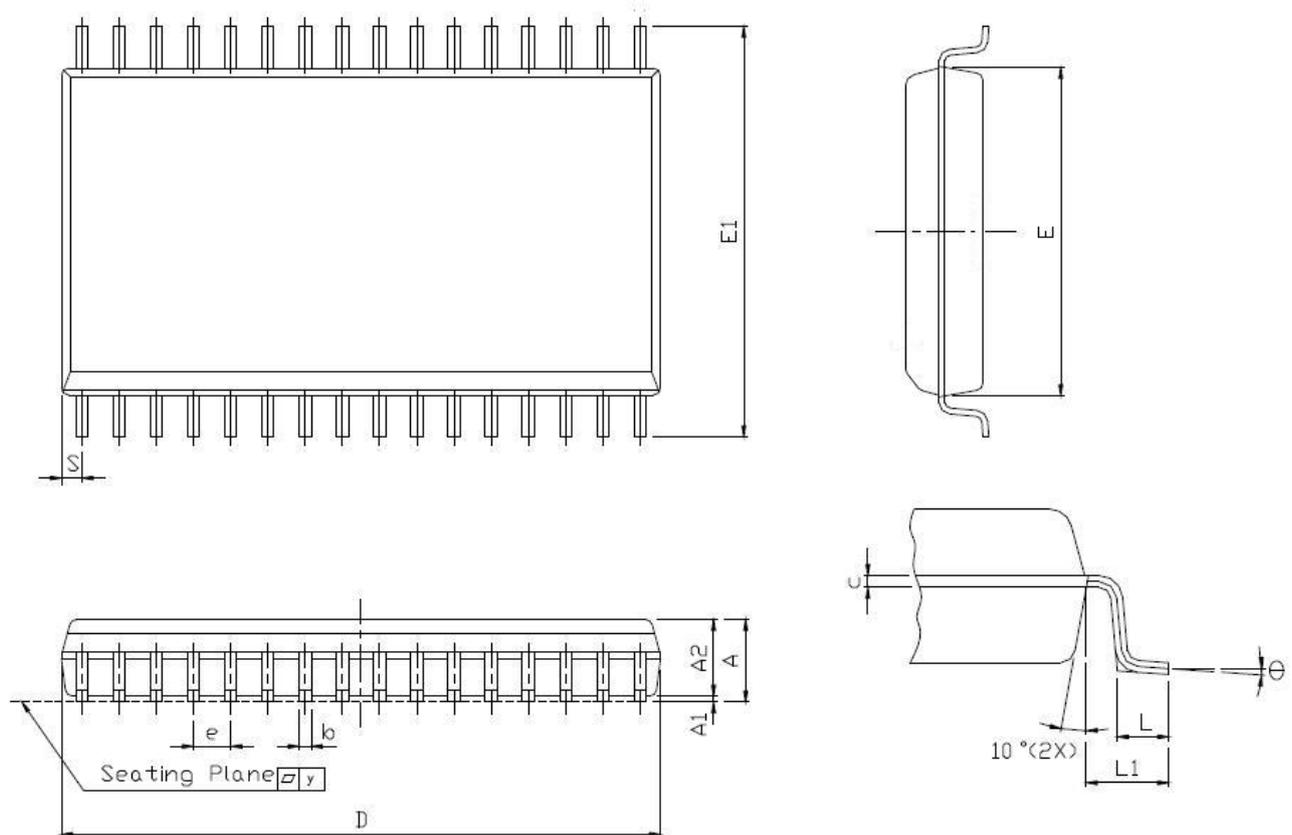
Low V_{CC} Data Retention Waveform (2) (CE2 controlled)





PACKAGE OUTLINE DIMENSION

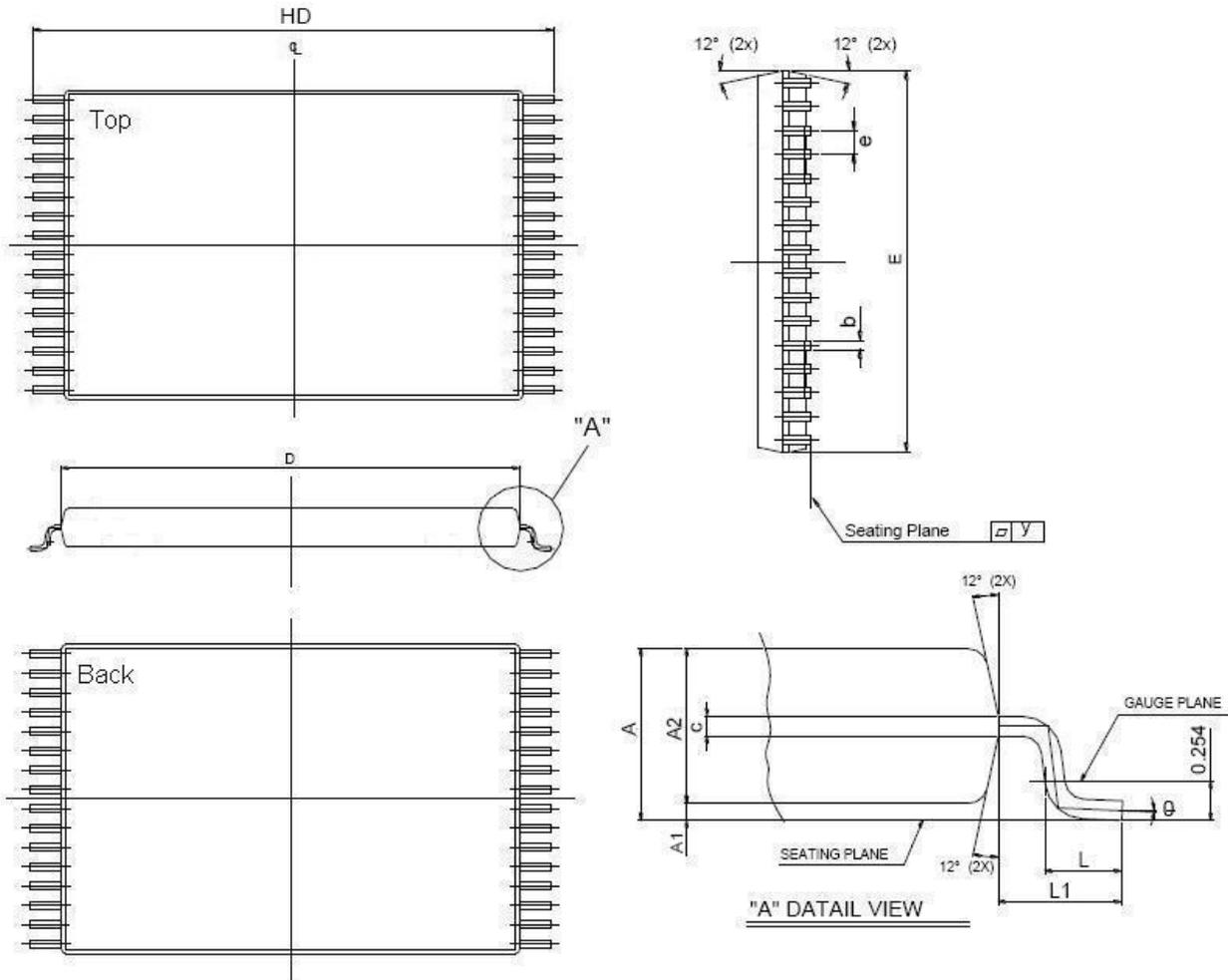
32 pin 450 mil SOP Package Outline Dimension



SYM.	UNIT	INCH.(BASE)	MM(REF)
A		0.120(MAX)	3.048(MAX)
A1		0.004(MIN)	0.102(MIN)
A2		0.116(MAX)	2.946(MAX)
b		0.016(TYP)	0.406(TYP)
c		0.008(TYP)	0.203(TYP)
D		0.817(MAX)	20.75(MAX)
E		0.445±0.006	11.303±0.152
E1		0.555±0.025	14.097±0.635
e		0.050(TYP)	1.270(TYP)
L		0.033±0.017	0.838±0.432
L1		0.055±0.008	1.397±0.203
S		0.026(MAX)	0.660(MAX)
y		0.004(MAX)	0.101(MAX)
Θ		0° -10°	0° -10°



32 pin 8mm x 13.4mm sTSOP Package Outline Dimension



SYM.	UNIT	INCH(BASE)	MM(REF)
A		0.049 (MAX)	1.25 (MAX)
A1		0.004 ±0.002	0.10 ±0.05
A2		0.039 ±0.002	1.00 ±0.05
b		0.009 ±0.002	0.22 ±0.05
c		0.006 ±0.002	0.155 ±0.055
D		0.465 ±0.008	11.80 ±0.20
E		0.315 ±0.008	8.00 ±0.20
e		0.020 (TYP)	0.50 (TYP)
HD		0.528±0.008	13.40 ±0.20.
L		0.02 ±0.008	0.50 ±0.20
L1		0.031 ±0.005	0.8 ±0.125
y		0.003 (MAX)	0.076 (MAX)
θ		0°~5°	0°~5°



ORDERING INFORMATION

Package Type	Access Time (Speed)(ns)	Power Type	Temperature Range(°C)	Packing Type	Lyontek Item No.
32Pin(450mil) SOP	45	Special Ultra Low Power	0°C~70°C	Tray	LY62W2568BSL-45SL
				Tape Reel	LY62W2568BSL-45SLT
			-40°C~85°C	Tray	LY62W2568BSL-45SLI
				Tape Reel	LY62W2568BSL-45SLIT
	55	Special Ultra Low Power	0°C~70°C	Tray	LY62W2568BSL-55LL
				Tape Reel	LY62W2568BSL-55LLT
			-40°C~85°C	Tray	LY62W2568BSL-55LLI
				Tape Reel	LY62W2568BSL-55LLIT
	70	Special Ultra Low Power	0°C~70°C	Tray	LY62W2568BSL-70SL
				Tape Reel	LY62W2568BSL-70SLT
			-40°C~85°C	Tray	LY62W2568BSL-70SLI
				Tape Reel	LY62W2568BSL-70SLIT



ORDERING INFORMATION

Package Type	Access Time (Speed)(ns)	Power Type	Temperature Range(°C)	Packing Type	Lyontek Item No.
32Pin (8mmx13.4mm) sTSOP	45	Special Ultra Low Power	0°C~70°C	Tray	LY62W2568BRL-45SL
				Tape Reel	LY62W2568BRL-45SLT
			-40°C~85°C	Tray	LY62W2568BRL-45SLI
				Tape Reel	LY62W2568BRL-45SLIT
	55	Special Ultra Low Power	0°C~70°C	Tray	LY62W2568BRL-55LL
				Tape Reel	LY62W2568BRL-55LLT
			-40°C~85°C	Tray	LY62W2568BRL-55LLI
				Tape Reel	LY62W2568BRL-55LLIT
	70	Special Ultra Low Power	0°C~70°C	Tray	LY62W2568BRL-70SL
				Tape Reel	LY62W2568BRL-70SLT
			-40°C~85°C	Tray	LY62W2568BRL-70SLI
				Tape Reel	LY62W2568BRL-70SLIT



Lyontek Inc.

LY62W2568B

Rev. 1.3

256K X 8 BIT LOW POWER CMOS SRAM

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