



**Lyontek Inc.**

**LY62W51216B**

Rev. 1.0

**512K X 16 BIT LOW POWER CMOS SRAM**

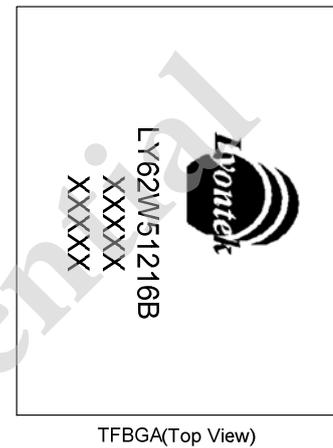
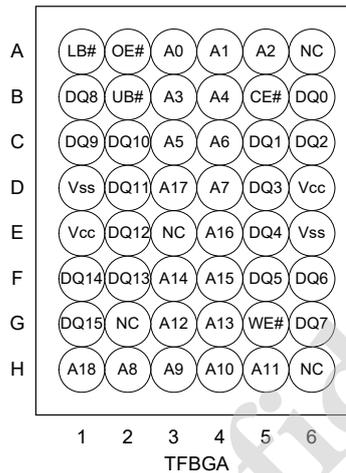
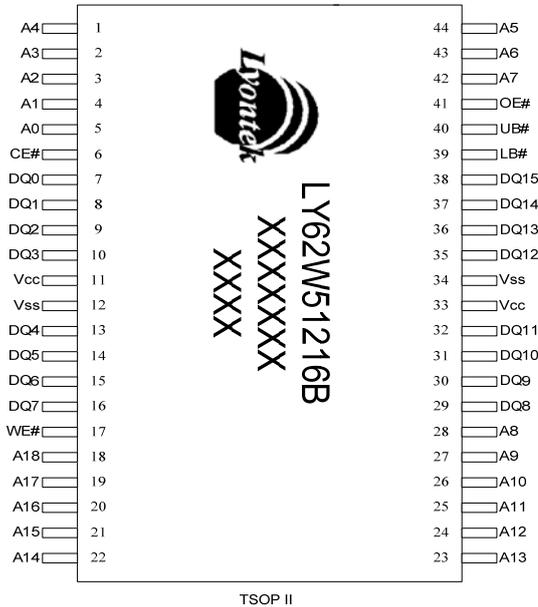
---

**REVISION HISTORY**

<u>Revision</u>	<u>Description</u>	<u>Issue Date</u>
Rev. 1.0	Initial Issue	Jan.30.2024

Lyontek Confidential



**PIN CONFIGURATION**

**ABSOLUTE MAXIMUM RATINGS\***

PARAMETER	SYMBOL	RATING	UNIT
Voltage on Vcc relative to Vss	V <sub>T1</sub>	-0.5 to 6.5	V
Voltage on any other pin relative to Vss	V <sub>T2</sub>	-0.5 to V <sub>CC</sub> +0.5	V
Operating Temperature	T <sub>A</sub>	0 to 70(C grade)	°C
		-40 to 85(I grade)	
Storage Temperature	T <sub>STG</sub>	-65 to 150	°C
Power Dissipation	P <sub>D</sub>	1	W
DC Output Current	I <sub>OUT</sub>	50	mA

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.



### TRUTH TABLE

MODE	CE#	OE#	WE#	LB#	UB#	I/O OPERATION		SUPPLY CURRENT
						DQ0-DQ7	DQ8-DQ15	
Standby	H	X	X	X	X	High - Z	High - Z	I <sub>SB</sub> , I <sub>SB1</sub>
	X	X	X	H	H	High - Z	High - Z	
Output Disable	L	H	H	L	X	High - Z	High - Z	I <sub>CC</sub> , I <sub>CC1</sub>
	L	H	H	X	L	High - Z	High - Z	
Read	L	L	H	L	H	D <sub>OUT</sub>	High - Z	I <sub>CC</sub> , I <sub>CC1</sub>
	L	L	H	H	L	High - Z	D <sub>OUT</sub>	
	L	L	H	L	L	D <sub>OUT</sub>	D <sub>OUT</sub>	
Write	L	X	L	L	H	D <sub>IN</sub>	High - Z	I <sub>CC</sub> , I <sub>CC1</sub>
	L	X	L	H	L	High - Z	D <sub>IN</sub>	
	L	X	L	L	L	D <sub>IN</sub>	D <sub>IN</sub>	

Note: H = V<sub>IH</sub>, L = V<sub>IL</sub>, X = Don't care.

### DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.* <sup>4</sup>	MAX.	UNIT	
Supply Voltage	V <sub>CC</sub>		2.7	3.0	5.5	V	
Input High Voltage	V <sub>IH</sub> <sup>*1</sup>	V <sub>CC</sub> = 2.7 ~ 3.6V	2.2	-	V <sub>CC</sub> +0.5	V	
		V <sub>CC</sub> = 4.5 ~ 5.5V	2.4	-	V <sub>CC</sub> +0.5	V	
Input Low Voltage	V <sub>IL</sub> <sup>*2</sup>	V <sub>CC</sub> = 2.7 ~ 3.6V	-0.2	-	0.6	V	
		V <sub>CC</sub> = 4.5 ~ 5.5V	-0.2	-	0.8	V	
Input Leakage Current	I <sub>LI</sub>	V <sub>CC</sub> ≥ V <sub>IN</sub> ≥ V <sub>SS</sub>	-1	-	1	μA	
Output Leakage Current	I <sub>LO</sub>	V <sub>CC</sub> ≥ V <sub>OUT</sub> ≥ V <sub>SS</sub> , Output Disabled	-1	-	1	μA	
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -1mA	2.4	2.7	-	V	
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2mA	-	-	0.4	V	
Average Operating Power supply Current	I <sub>CC</sub>	Cycle time = Min. CE# = V <sub>IL</sub> , I <sub>I/O</sub> = 0mA Other pins at V <sub>IL</sub> or V <sub>IH</sub>	-45	12	20	mA	
			-55	10	18	mA	
Average Operating Power supply Current	I <sub>CC1</sub>	Cycle time = 1μs CE# = 0.2V, I <sub>I/O</sub> = 0mA Other pins at 0.2V or V <sub>CC</sub> - 0.2V	-	3	5	mA	
			-	3	5	mA	
Standby Power Supply Current	I <sub>SB</sub>	CE# = V <sub>IH</sub> , Other pins at V <sub>IL</sub> or V <sub>IH</sub>	-	0.15	2	mA	
			-	0.15	2	mA	
	I <sub>SB1</sub>	CE# ≥ V <sub>CC</sub> - 0.2V or CE2 ≤ 0.2V; and Other pins at 0.2V or V <sub>CC</sub> - 0.2V	SL <sup>*5</sup> 25°C	-	3	8	μA
			SLI <sup>*5</sup> 40°C	-	4	10	μA
			SL	-	3	20	μA
SLI	-	3	25	μA			

Notes:

- V<sub>IH</sub>(max) = V<sub>CC</sub> + 3.0V for pulse width less than 10ns.
- V<sub>IL</sub>(min) = V<sub>SS</sub> - 3.0V for pulse width less than 10ns.
- Over/Undershoot specifications are characterized, not 100% tested.
- Typical values are included for reference only and are not guaranteed or tested.  
Typical values are measured at V<sub>CC</sub> = V<sub>CC</sub>(TYP.) and T<sub>A</sub> = 25°C
- This parameter is measured at V<sub>CC</sub> = 3.0V

**CAPACITANCE (T<sub>A</sub> = 25°C, f = 1.0MHz)**

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C <sub>IN</sub>	-	6	pF
Input/Output Capacitance	C <sub>I/O</sub>	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

**AC TEST CONDITIONS**

Input Pulse Levels	0.2V to V <sub>CC</sub> - 0.2V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	C <sub>L</sub> = 30pF + 1TTL, I <sub>OH</sub> /I <sub>OL</sub> = -1mA/2mA

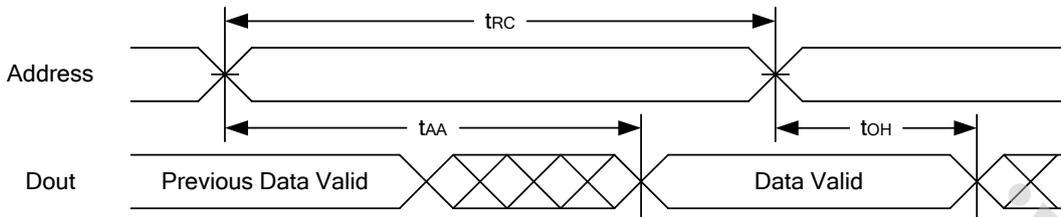
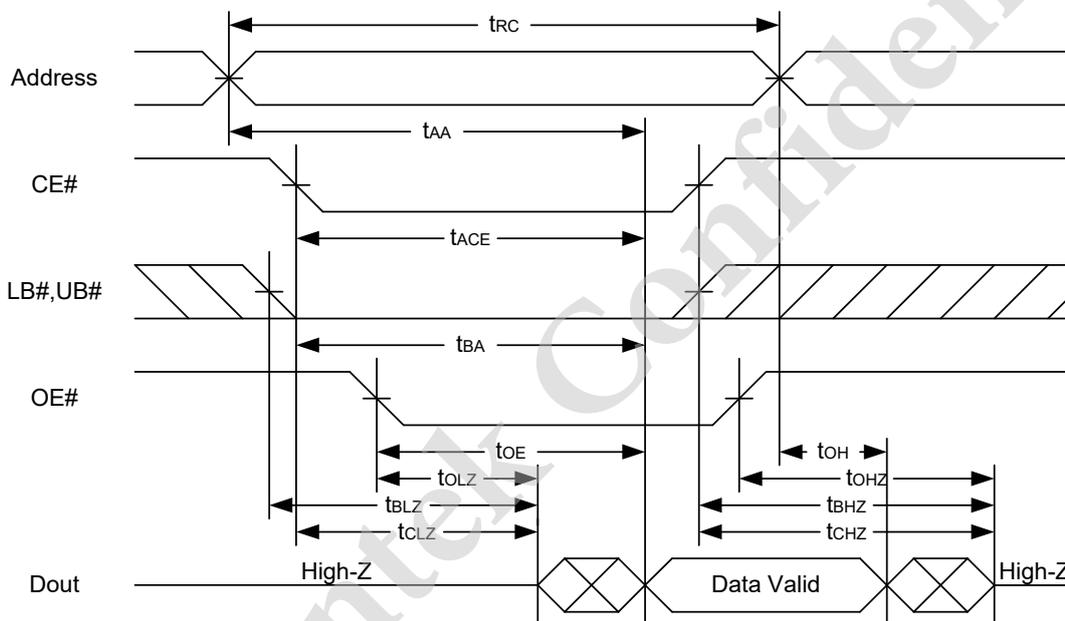
**AC ELECTRICAL CHARACTERISTICS**
**(1) READ CYCLE**

PARAMETER	SYM.	LY62W51216B-45		LY62W51216B-55		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t <sub>RC</sub>	45	-	55	-	ns
Address Access Time	t <sub>AA</sub>	-	45	-	55	ns
Chip Enable Access Time	t <sub>ACE</sub>	-	45	-	55	ns
Output Enable Access Time	t <sub>OE</sub>	-	25	-	30	ns
Chip Enable to Output in Low-Z	t <sub>CLZ</sub> *	10	-	10	-	ns
Output Enable to Output in Low-Z	t <sub>OLZ</sub> *	5	-	5	-	ns
Chip Disable to Output in High-Z	t <sub>CHZ</sub> *	-	15	-	20	ns
Output Disable to Output in High-Z	t <sub>OHZ</sub> *	-	15	-	2	ns
Output Hold from Address Change	t <sub>OH</sub>	10	-	10	-	ns
LB#, UB# Access Time	t <sub>BA</sub>	-	45	-	55	ns
LB#, UB# to High-Z Output	t <sub>BHZ</sub> *	-	15	-	25	ns
LB#, UB# to Low-Z Output	t <sub>BLZ</sub> *	10	-	10	-	ns

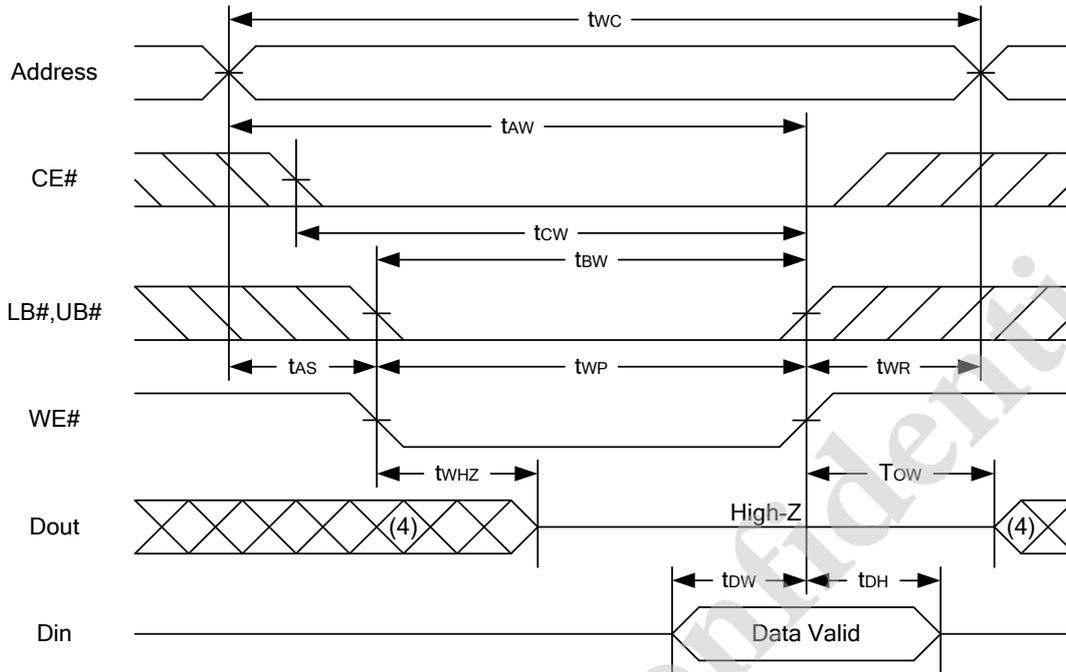
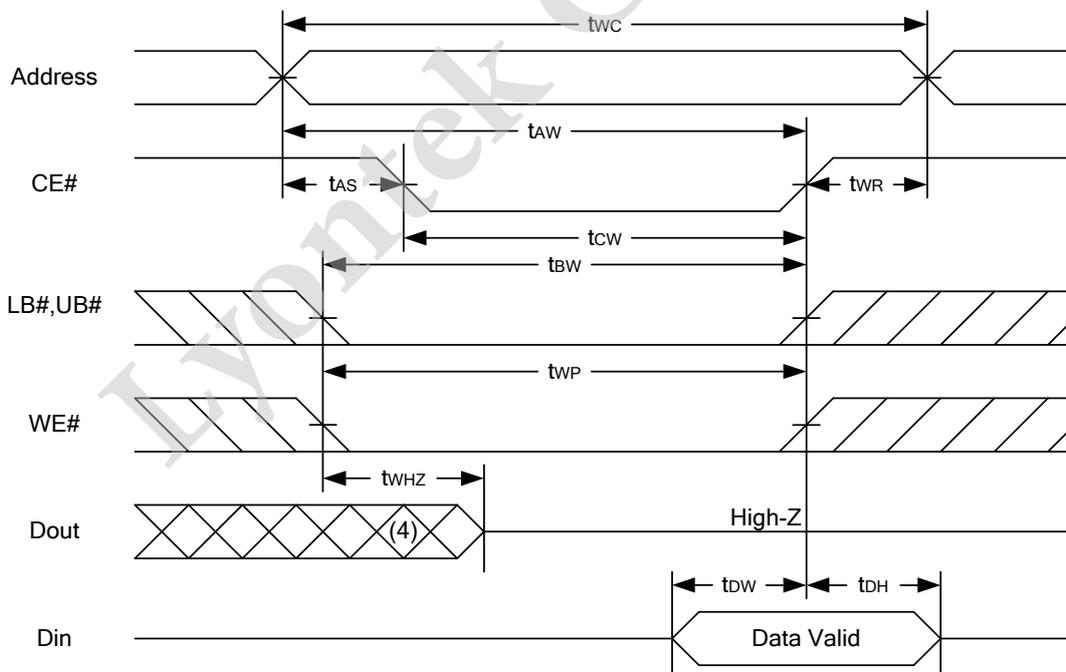
**(2) WRITE CYCLE**

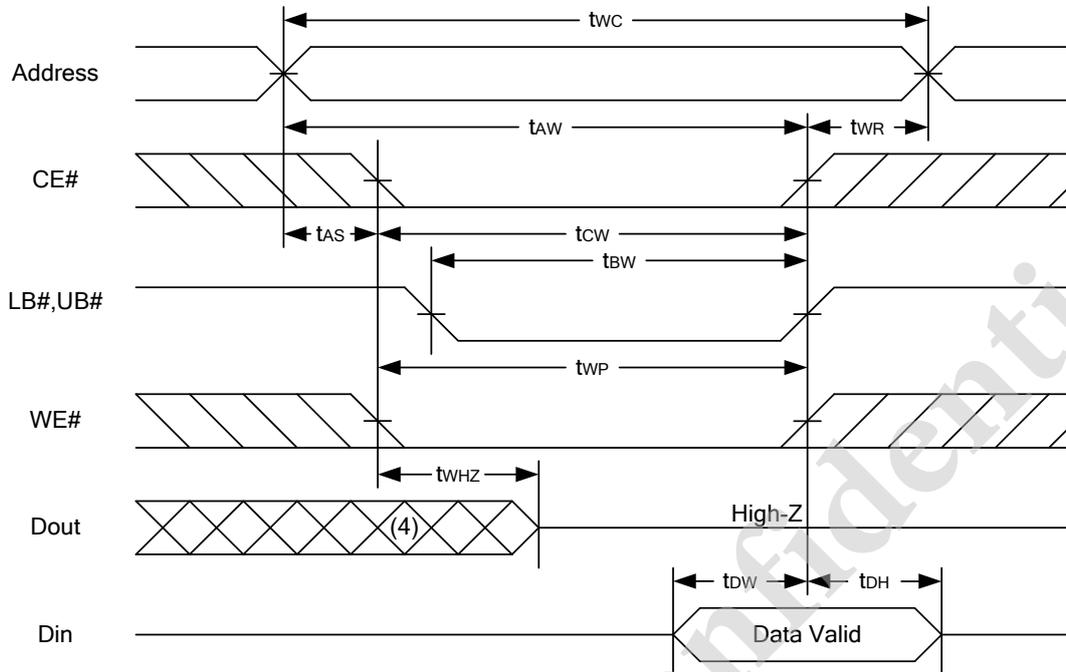
PARAMETER	SYM.	LY62W51216B-45		LY62W51216B-55		UNIT
		MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t <sub>WC</sub>	45	-	55	-	ns
Address Valid to End of Write	t <sub>AW</sub>	40	-	50	-	ns
Chip Enable to End of Write	t <sub>CW</sub>	40	-	50	-	ns
Address Set-up Time	t <sub>AS</sub>	0	-	0	-	ns
Write Pulse Width	t <sub>WP</sub>	35	-	45	-	ns
Write Recovery Time	t <sub>WR</sub>	0	-	0	-	ns
Data to Write Time Overlap	t <sub>DW</sub>	20	-	25	-	ns
Data Hold from End of Write Time	t <sub>DH</sub>	0	-	0	-	ns
Output Active from End of Write	t <sub>OW</sub> *	5	-	5	-	ns
Write to Output in High-Z	t <sub>WHZ</sub> *	-	20	-	20	ns
LB#, UB# Valid to End of Write	t <sub>BW</sub>	35	-	45	-	ns

\*These parameters are guaranteed by device characterization, but not production tested.

**TIMING WAVEFORMS**
**READ CYCLE 1 (Address Controlled) (1,2)**

**READ CYCLE 2 (CE# and OE# Controlled) (1,3,4,5)**

**Notes :**

1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low, LB# or UB# = low.
3. Address must be valid prior to or coincident with CE# = low, LB# or UB# = low transition; otherwise  $t_{AA}$  is the limiting parameter.
4.  $t_{CLZ}$ ,  $t_{BLZ}$ ,  $t_{OLZ}$ ,  $t_{CHZ}$ ,  $t_{BHZ}$  and  $t_{OHZ}$  are specified with  $C_L = 5pF$ . Transition is measured  $\pm 500mV$  from steady state.
5. At any given temperature and voltage condition,  $t_{CHZ}$  is less than  $t_{CLZ}$ ,  $t_{BHZ}$  is less than  $t_{BLZ}$ ,  $t_{OHZ}$  is less than  $t_{OLZ}$ .

**WRITE CYCLE 1 (WE# Controlled) (1,2,4,5)**

**WRITE CYCLE 2 (CE# Controlled) (1,4,5)**


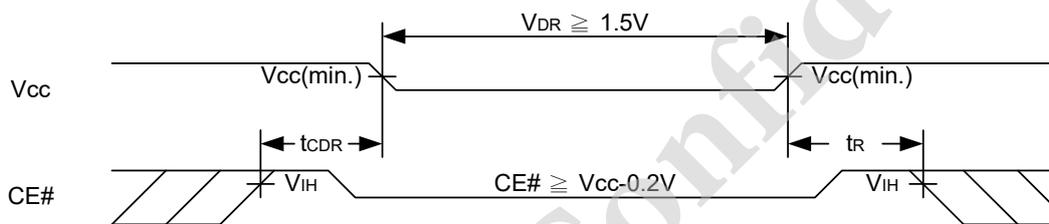
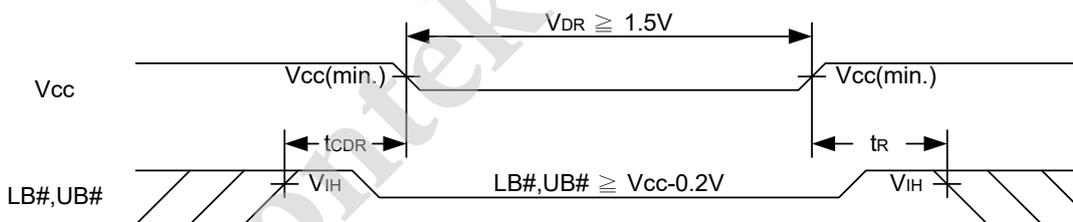
**WRITE CYCLE 3 (LB#,UB# Controlled) (1,4,5)**

**Notes :**

1. A write occurs during the overlap of a low CE#, low WE#, LB# or UB# = low.
2. During a WE# controlled write cycle with OE# low,  $t_{WP}$  must be greater than  $t_{WHZ} + t_{BW}$  to allow the drivers to turn off and data to be placed on the bus.
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the CE#, LB#, UB# low transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
5.  $t_{OW}$  and  $t_{WHZ}$  are specified with  $C_L = 5pF$ . Transition is measured  $\pm 500mV$  from steady state.

**DATA RETENTION CHARACTERISTICS**

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT		
Vcc for Data Retention	V <sub>DR</sub>	CE# ≥ V <sub>CC</sub> - 0.2V	1.5	-	5.5	V		
Data Retention Current	I <sub>DR</sub>	V <sub>CC</sub> = 1.5V CE# ≥ V <sub>CC</sub> - 0.2V Other pins at 0.2V or V <sub>CC</sub> -0.2V	SL	25°C	-	3	8	μA
			SLI	40°C	-	4	10	μA
			SL		-	3	20	μA
			SLI		-	3	25	μA
Chip Disable to Data Retention Time	t <sub>CDR</sub>	See Data Retention Waveforms (below)	0	-	-	ns		
Recovery Time	t <sub>R</sub>		t <sub>RC</sub> *	-	-	ns		

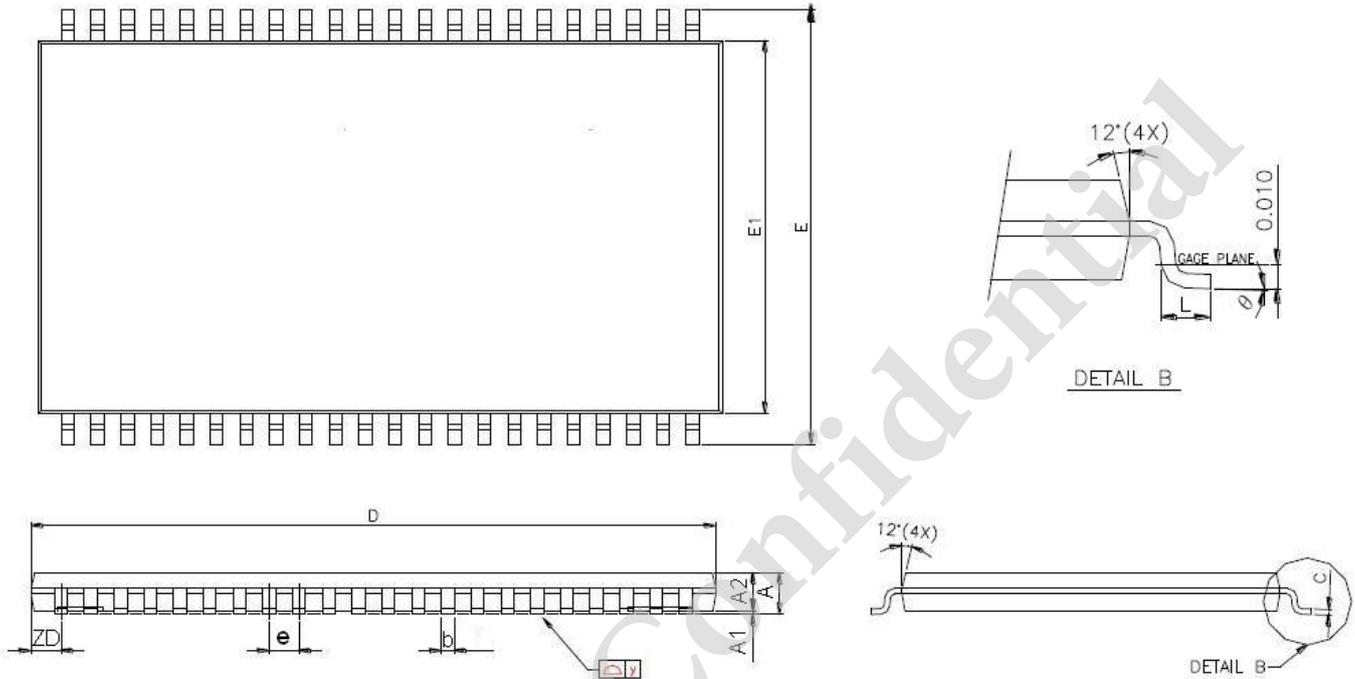
 t<sub>RC</sub>\* = Read Cycle Time

**DATA RETENTION WAVEFORM**
**Low Vcc Data Retention Waveform (1) (CE# controlled)**

**Low Vcc Data Retention Waveform (2) (LB#, UB# controlled)**




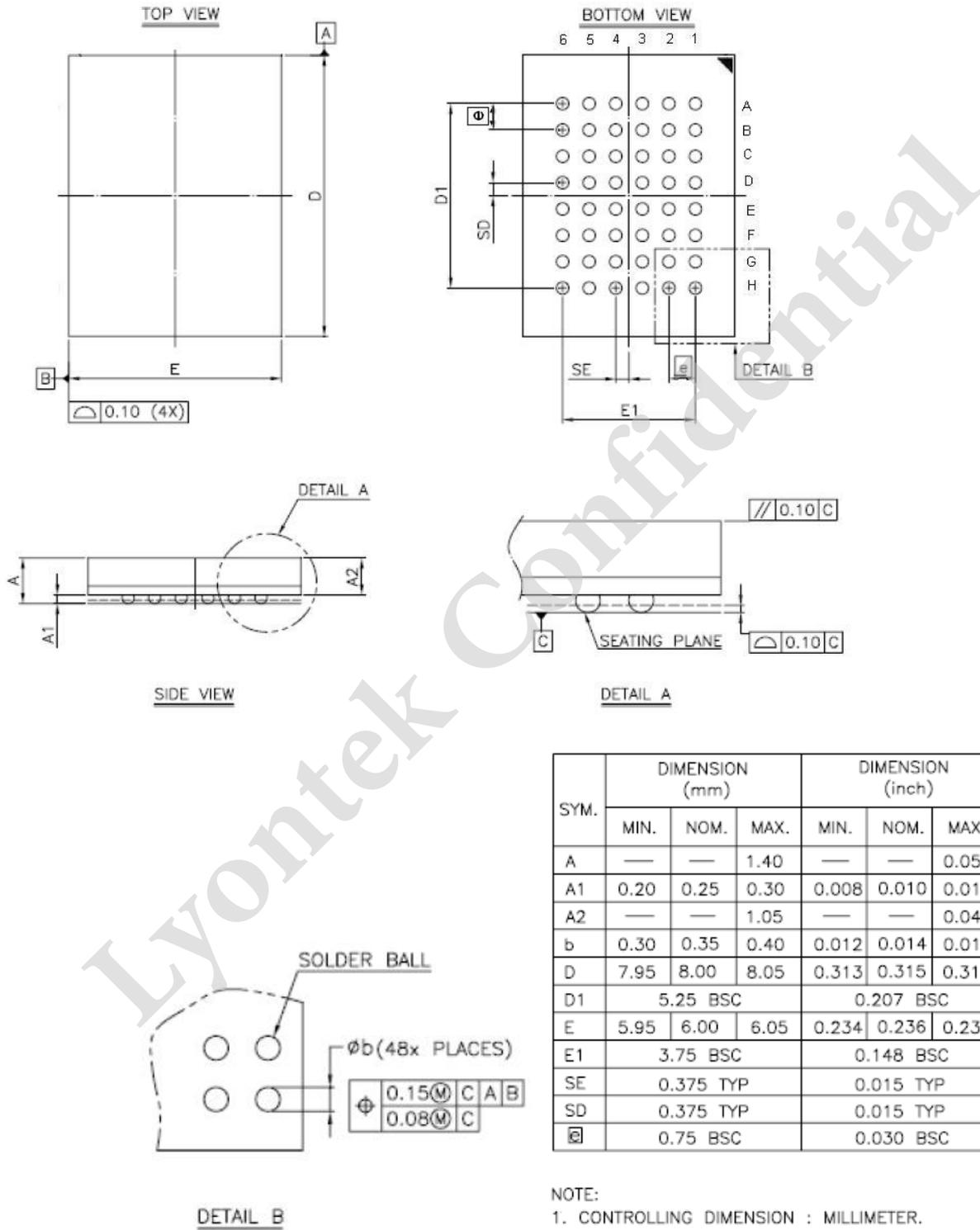
**PACKAGE OUTLINE DIMENSION**

**44-pin 400mil TSOP-II Package Outline Dimension**



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN MILS		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	-	-	1.20	-	-	47.2
A1	0.05	0.10	0.15	2.0	3.9	5.9
A2	0.95	1.00	1.05	37.4	39.4	41.3
b	0.30	-	0.45	11.8	-	17.7
c	0.12	-	0.21	4.7	-	8.3
D	18.212	18.415	18.618	717	725	733
E	11.506	11.760	12.014	453	463	473
E1	9.957	10.160	10.363	392	400	408
e	-	0.800	-	-	31.5	-
L	0.40	0.50	0.60	15.7	19.7	23.6
ZD	-	0.805	-	-	31.7	-
y	-	-	0.076	-	-	3
θ	0°	3°	6°	0°	3°	6°

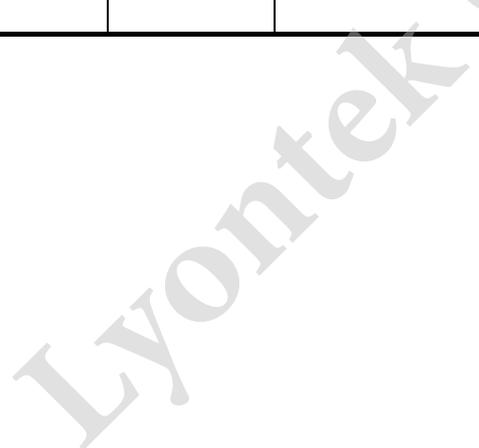
#### 48-ball 6mm × 8mm TFBGA Package Outline Dimension





#### ORDERING INFORMATION

Package Type	Access Time (Speed/ns)	Power Type	Temperature Range(°C)	Packing Type	Lyontek Item No.
44Pin 400mil TSOP-II	45	Special Ultra Low Power	0°C~70°C	Tray	LY62W51216BML-45SL
				Tape Reel	LY62W51216BML-45SLT
			-40°C~85°C	Tray	LY62W51216BML-45SLI
				Tape Reel	LY62W51216BML-45SLIT
	55	Special Ultra Low Power	0°C~70°C	Tray	LY62W51216BML-55SL
				Tape Reel	LY62W51216BML-55SLT
			-40°C~85°C	Tray	LY62W51216BML-55SLI
				Tape Reel	LY62W51216BML-55SLIT
48-Ball 6mm x 8mm TFBGA	45	Special Ultra Low Power	0°C~70°C	Tray	LY62W51216BGL-45SL
				Tape Reel	LY62W51216BGL-45SLT
			-40°C~85°C	Tray	LY62W51216BGL-45SLI
				Tape Reel	LY62W51216BGL-45SLIT
	55	Special Ultra Low Power	0°C~70°C	Tray	LY62W51216BGL-55SL
				Tape Reel	LY62W51216BGL-55SLT
			-40°C~85°C	Tray	LY62W51216BGL-55SLI
				Tape Reel	LY62W51216BGL-55SLIT





THIS PAGE IS LEFT BLANK INTENTIONALLY.

Lyontek Confidential