



Lyontek Inc.

LY62W5128B

Rev. 1.4

512K X 8 BIT LOW POWER CMOS SRAM

REVISION HISTORY

<u>Revision</u>	<u>Description</u>	<u>Issue Date</u>
Rev. 1.0	Initial Issue	Jun.21.2023
Rev. 1.1	Revised <u>ORDERING INFORMATION</u> in page 14 32 Pin(450mil) SOP Packing Type : Tube→Tray	Aug.24.2023
Rev. 1.2	Revised <u>DC ELECTRICAL CHARACTERISTICS</u> :ICC TEST CONDITION--- Page4	Mar.27.2024
Rev. 1.3	Revised <u>AC ELECTRICAL CHARACTERISTICS</u> : (1) READ CYCLE: LY62W5128B-45 MIN.55→45 ----Page5	Dec.02.2024
Rev. 1.4	Revised Typo error of <u>PACKAGE OUTLINE DIMENSION</u> : 32 pin 8mm x 20mm TSOP I L1 in page 10	Aug.11.2025



FEATURES

- Fast access time : 45/55ns
- Low power consumption:
Operating current : 15/12mA (TYP.)
Standby current : 2.2 μ A (TYP.)
- Single 2.7V ~ 5.5V power supply
- All outputs TTL compatible
- Fully static operation
- Tri-state output
- Data retention voltage : 1.5V (MIN.)
- **Green package available**
- Package : 32-pin 450mil SOP
32-pin 8mm x 20mm TSOP I
32-pin 8mm x 13.4mm sTSP
36-ball 6mm x 8mm TFBGA

GENERAL DESCRIPTION

The LY62W5128B is a 4,194,304-bit low power CMOS static random access memory organized as 524,288 words by 8 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

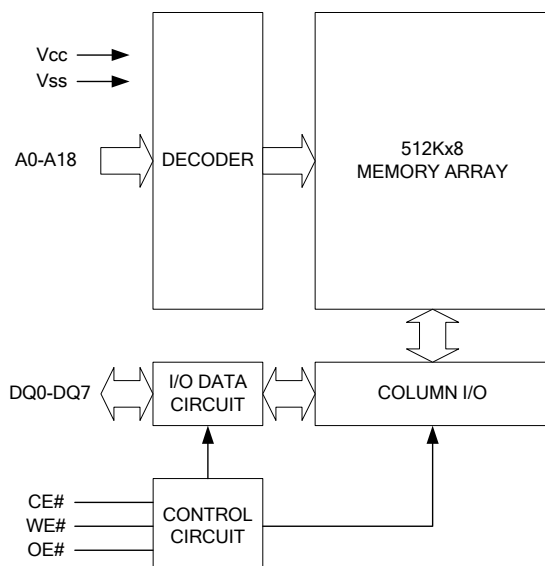
The LY62W5128B is well designed for very low power system applications, and particularly well suited for battery back-up nonvolatile memory application.

The LY62W5128B operates from a single power supply of 2.7V ~ 5.5V and all outputs are fully TTL compatible.

PRODUCT FAMILY

Product Family	Operating Temperature	V _{CC} Range	Speed	Power Dissipation	
				Standby(I _{SB1} , TYP.)	Operating(I _{CC} , TYP.)
LY62W5128B	0 ~ 70°C	2.7 ~ 5.5V	45/55ns	2.2 μ A	15/12mA
LY62W5128B(I)	-40 ~ 85°C	2.7 ~ 5.5V	45/55ns	2.2 μ A	15/12mA

FUNCTIONAL BLOCK DIAGRAM

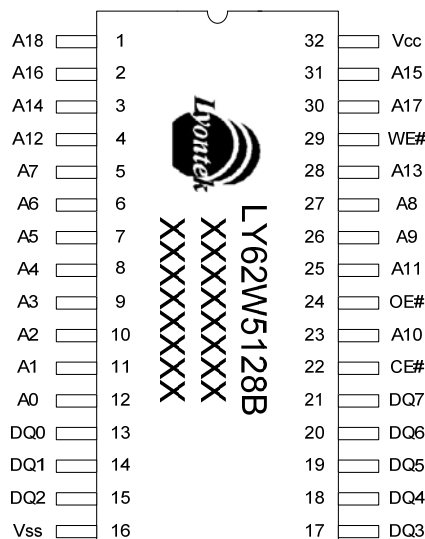


PIN DESCRIPTION

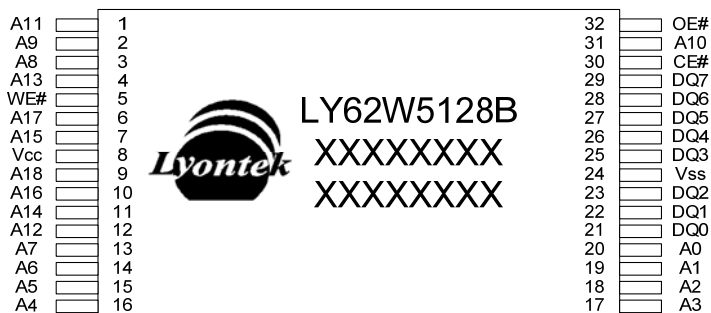
SYMBOL	DESCRIPTION
A0 - A18	Address Inputs
DQ0 - DQ7	Data Inputs/Outputs
CE#	Chip Enable Inputs
WE#	Write Enable Input
OE#	Output Enable Input
V _{CC}	Power Supply
V _{SS}	Ground
NC	No Connection



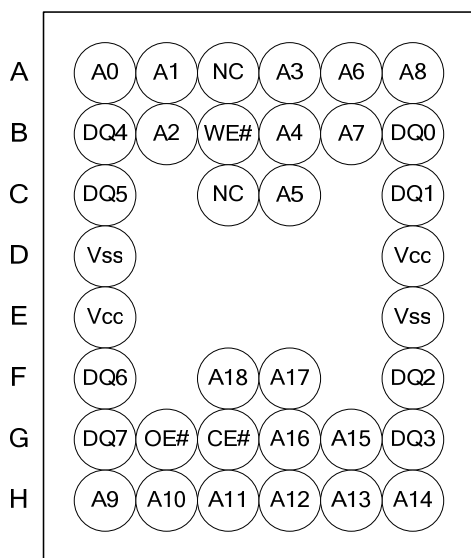
PIN CONFIGURATION



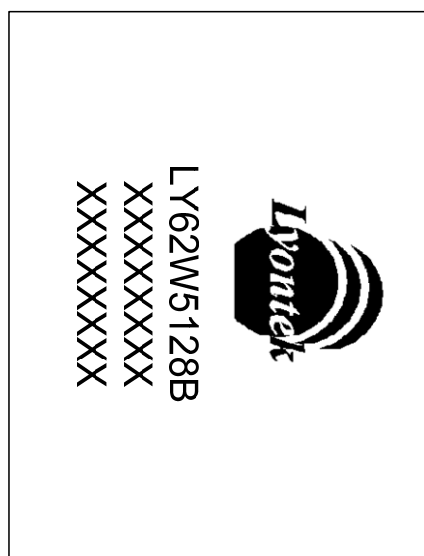
SOP



TSOP I / sTSOP



TFBGA(See through with Top View)



TFBGA(Top View)

**ABSOLUTE MAXIMUM RATINGS***

PARAMETER	SYMBOL	RATING	UNIT
Voltage on V_{CC} relative to V_{SS}	V_{T1}	-0.5 to 6.5	V
Voltage on any other pin relative to V_{SS}	V_{T2}	-0.5 to $V_{CC}+0.5$	V
Operating Temperature	T_A	0 to 70(C grade) -40 to 85(I grade)	°C
Storage Temperature	T_{STG}	-65 to 150	°C
Power Dissipation	P_D	1	W
DC Output Current	I_{OUT}	50	mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE#	OE#	WE#	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	High-Z	I_{SB1}
Output Disable	L	H	H	High-Z	I_{CC}, I_{CC1}
Read	L	L	H	D_{OUT}	I_{CC}, I_{CC1}
Write	L	X	L	D_{IN}	I_{CC}, I_{CC1}

Note: H = V_{IH} , L = V_{IL} , X = Don't care.



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP. ^{*4}	MAX.	UNIT	
Supply Voltage	V _{CC}			2.7	3.0	5.5	V	
Input High Voltage	V _{IH} ^{*1}	V _{CC} =4~5.5V		2.4	-	V _{CC} +0.3	V	
		V _{CC} =2.7~4V		2.2				
Input Low Voltage	V _{IL} ^{*2}	V _{CC} =4~5.5V		- 0.2	-	0.8	V	
		V _{CC} =2.7~4V				0.6		
Input Leakage Current	I _{LI}	V _{CC} ≥ V _{IN} ≥ V _{SS}		- 1	-	1	μA	
Output Leakage Current	I _{LO}	V _{CC} ≥ V _{OUT} ≥ V _{SS} , Output Disabled		- 1	-	1	μA	
Output High Voltage	V _{OH}	I _{OH} = -1mA		2.4	2.7	-	V	
Output Low Voltage	V _{OL}	I _{OL} = 2mA		-	-	0.4	V	
Average Operating Power supply Current	I _{CC}	Cycle time = MIN. CE# ≤ 0.2V, I _{I/O} = 0mA Other pins at 0.2V or V _{CC} -0.2V	- 45	-	15	25	mA	
			- 55	-	12	20	mA	
	I _{CC1}	Cycle time = 1μs CE# ≤ 0.2V, I _{I/O} = 0mA Other pins at 0.2V or V _{CC} -0.2V		-	3	5	mA	
Standby Power Supply Current	I _{SB1}	CE# ≥ V _{CC} -0.2V Others at 0.2V or V _{CC} - 0.2V	SL ^{*5}	25°C	-	2.2	5	μA
			SLI ^{*5}	40°C	-	3	6	μA
			SL		-	2.2	12	μA
			SLI		-	2.2	20	μA

Notes:

- $V_{IH}(\max) = V_{CC} + 3.0V$ for pulse width less than 10ns.
- $V_{IL}(\min) = V_{SS} - 3.0V$ for pulse width less than 10ns.
- Over/Undershoot specifications are characterized, not 100% tested.
- Typical values are included for reference only and are not guaranteed or tested.
Typical values are measured at $V_{CC} = V_{CC}(\text{TYP.})$ and $T_A = 25^{\circ}C$
- This parameter is measured at $V_{CC} = 3.0V$

CAPACITANCE ($T_A = 25^{\circ}C$, $f = 1.0MHz$)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Input Capacitance	C_{IN}	-	6	pF
Input/Output Capacitance	$C_{I/O}$	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0.2V to $V_{CC} - 0.2V$
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	$C_L = 30pF + 1TTL$, $I_{OH}/I_{OL} = -2mA/4mA$



AC ELECTRICAL CHARACTERISTICS

(1) READ CYCLE

PARAMETER	SYM.	LY62W5128B-45		LY62W5128B-55		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t _{RC}	45	-	55	-	ns
Address Access Time	t _{AA}	-	45	-	55	ns
Chip Enable Access Time	t _{ACE}	-	45	-	55	ns
Output Enable Access Time	t _{OE}	-	25	-	30	ns
Chip Enable to Output in Low-Z	t _{CLZ} *	10	-	10	-	ns
Output Enable to Output in Low-Z	t _{OLZ} *	5	-	5	-	ns
Chip Disable to Output in High-Z	t _{CHZ} *	-	20	-	20	ns
Output Disable to Output in High-Z	t _{OHZ} *	-	20	-	20	ns
Output Hold from Address Change	t _{OH}	10	-	10	-	ns

(2) WRITE CYCLE

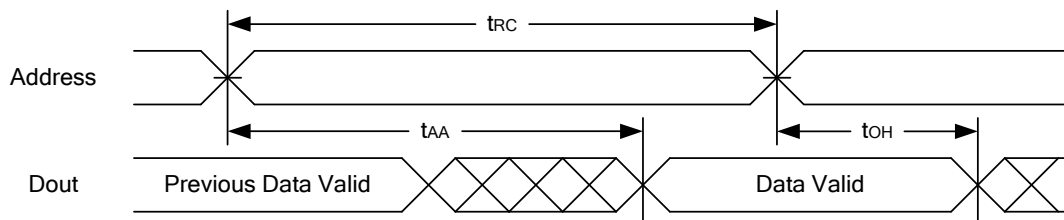
PARAMETER	SYM.	LY62W5128B-45		LY62W5128B-55		UNIT
		MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t _{WC}	45	-	55	-	ns
Address Valid to End of Write	t _{AW}	40	-	50	-	ns
Chip Enable to End of Write	t _{CW}	40	-	50	-	ns
Address Set-up Time	t _{AS}	0	-	0	-	ns
Write Pulse Width	t _{WP}	35	-	45	-	ns
Write Recovery Time	t _{WR}	0	-	0	-	ns
Data to Write Time Overlap	t _{DW}	20	-	25	-	ns
Data Hold from End of Write Time	t _{DH}	0	-	0	-	ns
Output Active from End of Write	t _{OW} *	5	-	5	-	ns
Write to Output in High-Z	t _{WHZ} *	-	20	-	20	ns

*These parameters are guaranteed by device characterization, but not production tested.

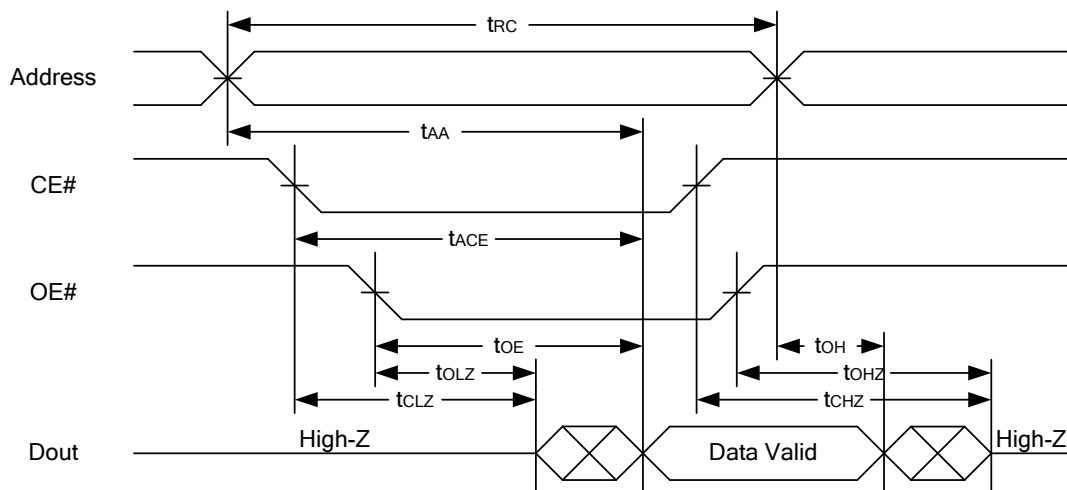


TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)



READ CYCLE 2 (CE# and OE# Controlled) (1,3,4,5)

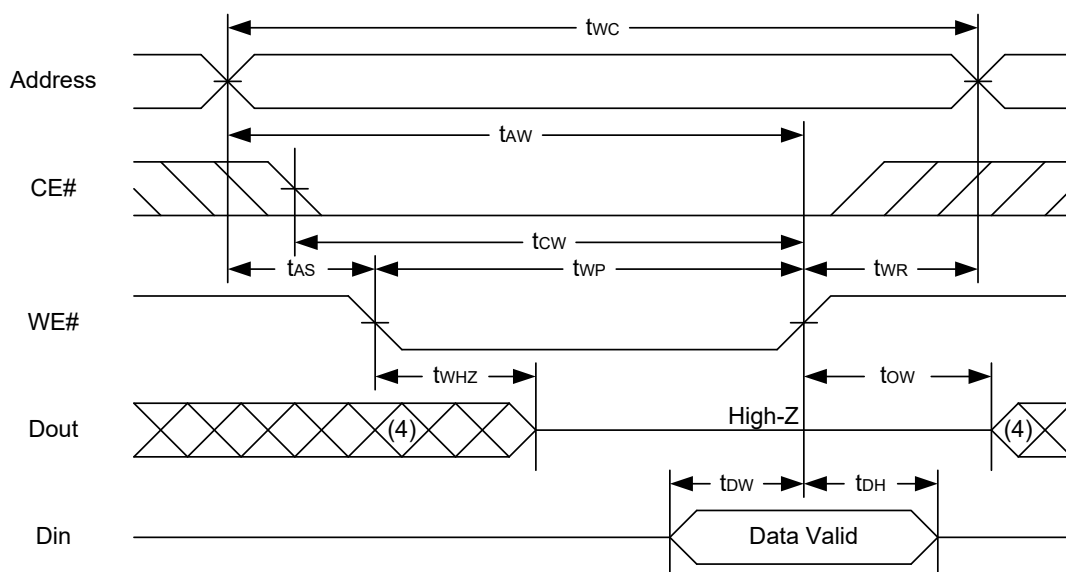


Notes :

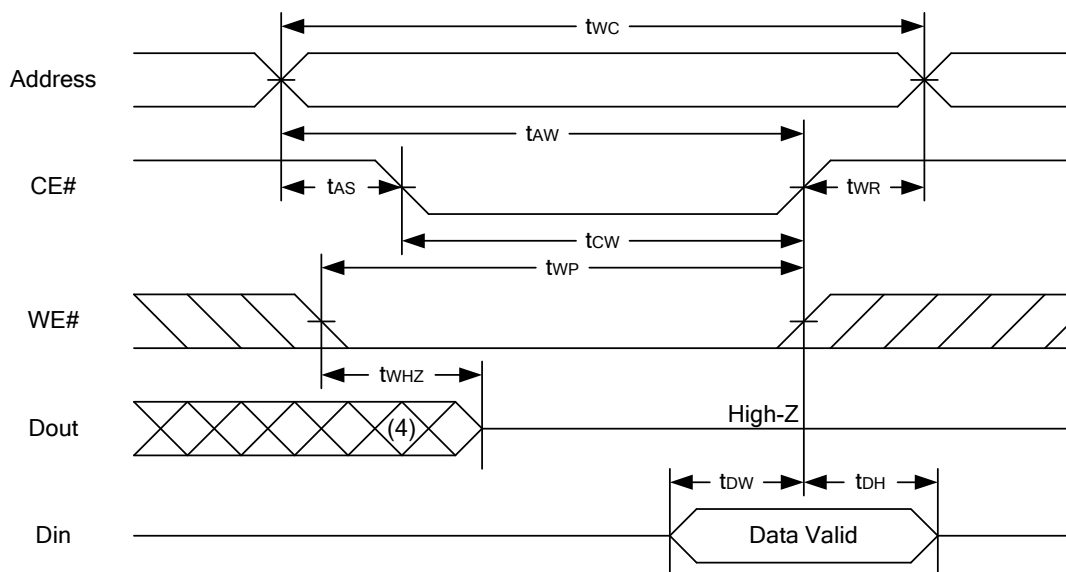
1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low.
3. Address must be valid prior to or coincident with CE# = low,; otherwise tAA is the limiting parameter.
4. tCLZ, tOLZ, tCHZ and toHZ are specified with CL = 5pF. Transition is measured ±500mV from steady state.
5. At any given temperature and voltage condition, tCHZ is less than tCLZ, toHZ is less than tOLZ.



WRITE CYCLE 1 (WE# Controlled) (1,2,4,5)



WRITE CYCLE 2 (CE# Controlled) (1,4,5)



Notes :

- 1.A write occurs during the overlap of a low CE#, low WE#.
- 2.During a WE# controlled write cycle with OE# low, t_{WP} must be greater than $t_{WHZ} + t_{DW}$ to allow the drivers to turn off and data to be placed on the bus.
- 3.During this period, I/O pins are in the output state, and input signals must not be applied.
- 4.If the CE# low transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
5. t_{OW} and t_{WHZ} are specified with $C_L = 5\text{pF}$. Transition is measured $\pm 500\text{mV}$ from steady state.

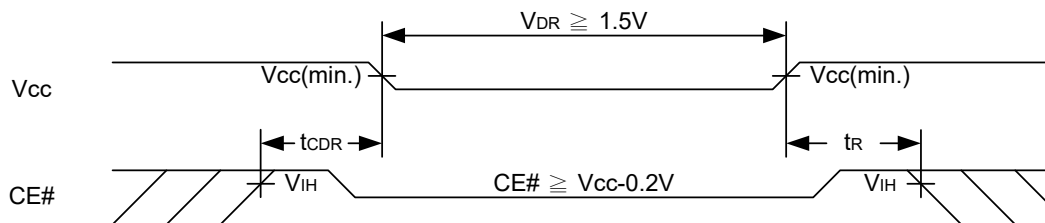


DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
V _{CC} for Data Retention	V _{DR}	CE# ≥ V _{CC} - 0.2V			1.5	-	5.5	V
Data Retention Current	I _{DR}	V _{CC} = 1.5V CE# ≥ V _{CC} - 0.2V Other pins at 0.2V or V _{CC} -0.2V	SL	25°C	-	2.2	5	μA
			SLI	40°C	-	3	6	μA
			SL		-	2.2	12	μA
			SLI		-	2.2	20	μA
Chip Disable to Data Retention Time	t _{CDR}	See Data Retention Waveforms (below)			0	-	-	ns
Recovery Time	t _R				t _{RC} *	-	-	ns

t_{RC}* = Read Cycle Time

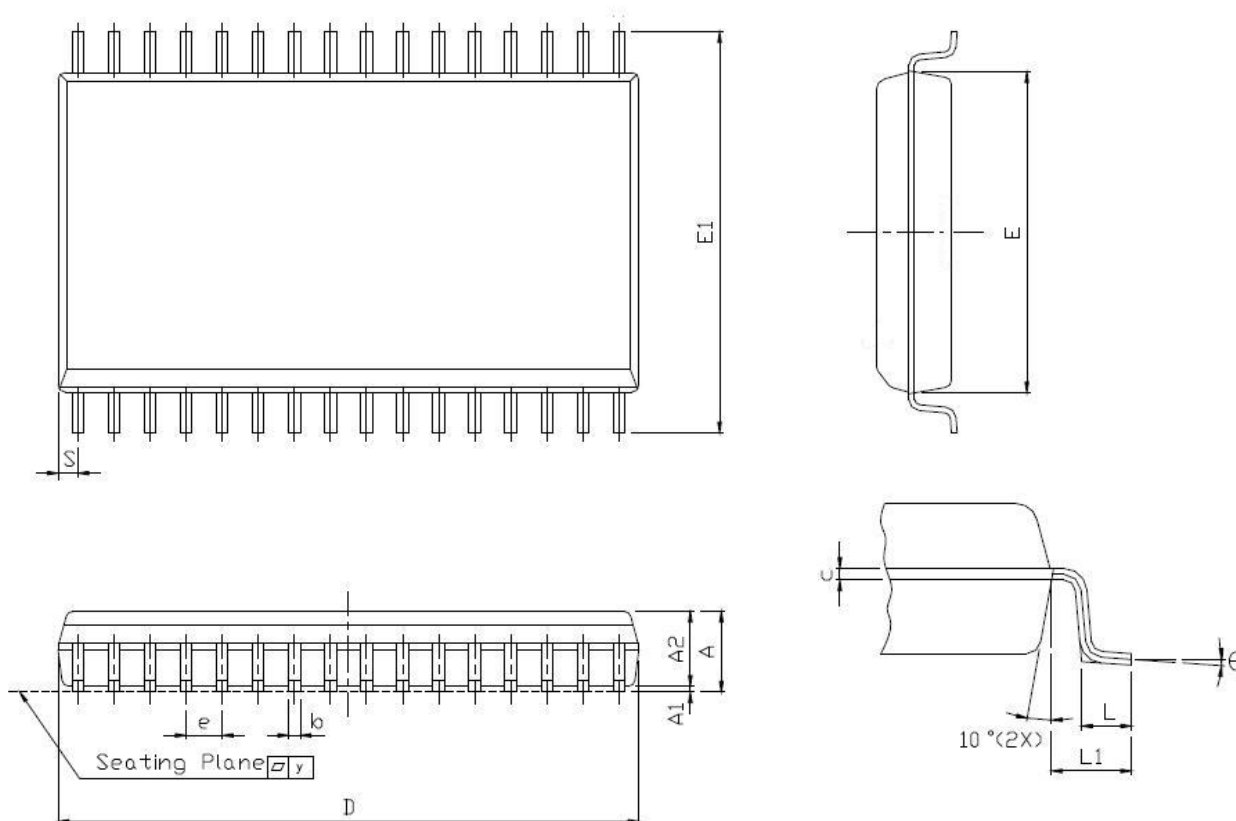
DATA RETENTION WAVEFORM





PACKAGE OUTLINE DIMENSION

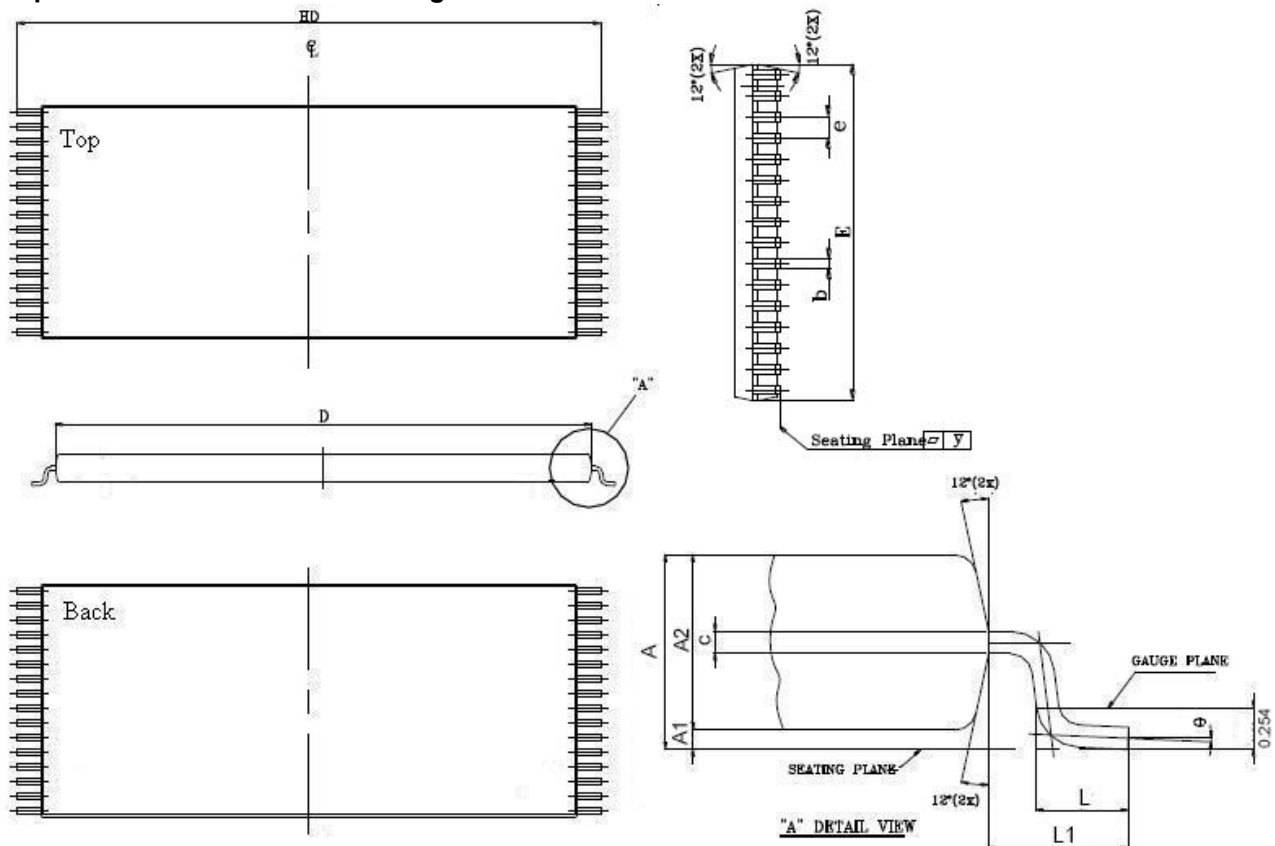
32-pin 450 mil SOP Package Outline Dimension



SYMBOL	UNIT	INCH.(BASE)	MM(REF)
A		0.120(MAX)	3.048(MAX)
A1		0.004(MIN)	0.102(MIN)
A2		0.116(MAX)	2.946(MAX)
b		0.016(TYP)	0.406(TYP)
c		0.008(TYP)	0.203(TYP)
D		0.817(MAX)	20.75(MAX)
E		0.445±0.006	11.303±0.152
E1		0.555±0.025	14.097±0.635
e		0.050(TYP)	1.270(TYP)
L		0.033±0.017	0.838±0.432
L1		0.055±0.008	1.397±0.203
S		0.026(MAX)	0.660(MAX)
y		0.004(MAX)	0.101(MAX)
Θ		0° -10°	0° -10°



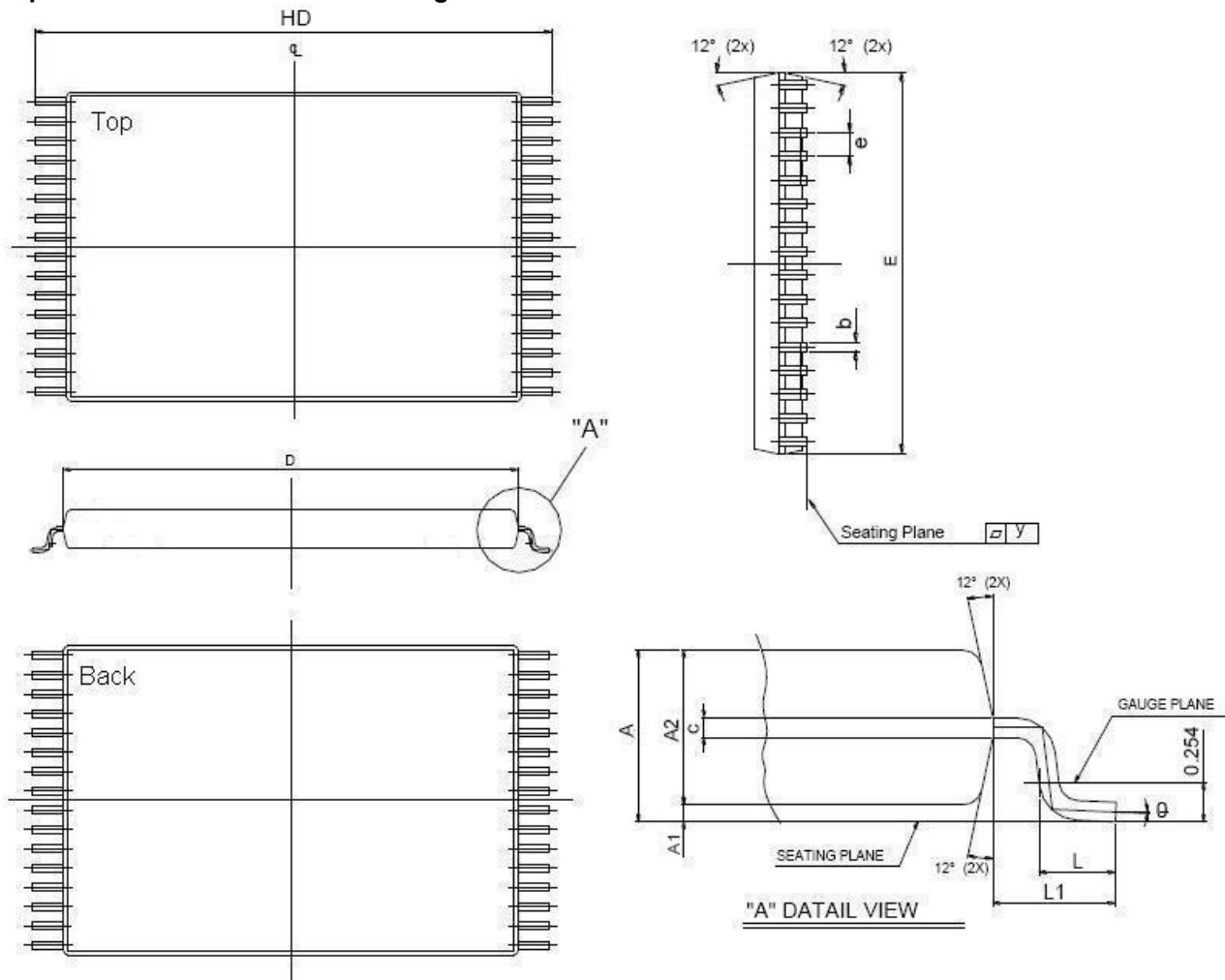
32-pin 8mm x 20mm TSOP I Package Outline Dimension



SYM.	UNIT	INCH(BASE)	MM(REF)
A		0.047 (MAX)	1.20 (MAX)
A1		0.004 $\pm$ 0.002	0.10 $\pm$ 0.05
A2		0.039 $\pm$ 0.002	1.00 $\pm$ 0.05
b		0.009 $\pm$ 0.002	0.22 $\pm$ 0.05
c		0.006 $\pm$ 0.002	0.155 $\pm$ 0.055
D		0.724 $\pm$ 0.008	18.40 $\pm$ 0.20
E		0.315 $\pm$ 0.008	8.00 $\pm$ 0.20
e		0.020 (TYP)	0.50 (TYP)
HD		0.787 $\pm$ 0.008	20.00 $\pm$ 0.20
L		0.024 $\pm$ 0.004	0.60 $\pm$ 0.10
L1		0.031 REF	0.8 REF
y		0.003 (MAX)	0.08 (MAX)
Θ		0°~5°	0°~5°

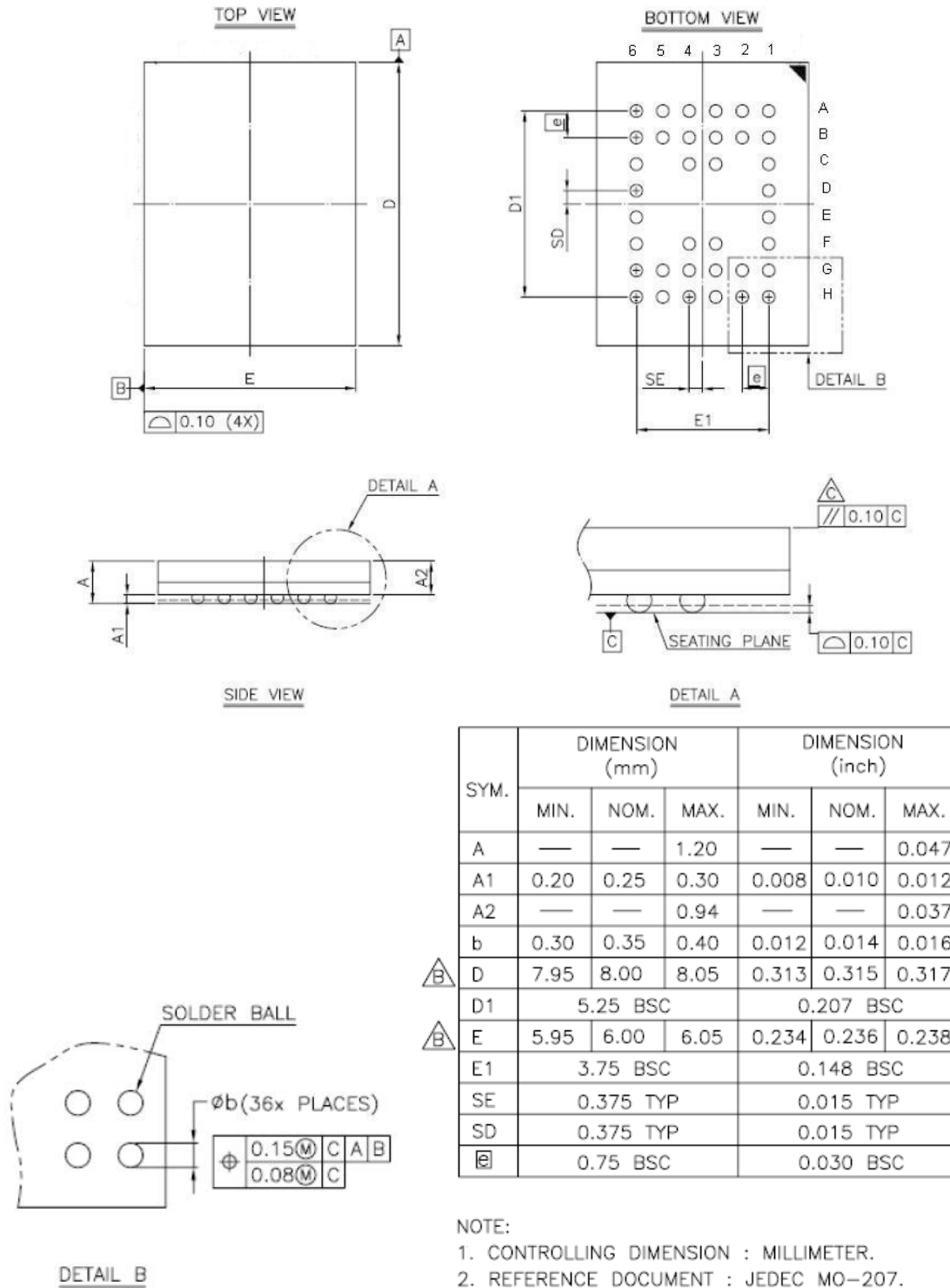


32-pin 8mm x 13.4mm sTSP Package Outline Dimension



SYM.	UNIT	INCH(BASE)	MM(REF)
A		0.049 (MAX)	1.25 (MAX)
A1		0.004 ±0.002	0.10 ±0.05
A2		0.039 ±0.002	1.00 ±0.05
b		0.009 ±0.002	0.22 ±0.05
c		0.006 ±0.002	0.155 ±0.055
D		0.465 ±0.008	11.80 ±0.20
E		0.315 ±0.008	8.00 ±0.20
e		0.020 (TYP)	0.50 (TYP)
HD		0.528±0.008	13.40 ±0.20.
L		0.02 ±0.008	0.50 ±0.20
L1		0.031 ±0.005	0.8 ±0.125
y		0.003 (MAX)	0.076 (MAX)
Θ		0°~5°	0°~5°

36-ball 6mm × 8mm TFBGA Package Outline Dimension





Lyontek Inc.

LY62W5128B

Rev. 1.4

512K X 8 BIT LOW POWER CMOS SRAM

ORDERING INFORMATION

Package Type	Access Time (Speed)(ns)	Power Type	Temperature Range(°C)	Packing Type	Lyontek Item No.
32-pin (450mil) SOP	45	Special Ultra Low Power	0°C~70°C	Tray	LY62W5128BSL-45SL
				Tape Reel	LY62W5128BSL-45SLT
			-40°C~85°C	Tray	LY62W5128BSL-45SLI
				Tape Reel	LY62W5128BSL-45SLIT
	55	Special Ultra Low Power	0°C~70°C	Tray	LY62W5128BSL-55SL
				Tape Reel	LY62W5128BSL-55SLT
			-40°C~85°C	Tray	LY62W5128BSL-55SLI
				Tape Reel	LY62W5128BSL-55SLIT



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LY62W5128B

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Package Type	Access Time (Speed)(ns)	Power Type	Temperature Range(°C)	Packing Type	Lyontek Item No.
32-pin (8mm x 20mm) TSOP I	45	Special Ultra Low Power	0°C~70°C	Tray	LY62W5128BLL-45SL
				Tape Reel	LY62W5128BLL-45SLT
			-40°C~85°C	Tray	LY62W5128BLL-45SLI
				Tape Reel	LY62W5128BLL-45SLIT
	55	Special Ultra Low Power	0°C~70°C	Tray	LY62W5128BLL-55SL
				Tape Reel	LY62W5128BLL-55SLT
			-40°C~85°C	Tray	LY62W5128BLL-55SLI
				Tape Reel	LY62W5128BLL-55SLIT



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Package Type	Access Time (Speed)(ns)	Power Type	Temperature Range(°C)	Packing Type	Lyontek Item No.
32-pin (8mm x 13.4mm) sTSOP	45	Special Ultra Low Power	0°C~70°C	Tray	LY62W5128BRL-45SL
				Tape Reel	LY62W5128BRL-45SLT
			-40°C~85°C	Tray	LY62W5128BRL-45SLI
				Tape Reel	LY62W5128BRL-45SLIT
	55	Special Ultra Low Power	0°C~70°C	Tray	LY62W5128BRL-55SL
				Tape Reel	LY62W5128BRL-55SLT
			-40°C~85°C	Tray	LY62W5128BRL-55SLI
				Tape Reel	LY62W5128BRL-55SLIT



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Package Type	Access Time (Speed)(ns)	Power Type	Temperature Range(°C)	Packing Type	Lyontek Item No.
36-ball (6mm x 8mm) TFBGA	45	Special Ultra Low Power	0°C~70°C	Tray	LY62W5128BGL-45SL
				Tape Reel	LY62W5128BGL-45SLT
			-40°C~85°C	Tray	LY62W5128BGL-45SLI
				Tape Reel	LY62W5128BGL-45SLIT
	55	Special Ultra Low Power	0°C~70°C	Tray	LY62W5128BGL-55SL
				Tape Reel	LY62W5128BGL-55SLT
			-40°C~85°C	Tray	LY62W5128BGL-55SLI
				Tape Reel	LY62W5128BGL-55SLIT



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